

## SWITCHING

## N-CHANNEL POWER MOS FET

## INDUSTRIAL USE

### DESCRIPTION

This product is N-Channel MOS Field Effect Transistor designed for power management applications and Li-ion battery application.

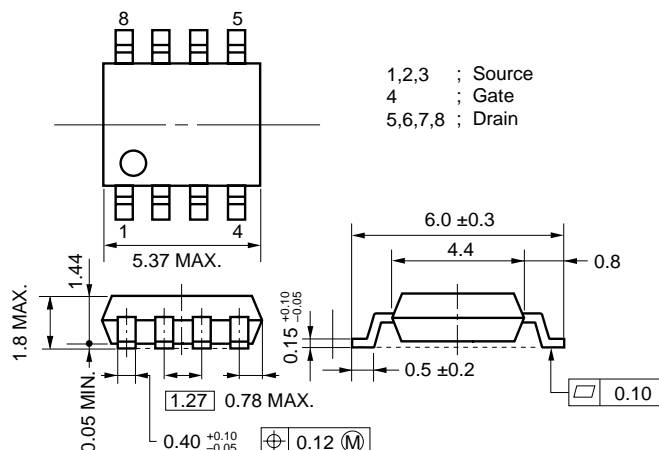
### FEATURES

- 2.5 V gate drive and low on-resistance  
 $R_{DS(on)1} = 9.5 \text{ m}\Omega$  (TYP.) ( $V_{GS} = 4.5 \text{ V}$ ,  $I_D = 5.0 \text{ A}$ )  
 $R_{DS(on)2} = 11.5 \text{ m}\Omega$  (TYP.) ( $V_{GS} = 2.5 \text{ V}$ ,  $I_D = 5.0 \text{ A}$ )
- Low  $C_{iss}$ :  $C_{iss} = 2000 \text{ pF}$  (TYP.)
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

### ORDERING INFORMATION

PART NUMBER	PACKAGE
$\mu$ PA1724G	Power SOP8

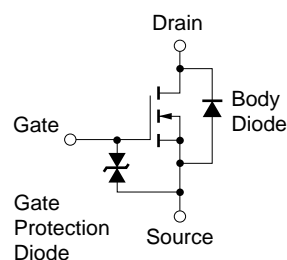
### PACKAGE DRAWING (Unit : mm)



### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ , All terminals are connected.)

Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DS}$	20	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GS}$	$\pm 12$	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 10$	A
Drain Current (pulse) <sup>Note1</sup>	$I_{D(pulse)}$	$\pm 40$	A
Total Power Dissipation ( $T_A = 25^\circ\text{C}$ ) <sup>Note2</sup>	$P_T$	2.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

### EQUIVALENT CIRCUIT



**Notes 1.**  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1 \%$

**2.** Mounted on ceramic substrate of  $1200 \text{ mm}^2 \times 1.7 \text{ mm}$

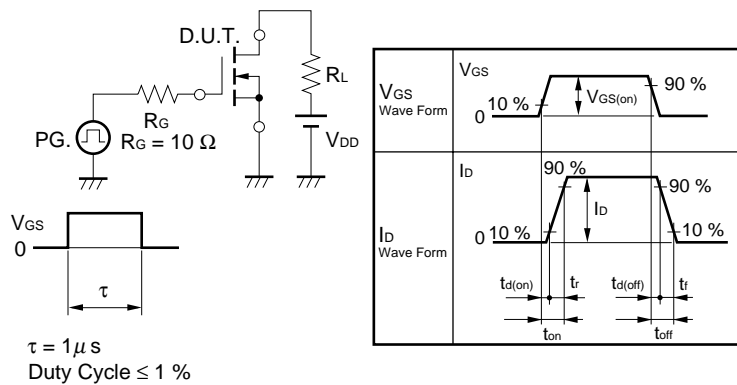
**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

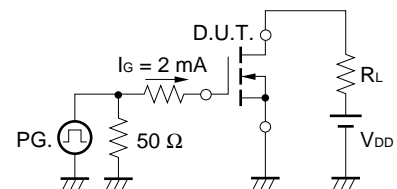
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, All terminals are connected.)**

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 5.0 A		9.5	12.0	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 5.0 A		11.5	15.5	mΩ
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	0.5	1.0	1.5	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 5.0 A	5.0			S
Drain Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V			10	μA
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±12 V, V <sub>DS</sub> = 0 V			±10	μA
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V		2000		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		600		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		420		pF
Turn-on Delay Time	t <sub>d(on)</sub>	I <sub>D</sub> = 5.0 A		25		ns
Rise Time	t <sub>r</sub>	V <sub>GS(on)</sub> = 4.5 V		210		ns
Turn-off Delay Time	t <sub>d(off)</sub>	V <sub>DD</sub> = 10 V		70		ns
Fall Time	t <sub>f</sub>	R <sub>G</sub> = 10 Ω		45		ns
Total Gate Charge	Q <sub>G</sub>	I <sub>D</sub> = 10 A		19		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>DD</sub> = 16 V		5		nC
Gate to Drain Charge	Q <sub>GD</sub>	V <sub>GS</sub> = 4.5 V		7		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 10 A, V <sub>GS</sub> = 0 V		0.83		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 10 A, V <sub>GS</sub> = 0 V		32		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A / μs		22		nC

**TEST CIRCUIT 1 SWITCHING TIME**



**TEST CIRCUIT 2 GATE CHARGE**



[MEMO]

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Anti-radioactive design is not implemented in this product.