Low Voltage Automotive Fast 64K x 16 SRAM

Features

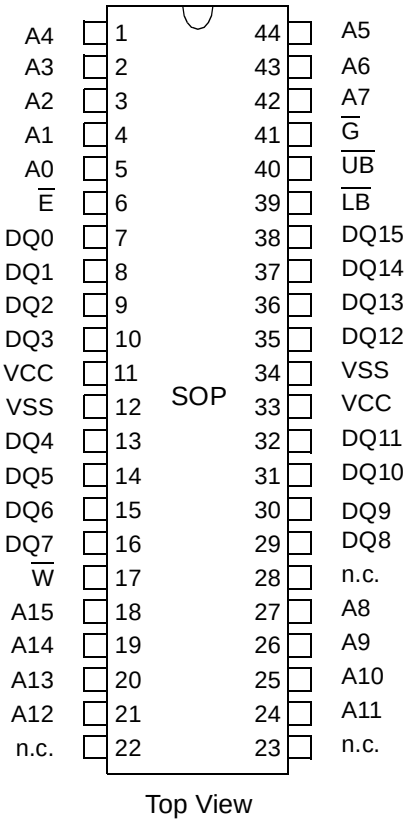
- ❒ 65536 x 16 bit static CMOS RAM
- ❒ 15 and 20 ns Access Time
- ❒ Common data inputs and data outputs
- ❒ Three-state outputs
- ❒ Standby current < 50 µA at 125°C
- ❒ Power supply voltage 2.5 V
- ❒ Operating temperature range
  K-Type:-40 °C to 85 °C
  A-Type:-40 °C to 125 °C
- ❒ CECC 90000 Quality Standard
- ❒ ESD protection > 2000 V (MIL STD 883C M3015.7)
- ❒ Latch-up immunity >100 mA
- ❒ Package: SOP44 (525 mil)

Description

The UL62H1616B is a static RAM manufactured using a CMOS process technology with the following operating modes:
- Lower / Upper Byte Read
- Word Read
- Lower / Upper Byte Write
- Word Write
- Standby
- Data Retention

The memory array is based on a 6-Transistor cell.
The circuit is activated by the falling edge of $\overline{E}$. The address and control inputs open simultaneously. According to the information of $\overline{W}$ and $\overline{G}$, the data inputs, or outputs, are active. During the active state $\overline{E}$ = L and $\overline{W}$ = H each address change leads to a new Read cycle. In a Read cycle, the data outputs are activated by the falling edge of $\overline{G}$. If $\overline{LB}$ = L the data lower byte will be available at the outputs DQ0-DQ7, on $\overline{UB}$ = L the data upper byte appear at the outputs DQ8-DQ15. After the address change, the data outputs go High-Z until the new information is available. The data outputs have no preferred state. The Read cycle is finished by the falling edge of $\overline{W}$, or by the rising edge of $\overline{E}$, respectively.
Data retention is guaranteed down to 2 V. With the exception of $\overline{E}$, all inputs consist of NOR gates, so that no pull-up/pull-down resistors are required.

Pin Configuration

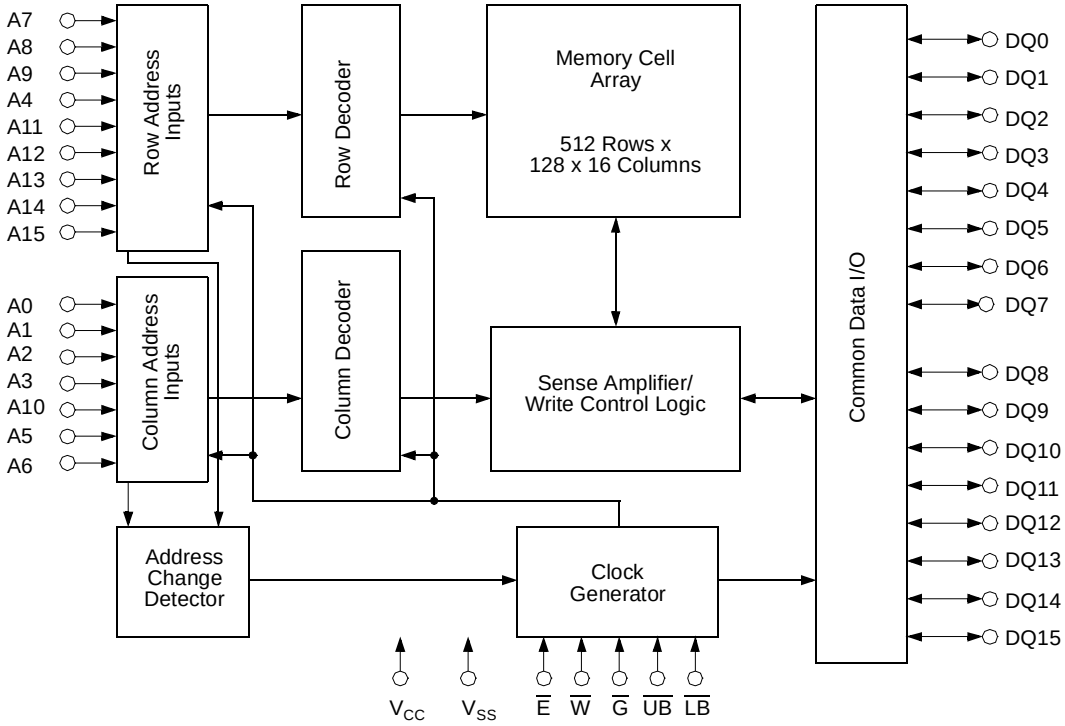


Top View

Pin Description

Signal Name	Signal Description
A0 - A15	Address Inputs
DQ0 - DQ15	Data In/Out
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{UB}$	Upper Byte Enable
$\overline{LB}$	Lower Byte Enable
VCC	Power Supply Voltage
VSS	Ground
n.c.	not connected

Block Diagram



Truth Table

Operating Mode	E	W	G	LB	UB	DQ0-DQ7	DQ8-DQ15
Standby/not selected	H	*	*	*	*	High-Z	High-Z
Internal Read	L L	H *	H *	* H	* H	High-Z	High-Z
Lower Byte Read	L	H	L	L	H	Data Outputs Low-Z	High-Z
Upper Byte Read	L	H	L	H	L	High-Z	Data Outputs Low-Z
Word Read	L	H	L	L	L	Data Outputs Low-Z	Data Outputs Low-Z
Lower Byte Write	L	L	*	L	H	Data Inputs High-Z	High-Z
Upper Byte Write	L	L	*	H	L	High-Z	Data Inputs High-Z
Word Write	L	L	*	L	L	Data Inputs High-Z	Data Inputs High-Z

* H or L

Characteristics

All voltages are referenced to V_{SS} = 0 V (ground).
All characteristics are valid in the power supply voltage range and in the operating temperature range specified.
Dynamic measurements are based on a rise and fall time of ≤ 5 ns, measured between 10 % and 90 % of V_I, as well as input levels of V_{IL} = 0 V and V_{IH} = 2.5 V. The timing reference level of all input and output signals is 1.2 V, with the exception of the t_{dis}-times and t_{en}-times, in which cases transition is measured ±200 mV from steady-state voltage.

Maximum Ratings		Symbol	Min.	Max.	Unit
Power Supply Voltage		V_{CC}	-0.3	3.6	V
Input Voltage		V_I	-0.3	V_{CC} + 0.3	V
Output Voltage		V_O	-0.3	V_{CC} + 0.3	V
Power Dissipation		P_D	-	1	W
Operating Temperature	K-Type A-Type	T_a	-40 -40	85 125	°C
Storage Temperature		T_{stg}	-65	150	°C
Output Short-Circuit Current at V_{CC} = 2.5 V and V_O = 0 V**		$\| I_{OS} \|$		100	mA

**Not more than 1 output should be shorted at the same time. Duration of the short circuit should not exceed 30 s.

Recommended Operating Conditions	Symbol	Conditions	Min.	Max.	Unit
Power Supply Voltage	V_{CC}		2.3	2.7	V
Input Low Voltage*	V_{IL}		-0.2	0.6	V
Input High Voltage	V_{IH}		2.0	V_{CC} + 0.2	V

* -2 V at Pulse Width 10 ns

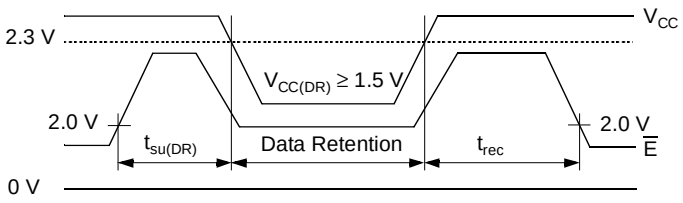
Electrical Characteristics	Symbol	Conditions	Min.	Max.	Unit
Supply Current - Operating Mode	$I_{CC(OP)}$	V_{CC} = 2.7 V V_{IL} = 0.6 V V_{IH} = 2.0 V t_{cW} = 35 ns t_{cW} = 55 ns t_{cW} = 60 ns		 90 70 60	 mA mA mA
Supply Current - Standby Mode (CMOS level)	$I_{CC(SB)}$	V_{CC} = 2.7 V $V_{\overline{E}}$ = V_{CC} - 0.2 V		50	µA
Supply Current - Standby Mode (LVTTL level)	$I_{CC(SB)1}$	V_{CC} = 2.7 V $V_{\overline{E}}$ = 2.0 V K-Type A-Type		 10 20	 mA mA
Output High Voltage	V_{OH}	V_{CC} = 2.3 V I_{OH} = -0.5 mA	2.0		V
Output Low Voltage	V_{OL}	V_{CC} = 2.3 V I_{OL} = 0.5 mA		0.4	V
Input High Leakage Current	I_{IH}	V_{CC} = 2.7 V V_{IH} = 2.7 V		2	µA
Input Low Leakage Current	I_{IL}	V_{CC} = 2.7 V V_{IL} = 0 V	-2		µA
Output High Current	I_{OH}	V_{CC} = 2.3 V V_{OH} = 2.0 V		-0.5	mA
Output Low Current	I_{OL}	V_{CC} = 2.3 V V_{OL} = 0.4 V	0.5		mA
Output Leakage Current High at Three-State Outputs	I_{OHZ}	V_{CC} = 2.7 V V_{OH} = 2.7 V		2	µA
Low at Three-State Outputs	I_{OLZ}	V_{CC} = 2.7 V V_{OL} = 0 V	-2		µA

Switching Characteristics Read Cycle	**Symbol**		**15**		**20**		**Unit**
	Alt.	**IEC**	**Min.**	**Max.**	**Min.**	**Max.**	
Read Cycle Time	t_{RC}	t_{cR}	15		20		ns
Address Access Time to Data Valid	t_{AA}	$t_{a(A)}$		15		20	ns
Chip Enable Access Time to Data Valid	t_{ACE}	$t_{a(E)}$		15		20	ns
$\overline{G}$ LOW to Data Valid	t_{OE}	$t_{a(G)}$		7		9	ns
$\overline{LB}$, $\overline{UB}$ LOW to Data Valid	t_B	$t_{a(B)}$		7		9	ns
$\overline{E}$ HIGH to Output in High-Z	t_{HZCE}	$t_{dis(E)}$		7		8	ns
$\overline{G}$ HIGH to Output in High-Z	t_{HZOE}	$t_{dis(G)}$		7		8	ns
$\overline{LB}$, $\overline{UB}$ HIGH to Output in High-Z	t_{HZB}	$t_{dis(B)}$		7		8	ns
$\overline{E}$ LOW to Output in Low-Z	t_{LZCE}	$t_{en(E)}$	4		4		ns
$\overline{G}$ LOW to Output in Low-Z	t_{LZOE}	$t_{en(G)}$	0		0		ns
$\overline{LB}$, $\overline{UB}$ LOW to Output in Low-Z	t_{LZB}	$t_{en(B)}$	0		0		ns
Output Hold Time from Address Change	t_{OH}	$t_{v(A)}$	3		3		ns
$\overline{E}$ LOW to Power-Up Time	t_{PU}		0		0		ns
$\overline{E}$ HIGH to Power-Down Time	t_{PD}			15		20	ns

Switching Characteristics Write Cycle	**Symbol**		**15**		**20**		**Unit**
	Alt.	**IEC**	**Min.**	**Max.**	**Min.**	**Max.**	
Write Cycle Time	t_{WC}	t_{cW}	15		20		ns
Write Pulse Width	t_{WP}	$t_{w(W)}$	10		12		ns
Write Setup Time	t_{WP}	$t_{su(W)}$	10		12		ns
Address Setup Time	t_{AS}	$t_{su(A)}$	0		0		ns
Address Valid to End of Write	t_{AW}	$t_{su(A-WH)}$	10		12		ns
Chip Enable Setup Time	t_{CW}	$t_{su(E)}$	10		12		ns
Byte Enable Setup Time	t_{BW}	$t_{su(B)}$	10		12		ns
Pulse Width Chip Enable to End of Write	t_{CW}	$t_{w(E)}$	10		12		ns
Pulse Width Byte Enable to End of Write	t_{BW}	$t_{w(B)}$	10		12		ns
Data Setup Time	t_{DS}	$t_{su(D)}$	7		9		ns
Data Hold Time	t_{DH}	$t_{h(D)}$	0		0		ns
Address Hold from End of Write	t_{AH}	$t_{h(A)}$	0		0		ns
$\overline{W}$ LOW to Output in High-Z	t_{HZWE}	$t_{dis(W)}$		7		8	ns
$\overline{G}$ HIGH to Output in High-Z	t_{HZOE}	$t_{dis(G)}$		7		8	ns
$\overline{W}$ HIGH to Output in Low-Z	t_{LZWE}	$t_{en(W)}$	3		3		ns
$\overline{G}$ LOW to Output in Low-Z	t_{LZOE}	$t_{en(G)}$	0		0		ns

Data Retention Mode

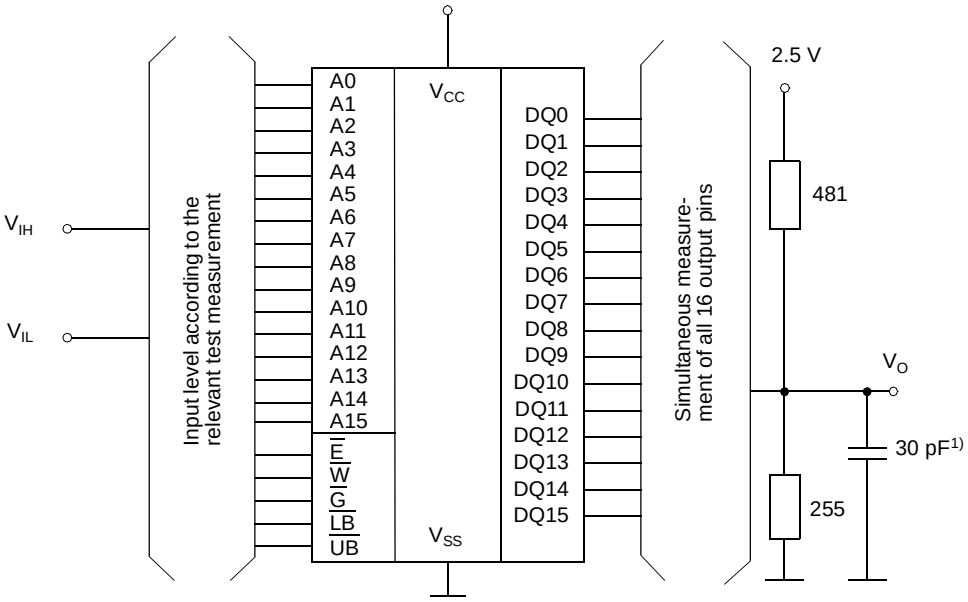
$\overline{E}$ - controlled



$V_{CC(DR)} - 0.2\ V \leq V_{\overline{E}(DR)} \leq V_{CC(DR)} + 0.3\ V$

Data Retention Characteristics	Symbol		Conditions	Min.	Typ.	Max.	Unit
	Alt.	IEC					
Data Retention Supply Voltage		$V_{CC(DR)}$		1.5		2.7	V
Data Retention Supply Current		$I_{CC(DR)}$	$V_{CC(DR)}$ = 2 V $V_{\overline{E}}$ = $V_{CC(DR)}$ - 0.2 V			30	µA
Data Retention Setup Time	t_{CDR}	$t_{su(DR)}$	See Data Retention Waveforms (above)	0			ns
Operating Recovery Time	t_R	t_{rec}		t_{cR}			ns

Test Configuration for Functional Check

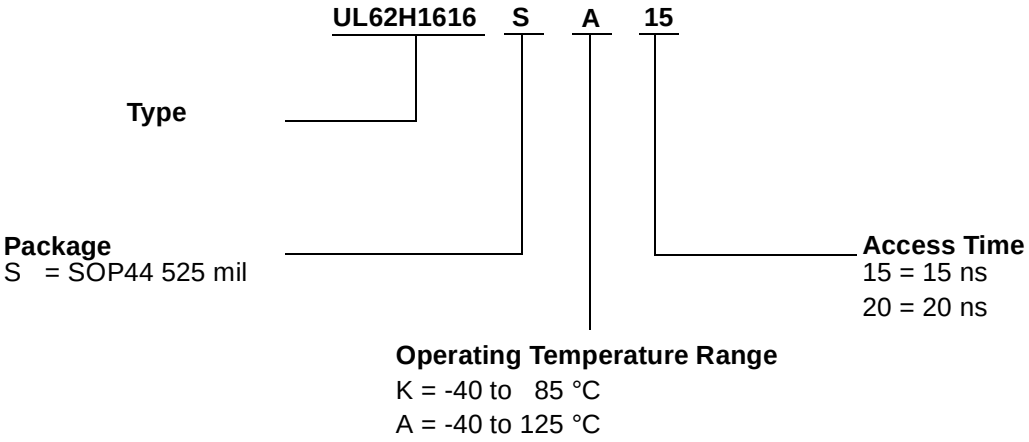


[1)] In measurement of $t_{dis(E)}$,$t_{dis(W)}$, $t_{en(E)}$, $t_{en(W)}$, $t_{en(G)}$ the capacitance is 5 pF.

Capacitance	Conditions	Symbol	Min.	Max.	Unit
Input Capacitance	V_{CC} = 2.5 V V_I = V_{SS} f = 1 MHz T_a = 25 °C	C_I		7	pF
Output Capacitance		C_o		7	pF

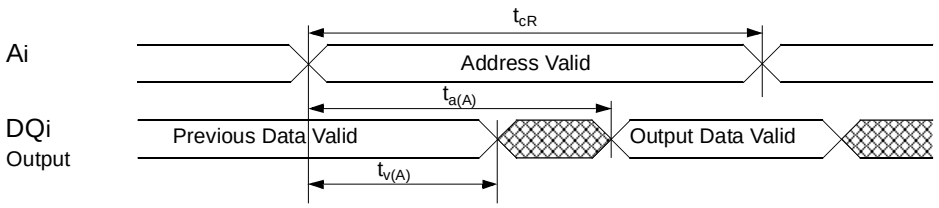
All pins not under test must be connected with ground by capacitors.

IC Code Numbers

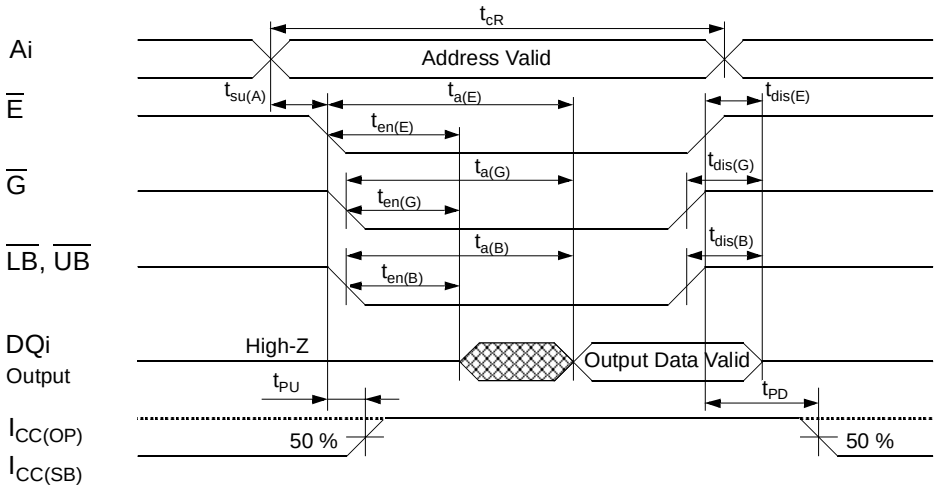


The date of manufacture is given by the last 4 digits of the mark, the first 2 digits indicating the year, and the last 2 digits the calendar week.

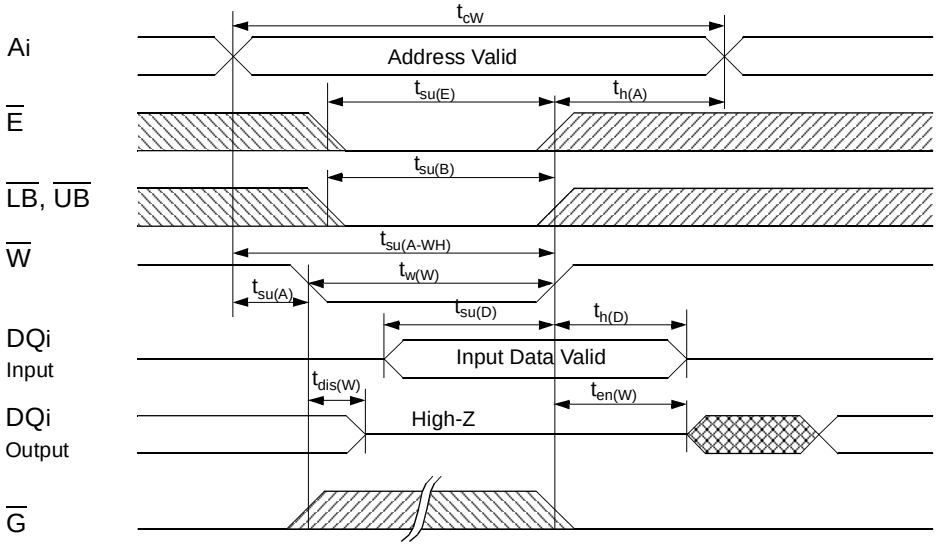
Read Cycle 1: A_i-controlled (during Read Cycle : $\overline{E}$ = $\overline{G}$ = V_{IL}, $\overline{W}$ = V_{IH})



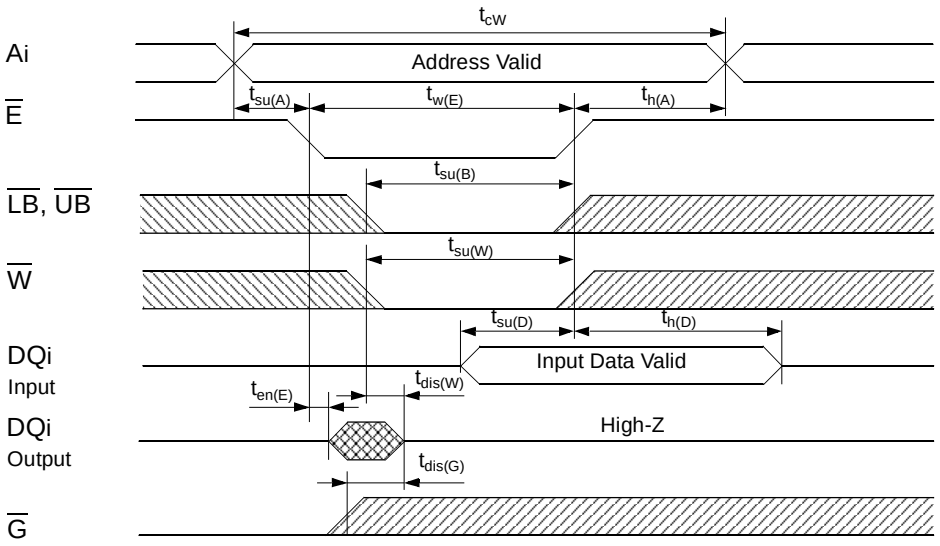
Read Cycle 2: $\overline{G}$-, $\overline{E}$-, $\overline{LB}$-, $\overline{UB}$-controlled (during Read Cycle: $\overline{W}$ = V_{IH})



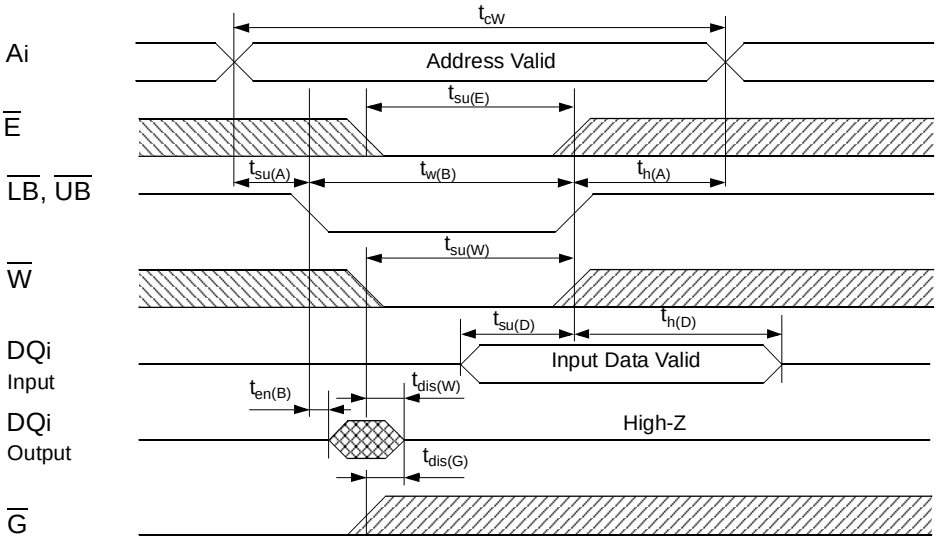
Write Cycle1: $\overline{W}$-controlled



Write Cycle 2: $\overline{E}$-controlled



Write Cycle 3: $\overline{LB}$-, $\overline{UB}$-controlled



undefined L- to H-level H- to L-level

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Zentrum Mikroelektronik Dresden AG
Grenzstraße 28 • D-01109 Dresden • P. O. B. 80 01 34 • D-01101 Dresden • Germany
Phone: +49 351 8822 306 • Fax: +49 351 8822 337 • Email: sales@zmd.de • http://www.zmd.de