APPLICATIONS NOTEBOOK: CLARIFYING the 2953/2954 REPLACEMENT/SUBSTITUTION

APPLICATIONS: EXISTING 2953/54 DESIGNS NECESSITATIONG CONVERSION TO NEWER ICs

SYNOPSIS

Earlier, the UDN2953B and UDN2954W were included in a product status change listing. These motor ICs were discontinued as of year end 1995; thus, numerous questions and dialogues have ensued. The objective of this applications note is the clarification of suitable alternative motor driver ICs, and the distinctions between the fading ICs and the replacements. The *interim* solutions for designers unable (or unwilling) to redesign circuit boards are the A3951SB (supersedes 2953B) and/or A3951SW (replaces 2954W). However, despite having identical package connections, there are *nuances* that should be identified and understood before directly substituting for the 2953B/2954W. Further, new designs should *"leapfrog"* the 3951 and utilize the complete capabilities of A3952.

The A3952 has *different* lead connections, plus a number of improvements that should be recognized; however, the emphasis here is clarifying the substitution perspective. A straightforward technique for distinguishing the differences in operation and ratings will be presented for the three motor ICs (2953 vs 2954 differences relate to packaging).

ABSOLUTE MAXIMUM RATINGS

Rather than list all the absolute maximums, only the dissimilarities are listed. All three full-bridge PWM motor ICs specify identical continuous current (2 A), maximum voltage (50V), and logic supply power (7.0V); but other basic distinctions involve:

2953/54 Output Current (Peak)*	$\pm$3.5 A
3951/52 Output Current ($t_w \leq$20 us)	$\pm$3.5 A

Pulse width noted for 3951/3952; sustained operation @ $\pm$3.5 A* damages (or destroys) these high-current motor control ICs.

2953/54	Flyback Voltage, V_K	V_{BB}
3951/52	Flyback	Internal Connection

No connection changes should be affected.

2953/54	Min. Clamp Voltage, V_A	Ground
3951/52	Clamping	Internal Connection

Normally, no connection changes expected.

2953/54 Logic Input Voltage

V_{PHASE} V_{ENABLE} V_{BB}

3951/52 Logic Input Voltage Range

V_{IN} -0.3 V to V_{CC} +0.3 V

Seldom is this logic input voltage an issue; however, both Phase and Enable inputs are limited to the range specified above.

2953/54 Reference Voltage (max)	15 V
3951 Reference Voltage (max)	V_{CC}
3952 Reference Voltage (max)	15 V

REFERENCE VOLTAGE RANGES

The 2953/2954 and 3951 reference input is a dual function control, but there are other disparities between the devices. Braking is a single, shared input on both 2953/54 and 3951. Switching the combined $V_{REF/\overline{BRAKE}}$ input to a logic LOW ($\leq$0.8 V) actuates the dynamic braking on the 2953/54 and 3951.

The 3952 has separate inputs for Reference and $\overline{\text{Braking}}$; this allows a broader range of PWM current control than the 2953/54 or 3951 (as enumerated below).

2953/54 Reference Range ≥2.4 V to ≤15 V
3951 Reference Range ≥2.4 V to V_{CC}
3952 Reference Range V_{REF} 0V to 15 V

OTHER REFERENCE VOLTAGE CONCERNS

The 2953/54 design allowed PWM operation *without* connecting a reference input; these devices internally default to V_{CC} ÷2 as the voltage reference. But *neither* the 3951 or 3952 function in this condition; a suitable, stable voltage (V_{REF}) *must* be connected to the newer ICs. Converting 2953/54 designs lacking this V_{REF} connection *necessitates* a reference voltage (V_{CC}), plus *doubling* the sense resistor to provide the same current.

With no reference voltage applied, typically the 2953/54 "defaults" to 2.5 V (5.0 V logic supply). The PWM output current is based on two factors: V_{REF} and (10x) R_{SENSE}; thus, the 2953/54 internal default to "half-supply" converts to 3951/52 operation via doubling R_S (to conform to the formula below):

$$I_{TRIP} = \frac{V_{REF}}{10 * R_{SENSE}} \text{ (Normal PWM)}$$

All devices have a continuous output rating of 2.0 A; hence, the trip current should *not* exceed this value. As mentioned, operating the ICs above 2.0 A can damage or destroy any of these bridge circuits; also, dynamic braking can induce (uncontrolled dc) peak currents that the 2953/54 cannot sustain.

SAFE DYNAMIC BRAKING: Utilize the 3952

Neither the 2953 nor 2954 integrate control of the (peak) current in the braking mode. Only the 3951 and 3952 incorporate control of output current during braking operation; and safe, reliable dynamic braking is often a formidable design problem. Realistically, the 3952 is the only suitable driver for safe braking. The 3951 is severely restricted by both its reference voltage limit and range.

Safe braking current, plus PWM regulation, of **3952s** involve: V_{REF} = 15 V; R_S = 0.75 Ω; V_{SENSE} = 1.5 V. This combination meets the 2.0 A limit during PWM operation and under default braking conditions. However, **3951s cannot** satisfy both PWM and braking limits together; with V_{REF} = 5 V, and I_{TRIP} = 2.0 A, R_S = 0.25 Ω. With these conditions, default braking current ≈ 6 A (i.e. 1.5V ÷ 0.25 Ω), a value that **greatly exceeds** safe limits.

DEVICE TRUTH TABLES

Although the 2953/54 and 3951 terminology and sequence in the respective truth tables differ, the ICs function identically. Further, the A3951 truth table includes a description column indicating the mode of operation.

Truth Table: UDN2953B and UDN2954W

Output Enable	Phase	$\frac{V_{REF}}{BRAKE}$	OUT_A	OUT_B
Low	High	>2.4 V	High	Low
Low	Low	>2.4 V	Low	High
High	X	>2.4 V	Open	Open
X	X	<0.8 V	High	High

X = irrelevant

Truth Table: A3951SB and A3951SW

BRAKE	ENABLE	PHASE	OUT_A	OUT_B	DESCRIPTION
H	H	X	Z	Z	Outputs Disabled
H	L	H	H	L	Forward
H	L	L	L	H	Reverse
L	X	X	L	L	Brake, See Note

X = Irrelevant Z = High Impedance (source and sink both OFF)
NOTE: Includes internal default V_{SENSE} level for over-current protection.

The A3952 incorporates one additional logic input (MODE) that expands motor function via offering new drive methods (i.e. "sleep", standby, and four-quadrant operation). By adding the MODE input the 3952 truth table is enlarged; with safe, dynamic braking and effective microstepping added (fast-decay) as options in the complete truth table.

Truth Table: A3952SB/SEB/SLB/SW

BRAKE	ENABLE	PHASE	MODE	OUT_A	OUT_B	DESCRIPTION
H	H	X	H	Z	Z	Sleep Mode
H	H	X	L	Z	Z	Standby, Note 1
H	L	H	H	H	L	Forward, Fast-Decay Mode
H	L	H	L	H	L	Forward, Slow-Decay Mode
H	L	L	H	L	H	Reverse, Fast-Decay Mode
H	L	L	L	L	H	Reverse, Slow-Decay Mode
L	X	X	H	L	L	Brake, Fast-Decay Mode
L	X	X	L	L	L	Brake, No Current Control, Note 2

X = Irrelevant Z = High Impedance (source and sink both OFF)
NOTES:
1. Includes active pull-offs for power outputs
2. Includes internal default V_{SENSE} level for over-current protection.

CURRENT CONTROL OPTIONS

Only the 2953/2954 specifications include a table listing the current control techniques. A comprehensive table which encompasses all three full-bridge motor ICs distinguishes the differences between operating methods and (where applicable) component values. Although this information is included in our IC specifications, this table summarizes and simplifies the comparison and alleviates the device substitution process.

SUMMARY

Existing designs using either the UDN2953B and/or UDN2954W *must be converted* to the newer ICs. As cited, *"leapfrogging"* beyond the A3951 to the A3952 is *(very strongly)* recommended. This involves PCB redesign; but provides the better long-range solution. Further, the A3952 offers superior benefits in protective functions (especially reliable, safe, current controlled braking). **Note**: the RC network capacitor value *must be increased* (per the table below). Also, the minimum resistor value decreases.

Please provide this applications material to all known 2953/54 customers. Refer other pertinent concerns and questions to Allegro Applications: Paul Emerald @ 508/854-5267 or John Pyle @ 508/854-5333.

CURRENT CONTROL ALTERNATIVES

	Circuit Package Connections				
CONTROL OPTION	P/N	V_{REF} INPUT	RC INPUT (TIMING)	V_{SENSE}	$\overline{\text{ENABLE}}$
NO PWM (DC MODE)	2953 *	Vcc or HIGH	≥2.0kΩ to GROUND	GROUND	LOW
	3951	Vcc or HIGH	OPEN (or RC to GND)	GROUND	LOW
	3952	Vcc or HIGH	OPEN (or RC to GND)	GROUND	LOW
PWM (INTERNAL TIMING)	2953 *	Vcc or HIGH	Vcc	Rsense	LOW
	3951	NO INTERNAL TIMING CIRCUITRY; RC NETWORK REQUIRED			
	3952	NO INTERNAL TIMING CIRCUITRY; RC NETWORK REQUIRED			
PWM (EXTERNAL TIMING)	2953*	2.4V-15V* or Vcc	20-100kΩ/200-500pF	Rsense	LOW
	3951	2.4V to Vcc*	12-100kΩ/0.82-1.5nF	Rsense	LOW
	3952	≤0V-15V* or Vcc	12-100kΩ/0.82-1.5nF	Rsense	LOW
EXTERNAL PWM	2953*	Vcc or HIGH¶	≥20kΩ to GROUND	Rsense¶	TOGGLE**
	3951	>2.4V-5V* or Vcc¶	12-100kΩ/0.82-1.2nF	Rsense¶	TOGGLE***
	3952	>0V-15V* or Vcc¶	12-100kΩ/0.82-1.2nF	Rsense¶	TOGGLE***

NOTES: * Applies to both UDN2953B and UDN2954W; * Variable, programmable reference (ex: D/A converter)
¶Default (Peak) ITRIP can be set for protection; ** Closed-loop speed/position control applications
¶Default (Peak) ITRIP can be set for protection; *** Closed-loop speed/position control applications;
Also, 3951/3952 allow utilizing both 2-quadrant and 4-quadrant current control.