

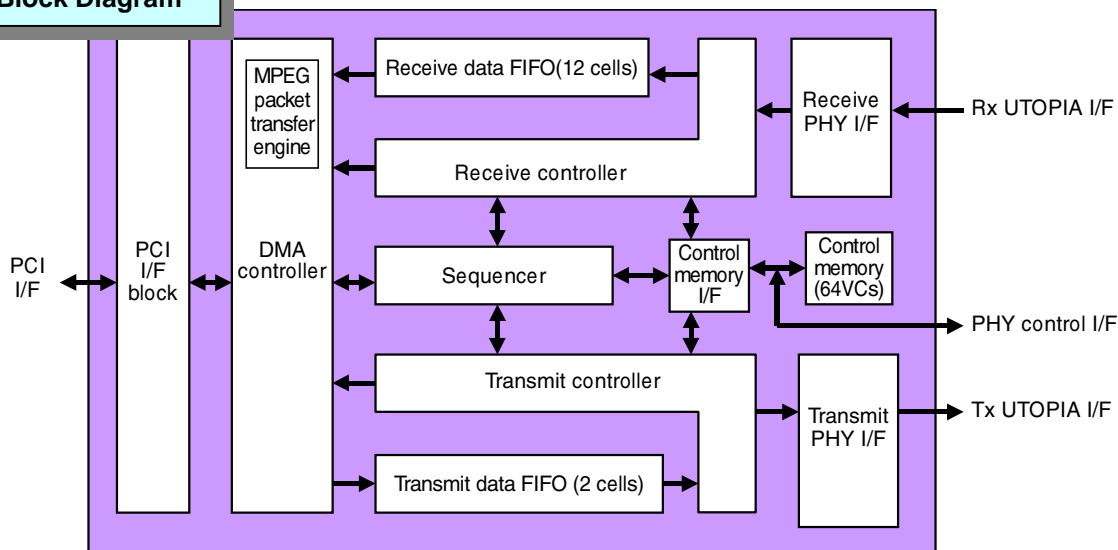
μPD98409

ATM LIGHT SAR CONTROLLER (NEASCOT-S40C™)

Features

- Conforms to the ATM-Forum recommendations
- Implements PCI bus interface (5/3.3 V, 32-bit, 33 MHz): PCI Specification Revision 2.1 compliant
- Implements AAL-5 SAR sublayer and ATM layer
- AAL-5 type supported in hardware (non AAL-5 types can be supported in software)
- Supports up to 64 virtual channels (VCs) (Integrated 64 VCs control memory)
- Two traffic shapers for transmission scheduling
- MPEG packet transfer engine to reduce transfer overhead of compressed picture data
- Integrated 12-cell receive FIFO
- PHY device interface: UTOPIA Level-1 interface (Octet/Cell level handshake)
- JTAG boundary scan test function
- 0.35 μm CMOS process, +5/+3.3 V power supply
 - Host bus interface +5 V: +5 V and +3.3 V power supply
 - Host bus interface +3.3 V mode: +3.3 V power supply
- 240-pin plastic QFP (FINE PITCH)(32 x 32)

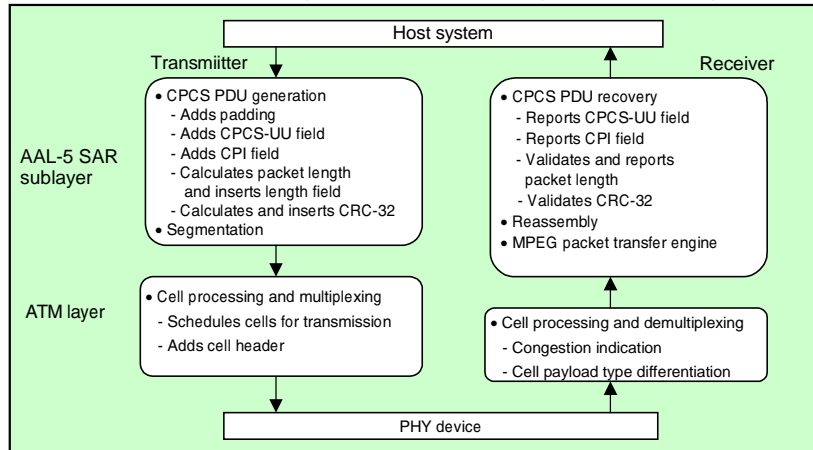
Block Diagram



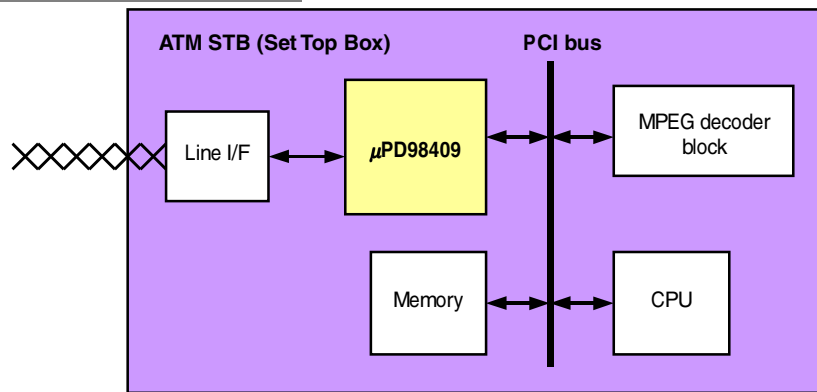
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Functions Overview

The μ PD98409 supports the ATM adaptation layer (AAL-5 SAR sublayer) and ATM layer function in hardware.



Sample Configuration of Application



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