

# 0.5 $\mu$ m CMOS Gate Array CMOS-N5 Family

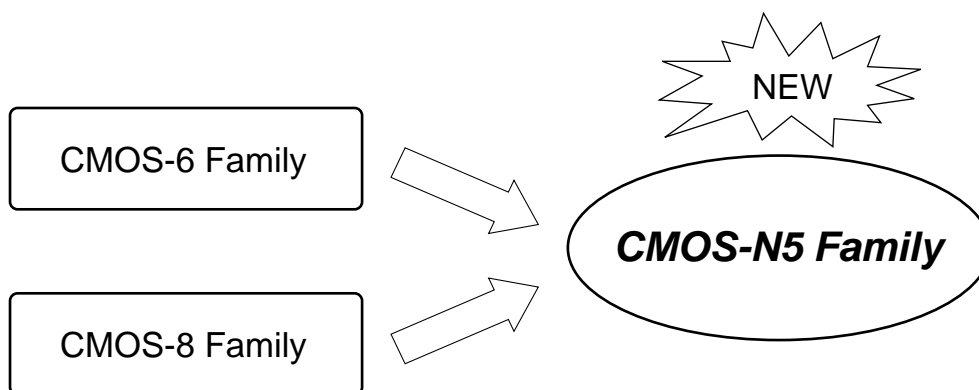


*High-speed operation with a 5-V power supply voltage  
Drastic cost reduction*

**New  
Products**

# Features

The CMOS-N5 family is a channel-less type gate array that provides high speed operation with a 5-V power supply voltage. Drastic cost reductions have been achieved compared with the conventional CMOS-6 and CMOS-8 families thanks to higher integration by the adoption of 0.5  $\mu\text{m}$  technology (2-layer wiring), and lowering the package assembly cost. Moreover, the 3-V power supply voltage is supported for the CMOS-N5 family.



## [Integration]

- 3K to 120K gates (number of integrated gates)
- 2K to 86K gates (number of usable gates)

## [Package]

- QFP (Fine pitch) 160 to 304 pins
- TQFP 48 to 80 pins
- LQFP 44 to 160 pins

## [High-speed operation] (preliminary)

- $t_{PD} = 0.26 \text{ ns}$  (2-input NAND (power gate), fanout = 2, standard wiring length)
- Operating frequency: 60 MHz max.

## [Function blocks]

- CPU peripheral block
- RAM block (1 port/2 ports)
- Oscillation block
- CTS block

## [Test design]

- Scan path test

# Product Overview

## Product type list

Product name	$\mu$ PD65880	$\mu$ PD65881	$\mu$ PD65882	$\mu$ PD65883	$\mu$ PD65884
Number of integrated gates <sup>Note 1</sup>	3456	5880	13952	25344	33864
Number of usable gates <sup>Note 2</sup>	2764	4704	11161	20275	27091
Number of pads <sup>Note 3</sup>	72	88	120	160	184
Internal gate	0.46 ns (fanout = 2, wiring length=2mm)				
Power gate	0.30 ns (fanout = 2, wiring length=2mm)				
Input buffer	0.33 ns (fanout = 2, wiring length=2mm)				
Output buffer	1.30 ns ( $C_L = 15$ pF)				
Output drive capability	$I_{OL} = 3, 6, 9, 12, 18, 24$ mA				
Power supply voltage	5 V $\pm$ 10 % (CMOS level)				

Product name	$\mu$ PD65885	$\mu$ PD65887	$\mu$ PD65889	$\mu$ PD65890	$\mu$ PD65893
Number of integrated gates <sup>Note 1</sup>	40768	56496	76000	99528	123384
Number of usable gates <sup>Note 4</sup>	28537	39547	53200	69669	86368
Number of pads <sup>Note 3</sup>	244	284	324	372	412
Internal gate	0.46 ns (fanout = 2, wiring length=2mm)				
Power gate	0.30 ns (fanout = 2, wiring length=2mm)				
Input buffer	0.33 ns (fanout = 2, wiring length=2mm)				
Output buffer	1.30 ns ( $C_L = 15$ pF)				
Output drive capability	$I_{OL} = 3, 6, 9, 12, 18, 24$ mA				
Power supply voltage	5 V $\pm$ 10 % (CMOS level)				

### Notes 1. 2-input NAND conversion

2. Cell utilization rate 80 %
3. Including power supply and GND pins. The number of pins that can actually be used differs depending on the type of package.
4. Cell utilization rate 70 %

## Package list (1)

Package	Number of pins	Lead pitch (mm)	Body height (mm)	Body size (mm)
QFP (FP)	160	0.5	2.7	24 × 24
	208	0.5	3.2	28 × 28
	240	0.5	3.2	32 × 32
	304	0.5	3.7	40 × 40
TQFP	48	0.5	1.0	7 × 7
	64	0.65	1.0	12 × 12
	80	0.5	1.0	12 × 12
LQFP	44	0.8	1.4	10 × 10
	100	0.5	1.4	14 × 14
	160	0.5	1.4	24 × 24

**Remark**   FP : Fine pitch

## Package list (2)

Master name	$\mu$ PD65880	$\mu$ PD65881	$\mu$ PD65882	$\mu$ PD65883	$\mu$ PD65884
160-pin QFP (FP)	–	–	–	–	–
208-pin QFP (FP)	–	–	–	–	–
240-pin QFP (FP)	–	–	–	–	–
304-pin QFP (FP)	–	–	–	–	–
48-pin TQFP	○	○	○		–
64-pin TQFP	–	○	○	○	
80-pin TQFP	–	–	○	○	
44-pin LQFP	○	○			–
100-pin LQFP	–	–	○	○	○
160-pin LQFP	–	–	–	–	○

Master name	$\mu$ PD65885	$\mu$ PD65887	$\mu$ PD65889	$\mu$ PD65890	$\mu$ PD65893
160-pin QFP (FP)	○	○	–	–	–
208-pin QFP (FP)	○	○	○	○	○
240-pin QFP (FP)	–	○	○	○	○
304-pin QFP (FP)	–	–	–	○	○
48-pin TQFP	–	–	–	–	–
64-pin TQFP			–	–	–
80-pin TQFP			–	–	–
44-pin LQFP	–	–	–	–	–
100-pin LQFP	○	○		–	–
160-pin LQFP	–	–	○	○	

**Remark**   ○ : Released   – : Not to be supported   Blank : Under consideration   FP : Fine pitch

# Development Tools

## Easy interface with your EWS or PC

Users can choose the following tools to their environment.

**Caution** Some functions may not be supported. Make it sure before use.

### OPENCAD™ V5.4 Configuration Tool

Function	NEC Tool	Interface Data	Commercially Available Tool Interface
Function simulator	—	• Netlist PWC/EDIF(2.0.0)/	ModelSim™/Verilog-XL™/ NC-Verilog™/VCS™
Schematic editor	Vdraw™	Verilog™ HDL	—
Logic synthesis	—		Design Compiler®
Gate level simulator <sup>Note 1</sup>	V.sim™	• Test pattern ALBA	ModelSim/Verilog-XL/NC-Verilog/ VCS
Formal verifier	—		Formality®/Tuxedo™-LEC
STA <sup>Note 1</sup>	Tiara	• Delay information file	PrimeTime®
Fault simulator <sup>Note 2</sup>	C.FGRADE™		—
Design for test	TESTACT/NEC_SCAN/ NEC_BSCAN/NEC_BIST/ TESTBUS	• Constraints file	TestCompiler™/Testgen™ FastScan™/TetraMax™
Floor planner <sup>Note 3</sup>	ace_floorplan galet_floorplan		—
Placement and Routing <sup>Note 3</sup>	Galet		Gate Ensemble™ Silicon Ensemble™

**Notes 1.** Sign-off tool

2. Tool not supported in the HP™ version

3. Stand-alone tool

**Remark** Platform: SUN™(Solaris™)/HP(HP-UX™)

GUI : X11R5/Motif™ 1.2

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