NEC Electronics Inc.

CMOS-8LH 3.3-Volt, 0.5-Micron CMOS Gate Arrays

Preliminary

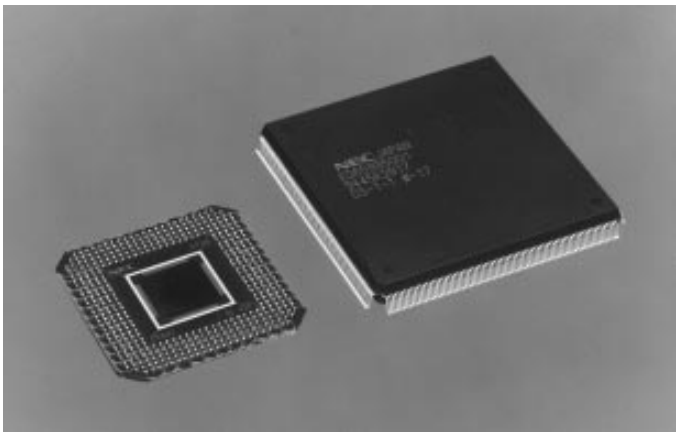
April 1996

Description

NEC's CMOS-8LH gate-array family consists of ultra-high performance, sub-micron gate arrays, targeted for applications requiring extensive integration and high speeds. With the CMOS-8LH family, NEC delivers its second generation 0.5-micron gate arrays. This family is fabricated in a high-speed, 0.5-micron, drawn gate length (Leff=0.35-micron), two- and three-level metal titanium-silicide CMOS process which provides improved performance and reduced power consumption. It features channelless (sea-of-gates) architecture with an enhanced pad layout for support of high-performance I/Os.

The CMOS-8LH family is provided with an extensive family of macros. I/O macros include GTL, HSTL, and pECL. TTL and CMOS I/Os are provided with 5-V tolerance for applications requiring interface to 5-V logic. PCI signaling standards are also supported including 3.3-V 66 MHz PCI. The technology is enhanced by a set of advanced features including phase-locked loops, clock tree synthesis, and high-speed memory. The CMOS-8LH gate-array family of 3.3-V devices consists of 22 masters, offered in densities of 31K raw gates to 329K raw gates. Usable gates range from 20K to 214K used gates in two-level metal and from 24K to 264K used gates in three-level metal.

Figure 1. CMOS-8LH Package Options: BGA & QFP



The gate-array family is supported by NEC's OpenCAD® design system, a mixture of popular third-party EDA tools, and proprietary NEC tools. NEC proprietary tools include the GALET floorplanner, which helps to reduce design time and improve design speed, and a clock tree synthesis tool that automatically builds a balanced-buffer clock tree to minimize on-chip clock skew.

Table 1. CMOS-8LH Family Features and Benefits

CMOS-8LH Family Features	CMOS-8LH Family Benefits
• Second generation 0.5-micron (drawn), 3-level metal CMOS	• Delivers up to 75 MHz system clock speed
• 24 base arrays with raw gates from 30K to 475K	• Provides base sizes to give best fit in core-limited designs
• Optimized pad pitch for low-cost packaging	• Minimizes assembly cost for popular BGA and PQFPs
• High-density, high-speed RAM compiler	• Provides high-density RAM in fast gate-array design time
• PCI, GTL, and HSTL interface buffers	• Supports popular high-speed interface standards
• Full range of 5-V-protected I/O drive strengths	• Allows interface with 5-V logic while protecting 3.3-V ASIC
• Phase-Locked Loop (DPLL) macros in development	• Eliminates clock insertion delay, reduces total clock skew
• Low power dissipation: 0.4 µW/MHz/gate	• Provides low power consumption at high system clock rates
• Extensive package offering: PQFP, BGA, PGA	• Delivers user-specific package requirements
• Clock tree synthesis tool for automated clock tree design	• Minimizes on-chip clock skew for high performance
• Floorplanner-supplied layout information for resynthesis	• Reduces design time and improves device performance
• Popular, third-party EDA tools	• Enables a smooth flow from user design to silicon
• Extra routing channel for increased utilization	• Achieves up to 80% utilization in 3-layer metal

CMOS-8LH Applications

The CMOS-8LH family is ideal for use in personal computer systems, engineering workstations, and telecommunications switching and transmission systems, where moderate integration and high speeds are primary design goals. CMOS-8LH is targeted to support applications with system speeds of 75-100 MHz. With power dissipation of 0.4 µW/MHz/gate, CMOS-8LH is also suited for lower-power applications where high performance is required.

Circuit Architecture

As shown in Figure 2, CMOS-8LH devices are divided into I/O and internal cell regions. The I/O region contains input and output buffers. The internal cell area is an array of basic cells, each composed of two p-channel MOS transistors and two n-channel transistors, as well as four additional small n-channel MOS transistors for compact RAM design. These p-channel and n-channel transistors are sized to offer a superb ratio of speed to silicon area. The four additional small RAM transistors, when not being used for RAM, provide additional area for signal routing, thus allowing exceptionally high utilization rates for a channelless architecture.

The I/O region consists of a single line of pads. The I/O buffer design allows all PCI, GTL, and HSTL class 1 buffers to fit into a single I/O slot. This layout also enhances support for low-cost PBGA and wire-bonded PQFP assembly techniques.

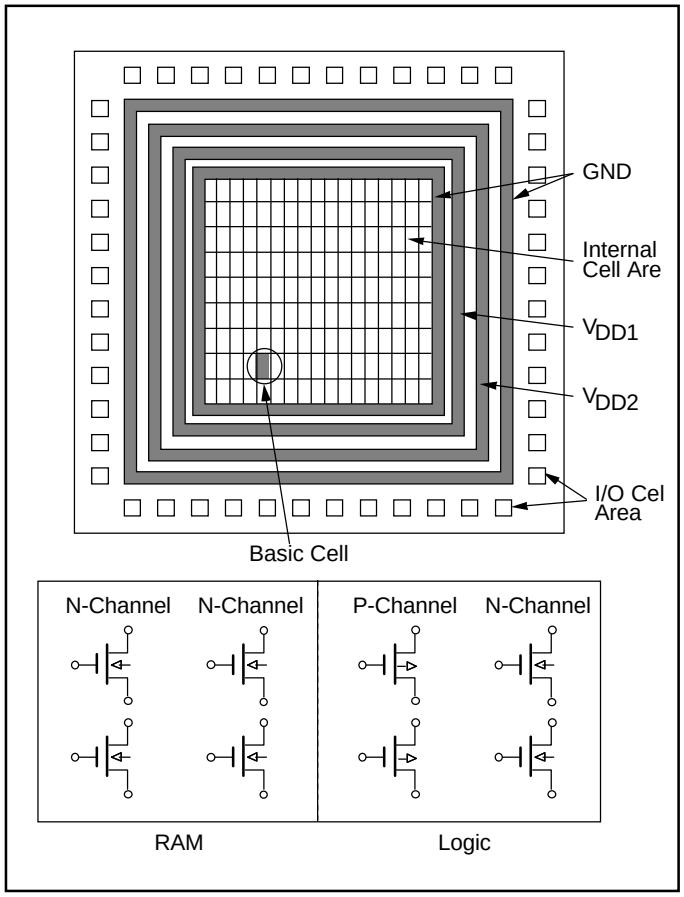
Table 2. CMOS-8LH Base Array Line-up

Device[1] (µPD663xx)		Available	Used Gates[2]		Max
2LM	3LM	Gates	2LM	3LM	Pads
42	62	30528	19843	24422	164
43	63	40992	26644	32794	188
45	65	51136	33238	40909	212
46	66	72576	47174	58061	236
48	68	83520	54288	66816	268
49	69	110400	71760	88320	308
50	70	120960	78624	96768	324
51	71	145360	94484	116288	356
52	72	204544	132953	163635	412
53	73	252928	164403	202342	468
55	75	329392	214104	263514	532

[1]2LM represents two-layer metal; 3LM represents three-layer metal.

[2]Actual gate utilization varies depending on circuit implementation. Based on utilization rate of 65% for 2LM and 80% for 3LM.

Figure 2. CMOS-8LH Layout and Cell Configuration



Power Rail Architecture

CMOS-8LH provides additional flexibility for mixed voltage system designs. As shown in Figure 2, the arrays contain two power rails: a 3.3-V rail and V_{DD2}. The V_{DD2} rail is used for interfaces such as 5-V PCI buffers where a clamping diode allows protection for up to an 11-V voltage spike, per the PCI revision 2.1 specification.

Packaging and Test

NEC utilizes BIST test structures for RAM testing. NEC also offers advanced packaging solutions including Plastic Ball Grid Arrays (PBGA), Plastic Quad Flat Packs (PQFP), and Pin Grid Arrays (PGA). Please call your local NEC ASIC design center representative for a listing of available master/package combinations.

Absolute Maximum Ratings

Power supply voltage, V_{DD}	–0.5 to +4.6-V
Input voltage, V_I	
3.3-V input buffer (at $V_I < V_{DD}$+ 0.5-V)	–0.5 to +4.6-V
3.3-V fail-safe input buffer (at $V_I < V_{DD}$+ 0.5-V)	–0.5 to +4.6-V
5-V-tolerant (at $V_I < V_{DD}$+ 3.0-V)	–0.5 to +4.6-V
Output Voltage, V_O	
3.3-V output buffer (at $V_O < V_{DD}$+ 0.5-V)	–0.5 to +4.6-V
5-V-tolerant output buffer (at $V_O < V_{DD}$+ 3.0-V)	–0.5 to +4.6-V
5-V open-drain output buffer (at $V_O < V_{DD}$+ 3.0-V)	–0.5 to +4.6-V
Latch-up current, I_{LATCH}	>1 A (typ)
Operating temperature, T_{OPT}	–40 to +85°C
Storage temperature, T_{STG}	–65 to +150°C

Input/Output Capacitance

$V_{DD} = V_I = 0$-V; f = 1 MHz

Terminal	Symbol	Typ	Max	Unit
Input	C_{IN}	10	20	pF
Output	C_{OUT}	10	20	pF
I/O	$C_{I/O}$	10	20	pF

(1) Values include package pin capacitance

Power Consumption

Description	Limits	Unit
Internal gate(1)	0.21	µW/MHz
Input buffer	2.546	µW/MHz
Output buffer	10.60	µW/MHz

(1) Assumes 30% internal gate switching at one time

Caution: Exposure to absolute maximum ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should not be operated outside the recommended operating conditions.

Recommended Operating Conditions

V_{DD} = 3.3-V ±0.3-V; T_j = –40 to +125°C

		3.3-V Interface Block		5-V Interface Block		5-V PCI Level		3.3-V PCI Level		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
I/O power supply voltage	V_{DD}	3.0	3.6	3.0	3.6	3.0	5.5	3.0	3.6	V
Junction temperature	T_J	0	+100	0	+100	0	+100	0	+100	°C
High-level input voltage	V_{IH}	2.0	V_{DD}	2.0	5.5	2.0	V_{CC}	0.5 V_{CC}	V_{CC}	V
Low-level input voltage	V_{IL}	0	0.8	0	0.8	0	0.8	0	0.3 V_{CC}	V
Positive trigger voltage	V_P	1.50	2.70	1.50	2.70	—	—	—	—	V
Negative trigger voltage	V_N	0.60	1.6	0.60	1.6	—	—	—	—	V
Hysteresis voltage	V_H	1.10	1.3	1.10	1.3	—	—	—	—	V
Input rise/fall time	t_R, t_F	0	200	0	200	0	200	0	200	ns
Input rise/fall time, Schmitt	t_R, t_F	0	10	0	10	—	—	—	—	ns

AC Characteristics

V_{DD} = 3.3-V ±0.3-V; T_j = –40 to +125°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Toggle frequency (F611)	f_{TOG}			477	MHz	D-F/F; F/O = 1; L = 0 mm
Delay time						
2-input NAND (L302)	t_{PD}		104		ps	F/O = 1; L = 0 mm
(F302)	t_{PD}		120		ps	F/O = 2; L = typ = 0.6 mm
Flip-flop (L611)	t_{PD}		457		ps	F/O = 1; L = 0 mm
	t_{PD}		579		ps	F/O = 2; L = typ
	t_{SETUP}		510		ps	—
	t_{HOLD}		430		ps	—
Input buffer (FI01)	t_{PD}		200		ps	F/O = 1; L = 0 mm
	t_{PD}		249		ps	F/O = 2; L = typ
Output buffer (9 mA) 3.3-V	t_{PD}		1.16		ns	C_L = 15 pF
Output buffer (9 mA) 5-V-tolerant	t_{PD}		1.428		ns	C_L = 15 pF
Output buffer (9 mA) 5-V-swing	t_{PD}		1.577		ns	C_L = 15 pF
Output rise time (9 mA)	t_R		1.47		ns	C_L = 15 pF
Output fall time (9 mA)	t_F		1.08		ns	C_L = 15 pF

DC Characteristics

V_{DD} = 3.3-V ±0.3-V; T_j = –40 to +125°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Quiescent current (1)						
µPD66358, 66378	I_{DDS}		2.0	300	µA	$V_I = V_{DD}$ or GND
µPD66355, 66353, 66352, 66375, 66373, 66372	I_{DDS}		1.0	300	µA	$V_I = V_{DD}$ or GND
Remaining masters	I_{DDS}		0.5	200	µA	$V_I = V_{DD}$ or GND
Off-state output leakage current						
3.3-V buffers, 3.3-V PCI	I_{OZ}			±10	µA	$V_O = V_{DD}$ or GND
5-V-tolerant buffers, 5-V PCI	I_{OZ}			±14	µA	$V_O = V_{DD}$ or GND
5-V CMOS	I_{OZ}			±14	µA	$V_O = V_{DD}$ or GND
Output short circuit current (3)	I_{OS}			–250	mA	V_O = GND
Input leakage current (2)						
5-V PCI	I_{IH}			+70, –70	µA	V_{IN} = 2.7-V, 0.5-V
3.3-V PCI	I_I			±10	µA	$V_{IN} = V_{DD}$ or GND
Regular	I_I		$±10^{-5}$	±10	µA	$V_I = V_{DD}$ or GND
50 kΩ pull-up	I_I	–180	–100	–40	µA	V_I = GND
5 kΩ pull-up	I_I	–1400	–850	–350	mA	V_I = GND
50 kΩ pull-down	I_I	30	80	160	µA	$V_I = V_{DD}$
Resistor values						
50 kΩ pull-up (6)	R_{pu}	20	33	75	kΩ	
5 kΩ pull-up	R_{pu}	2.6	3.9	8.6	kΩ	
50 kΩ pull-down (6)	R_{pu}	22.5	41.3	100	kΩ	
Input clamp voltage	V_{IC}	–1.2			V	I_I = 18 mA
Low-level output current (ALL buffer types)						
3 mA	I_{OL}	3			mA	V_{OL} = 0.4-V
6 mA	I_{OL}	6			mA	V_{OL} = 0.4-V
9 mA	I_{OL}	9			mA	V_{OL} = 0.4-V
12 mA	I_{OL}	12			mA	V_{OL} = 0.4-V
18 mA	I_{OL}	18			mA	V_{OL} = 0.4-V
24 mA	I_{OL}	24			mA	V_{OL} = 0.4-V
High-level output current (5-V-tolerant block)						
3 mA	I_{OH}	–3			mA	$V_{OH} = V_{DD}$ –0.4-V
6 mA	I_{OH}	–3			mA	$V_{OH} = V_{DD}$ –0.4-V
9 mA	I_{OH}	–3			mA	$V_{OH} = V_{DD}$ –0.4-V
12 mA	I_{OH}	–3			mA	$V_{OH} = V_{DD}$ –0.4-V
18 mA	I_{OH}	–4			mA	$V_{OH} = V_{DD}$ –0.4-V
24 mA	I_{OH}	–4			mA	$V_{OH} = V_{DD}$ –0.4-V
High-level output current (3.3-V interface block)						
3 mA	I_{OH}	–3			mA	$V_{OH} = V_{DD}$ –0.4-V
6 mA	I_{OH}	–6			mA	$V_{OH} = V_{DD}$ –0.4-V
9 mA	I_{OH}	–9			mA	$V_{OH} = V_{DD}$ –0.4-V
12 mA	I_{OH}	–12			mA	$V_{OH} = V_{DD}$ –0.4-V
18 mA	I_{OH}	–18			mA	$V_{OH} = V_{DD}$ –0.4-V
24 mA	I_{OH}	–24			mA	$V_{OH} = V_{DD}$ –0.4-V
Output voltage (5-V PCI)						
High-level output voltage	V_{OH}	2.4			mA	I_{OH} = 2 mA
Low-level output voltage	V_{OL}			0.55	mA	I_{OL} = 3 mA, 6 mA
Output voltage (3.3-V PCI)						
High-level output voltage	V_{OH}	0.9 V_{DD}			mA	I_{OH} = 500 µA
Low-level output voltage	V_{OL}			0.1 V_{DD}	mA	I_{OL} = 1500 µA
Low-level output voltage	V_{OL}			0.1	V	I_{OL} = 0 mA
High-level output voltage, 5-V TTL	V_{OH}	V_{DD}–0.2			V	I_{OL} = 0 mA
High-level output voltage, 3.3-V	V_{OH}	V_{DD}–0.1			V	I_{OH} = 0 mA

Notes:

(1) Static current consumption increases if an I/O block with on-chip pull-up/pull-down resistor or an oscillator is used. Call an NEC ASIC design center representative for assistance in calculation.

(2) Leakage current is limited by tester capabilities. Specification listed represents this measurement limitation. Actual values will be significantly lower.

(3) Rating is for only one output operating in this mode for less than 1 second.

(4) Normal type buffer: $I_{OH} < I_{OL}$.

(5) Balanced buffer: $I_{OH} = I_{OL}$.

(6) Resistor is called 50ký to maintain consistency with previous families.

Publications

This data sheet contains preliminary specifications for the CMOS-8LH gate-array family. Additional information will be available in NEC's *CMOS-8LH Block Library* and *CMOS-8LH Design Manual*. Call your local NEC ASIC design center representative or the NEC literature line for additional ASIC design information; see the back of this data sheet for locations and phone numbers.

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  Houston, TX 77070

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Document No. A11169EU1V0DS00