NEC Electronics Inc.

CMOS-9
3.3-VOLT, 0.35-MICRON CMOS GATE ARRAYS

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Description

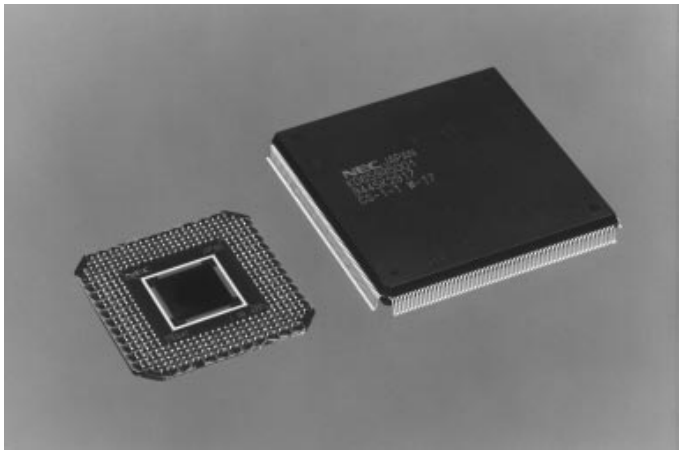
NEC's CMOS-9 gate array family provides designers with the performance capabilities and features required to develop devices for high-speed computer and communications systems. NEC combines the highest performance 0.35-micron drawn gate length (Leff=0.27 micron) 2- and 3-level metal CMOS technology with an extensive family of interface macros to support very high-speed system clocks. The high performance I/O macros including GTL, HSTL, and pECL are under development. PCI signaling standards are also supported including 3.3V 66 MHz PCI.

This technology is enhanced by a set of advanced features including phase-locked loops, clock tree synthesis, and high-speed memory.

The CMOS-9 gate array family of 3.3-volt devices consists of 20 masters, offered in densities of 190K raw gates to 2 million raw gates. Usable gates range from 76K to 1.2 million used gates.

The gate array family is supported by NEC's OpenCAD® design system; a mixture of popular third-party CAE tools, and proprietary NEC tools. NEC proprietary tools include the GALET floorplanner which helps reduce design cycle time and improve design performance, clock tree synthesis for clock skew minimization, and table look-up delay calculator for accurate delay calculation.

Figure 1. CMOS-9 Package Examples; BGA and QFP



CMOS-9 Applications

The CMOS-9 family is ideal for use in enterprise systems, engineering workstations, telecommunications switching and transmission systems, where extensive integration and high speeds are primary design goals. CMOS-9 is well-suited for designs requiring very high integration (300K-600K gates, 400-600 pins), high system speeds (100-200 MHz), and high performance interface standards (HSTL, GTL). CMOS-9 is also well-suited for lower power applications where high performance is required. CMOS-9 is offered now at 3.3V and will be released at 2.5V in the future.

Table 1. CMOS-9 Series Features and Benefits

CMOS-9 Series Features	CMOS-9 Series Benefits
• 0.35-micron (drawn), 2 and 3-level metal CMOS technology	• Delivers dense cell structure and high speed
• Eighteen base arrays with raw gates from 190K to 1.5M	• Provides many base sizes to give best fit to design needs
• Narrow pad pitch for maximum gate to pad ratio	• Minimizes device cost
• Pad counts from 300 to 1060 pads	• Supports high I/O integration and wide system bus widths
• GTL, GTL+, pECL, and all four classes of HSTL	• Interfaces to high speed memory and processor buses
• Full range of 5V-protected I/O buffers	• Allows interface with 5V logic while protecting 3.3V ASIC
• PCI buffers including 3.3V 66 MHz PCI buffer	• Supports signaling methods defined in PCI Spec 2.1
• Phase-Locked Loop (DPLL) macros in development	• Eliminates clock insertion delay, reduces total clock skew
• Low power dissipation: 0.9 µW/MHz/gate	• Provides low power consumption at high system clock rates
• Extensive package offering: PQFP, TQFP, BGA, TAB	• Delivers customer-specific package requirements
• Clock Tree Synthesis tool automates clock tree design	• Minimizes on-chip clock skew for high performance
• Floorplanner supplies layout information for resynthesis	• Reduces design time and improves device performance
• Popular, third-party CAE tools supported	• Enables a smooth flow from customer design to silicon

Array Architecture

The CMOS-9 gate array family is built with NEC's 0.35-micron (drawn) channelless array architecture. As shown in Figure 2, the array is divided into I/O and core regions. The I/O region contains input and output buffers. The core region contains the sea-of-gates array.

The CMOS-9 gate arrays architecture provides extra flexibility for high performance system designs. As shown in Figure 2, the arrays contain two power rails: a 3.3V rail, and a second power rail (V_{DD2}) for special I/O types.

The V_{DD2} rail is used for interfaces such as HSTL where a very low I/O power supply is required (1.4 to 1.6V). All four classes of HSTL buffer are supported.

The V_{DD2} rail may be separated into sections to allow one device to support two or more busses requiring special I/O voltages. Examples of spread I/O cells that may use this V_{DD} rail are HSTL and 5V PCI. Each section can operate as an independent voltage zone, and sections can be linked together to form common voltage zones.

Core Architecture

The core region consists of an array of gates. Each gate contains 2 n-channel and 2 p-channel MOS logic transistors. One core gate is equivalent to one 2-input NAND gate (L302). The logic transistors are sized to offer a superior ratio of speed to silicon area.

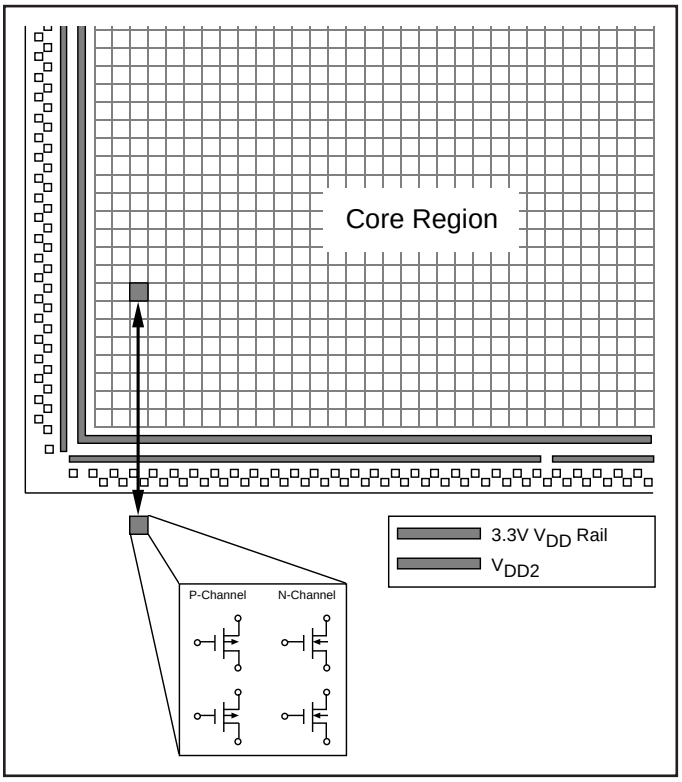
Table 2. CMOS-9 Base Array Line-up

Device[1] (μPD659xx) 2LM	3LM	Available Gates	Usable Gates[2] 2LM	3LM	Max Pads Regular Pitch	Tight Pitch
06	26	190152	76061	114091	300	388
07	27	249948	99979	149969	340	444
08	28	317904	127162	190742	380	500
09	29	376740	150696	226044	412	540
10	30	462088	184835	277253	452	596
11	31	629824	251930	377894	524	692
13	33	805580	322232	483348	588	772
15	35	1076032	430413	645619	676	892
17	37	1545240	618096	927144	804	1060

(1) 2LM represents two-layer metal; 3LM represents three-layer metal.

(2) Actual gate utilization varies depending on circuit implementation. Utilization is 40% for 2LM; 60% for 3LM.

Figure 2. CMOS-9 Power Rail Structure



Packaging and Test

CMOS-9 gate arrays support automatic test generation through a scan-test methodology, which allows higher fault coverage, easier testing and quicker development time. NEC also offers optional BIST test structures for RAM testing.

NEC offers advanced packaging solutions including Ball Grid Arrays (BGA), Plastic Quad Flat Packs (PQFP), Low Profile Plastic Quad Flat Packs (LQFP), Thin Plastic Quad Flat Packs (TQFP), Pin Grid Arrays (PGA) and advanced TAB technology.

Please contact your local NEC ASIC Design Center for a listing of available master/package combinations.

Publications

This data sheet contains preliminary specifications, package information, and operational data for the CMOS-9 gate array family. Additional design information will be available in NEC's CMOS-9 Block Library and CMOS-9 Design Manual.

Contact your local NEC ASIC Design Center or the NEC Literature Center for further ASIC design information; see the back of this data sheet for locations and phone numbers.

Absolute Maximum Ratings

Power supply voltage, V_{DD}	–0.5 to +4.6 V
Input voltage, V_I	
3V Input buffer (at $V_I < V_{DD} + 0.5V$)	-0.5 to 4.6 V
3V Fail-safe input buffer (at $V_I < V_{DD} + 0.5V$)	-0.5 to 4.6 V
5V Input buffer (at $V_I < V_{DD} + 0.5V$)	-0.5 to 6.6 V
Output voltage, V_O	
3V Output buffer (at $V_O < V_{DD} + 0.5V$)	-0.5 to 4.6 V
5V TTL Output buffer (at $V_O < V_{DD} + 3.0V$)	-0.5 to 6.6 V
5V CMOS Output buffer (at $V_O < V_{DD} + 3.0V$)	-0.5 to 6.6 V
Latch-up current, I_{LATCH}	>1 A (typ)
Operating temperature, T_{OPT}	-40 to +85°C
Storage temperature, T_{STG}	-65 to +150°C

Input/Output Capacitance

$V_{DD} = V_I = 0$ V; f = 1 MHz

Terminal		Symbol	Mln	Typ	Max	Unit
Input	3V	C_{IN}	4.0		6.0	pF
	5V		8.0		10.0	
Output	3V	C_{OUT}	4.0		6.0	pF
	5V		8.0		10.0	
I/O	3V	$C_{I/O}$	4.0		6.0	pF
	5V		8.0		10.0	

1) Values include package pin capacitance.

Power Consumption

Description	Limits	Unit
Internal gate	1.09	µW/MHz
Input buffer (FI01)	15.05	µW/MHz
Output buffer (FO01 @ 15 pF)	234	µW/MHz

Caution: Exposure to absolute maximum ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should not be operated outside the recommended operating conditions.

Recommended Operating Conditions

Parameter	Symbol	3.3V Interface Block		5V Interface Block		5V PCI Level		3.3V PCI Level		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
I/O Power supply voltage	V_{DD}	3.0	3.6	3.0	3.6	3.0	3.6	3.0	3.6	V
Junction temperature	T_J	-40	+125	-40	+125	-40	+125	-40	+125	°C
High-level input voltage	V_{IH}	2.0	V_{DD}	2.0	5.5	2.0	V_{CC}	$0.5V_{CC}$	V_{CC}	V
Low-level input voltage	V_{IL}	0	0.8	0	0.8	0	0.8	0	$0.3V_{CC}$	V
Positive trigger voltage	V_P	1.5	2.7	2.2	2.55	—	—	—	—	V
Negative trigger voltage	V_N	0.6	1.4	0.84	1.01	—	—	—	—	V
Hysteresis voltage	V_H	1.1	1.5	1.36	1.54	—	—	—	—	V
Input rise/fall time	t_R, t_F	0	200	0	200	0	200	0	200	ns
Input rise/fall time, Schmitt	t_R, t_F	0	10	0	10	—	—	—	—	ns

AC Characteristics

$V_{DD} = 3.3V \pm 0.3V$; $T_j = -40$ to +125°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Toggle frequency (D-flip-flop)	f_{TOG}			670	MHz	F/O = 2, 5V
Delay time, 2-input NAND gate @ 5V						
Standard gate (F302)	t_{PD}		99		ps	F/O = 1; L = 0 mm
			150		ps	F/O = 2; L = 0.5 mm
Power gate (F322)	t_{PD}		84		ps	F/O = 1; L = 0 mm
			119		ps	F/O = 2; L = 0.5 mm
Delay time, buffer						
Input buffer (FI01)	t_{PD}		188		ps	F/O = 1; L = 0.5 mm
Input buffer (FI01)	t_{PD}		216		ps	F/O = 2; L = 0 mm
Output buffer (FO01)	t_{PD}		1.40		ns	C_L = 15 pF
Output rise time (FO01)	t_R		2.35		ns	C_L = 15 pF
Output fall time (FO01)	t_F		1.83		ns	C_L = 15 pF

DC Characteristics

V_{DD} = 3.3V ± 0.3V; T_j = -40 to +125°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Quiescent current (µPD659xx) (1)						
-19, -39	I_L		7	1400	µA	$V_I = V_{DD}$ or GND
-17, -37, -15, -35, -13, -33, -11, -31	I_L		4	800	µA	$V_I = V_{DD}$ or GND
-10, -30, -09, -29, -08, -28	I_L		2	400	µA	$V_I = V_{DD}$ or GND
-06, -26, -07, -27	I_L		1	200	µA	$V_I = V_{DD}$ or GND
Off-state output leakage current						
3V output buffer	I_{OZ}			±10	µA	$V_O = V_{DD}$ or GND
5V-protected TTL buffer	I_{OZ}			±10	µA	$V_O = V_{DD}$ or GND
Output short circuit current (3)	I_{OS}			-250	mA	V_O = GND
Input leakage current (2)						
Regular	I_I		$\pm 10^{-4}$	±10	µA	$V_I = V_{DD}$ or GND
50 kΩ pull-up	I_I	36	89	165	µA	V_I = GND
5 kΩ pull-up	I_I	284	654	1305	µA	V_I = GND
50 kΩ pull-down	I_I	28	79	141	µA	$V_I = V_{DD}$
Resistor values						
50 kΩ pull-up (4)	R_{pu}	21.8	37.1	83.1	kΩ	
5 kΩ pull-up	R_{pu}	2.8	5.0	10.6	kΩ	
50 kΩ pull-down	R_{pu}	25.6	41.9	105.8	kΩ	
Low-level output current (5V Interface block)						
1 mA	I_{OL}	1			mA	V_{OL} = 0.4 V
2 mA	I_{OL}	2			mA	V_{OL} = 0.4 V
3 mA	I_{OL}	3			mA	V_{OL} = 0.4 V
6 mA	I_{OL}	6			mA	V_{OL} = 0.4 V
9 mA	I_{OL}	9			mA	V_{OL} = 0.4 V
12 mA	I_{OL}	12			mA	V_{OL} = 0.4 V
High-level output current (5V Interface block)						
1 mA	I_{OH}	–1			mA	V_{OH} = 2.4 V
2 mA	I_{OH}	–1			mA	V_{OH} = 2.4 V
3 mA	I_{OH}	–3			mA	V_{OH} = 2.4 V
6 mA	I_{OH}	–3			mA	V_{OH} = 2.4 V
9 mA	I_{OH}	–3			mA	V_{OH} = 2.4 V
12 mA	I_{OH}	–3			mA	V_{OH} = 2.4 V
Low-level output current (3.3V Interface block)						
3 mA (FO09)	I_{OL}	3			mA	V_{OL} = 0.4 V
6 mA (FO04)	I_{OL}	6			mA	V_{OL} = 0.4 V
9 mA (FO01)	I_{OL}	9			mA	V_{OL} = 0.4 V
12 mA (FO02)	I_{OL}	12			mA	V_{OL} = 0.4 V
18 mA (FO03)	I_{OL}	18			mA	V_{OL} = 0.4 V
24 mA (FO06)	I_{OL}	24			mA	V_{OL} = 0.4 V
High-level output current (3.3V Interface block)						
3 mA (FO09)	I_{OH}	-3			mA	V_{OH} = 2.4 V
6 mA (FO04)	I_{OH}	-6			mA	V_{OH} = 2.4 V
9 mA (FO01)	I_{OH}	-9			mA	V_{OH} = 2.4 V
12 mA (FO02)	I_{OH}	-12			mA	V_{OH} = 2.4 V
18 mA (FO03)	I_{OH}	-18			mA	V_{OH} = 2.4 V
24 mA (FO06)	I_{OH}	-24			mA	V_{OH} = 2.4 V
Low-level output voltage	V_{OL}			0.1	V	I_{OL} = 0 mA
High-level output voltage	V_{OH}	V_{DD}-0.1			V	I_{OH} = 0 mA

Notes:

(1) Static current consumption increases if an I/O block with on-chip pull-up/pull-down resistor or an oscillator is used. Contact an NEC ASIC Design Center for assistance in calculation.

(2) Leakage current is limited by tester capabilities. Specification listed represents this measurement limitation. Actual values will be significantly lower.

(3) Rating is for only one output operating in this mode for less than 1 second.

(4) Resistor is called 50kΩ for backwards compatibility.

CAD Support

The CMOS-9 family is fully supported by NEC's sophisticated OpenCAD design framework, CMOS-9 maximizes design quality and flexibility while minimizing ASIC design time.

NEC's OpenCAD system allows designers to combine the EDA industry's most popular third-party design tools with proprietary NEC tools, including those for advanced floorplanner, clock tree synthesis, automatic test pattern generation (ATPG), full-timing simulation, accelerated fault grading and advanced place and route algorithms. The latest OpenCAD system is open for sign-off using standard EDA tools. NEC offers RTL- and STA- (Static Timing Analysis) sign-off procedures to shorten the ASIC design cycle of high-complexity designs.

Support of High-Speed Systems. High-speed systems require tight control of clock skew on the chip and between devices on a printed circuit board. CMOS-9 provides three features to control clock skew: the standard Digital PLL (DPLL) working at frequencies up to 100 MHz for chip-to-chip skew minimization, the multiplying digital PLL providing frequencies up to 200 MHz, and Clock Tree Synthesis (CTS). CTS — supported by an NEC proprietary design tool — is used for clock skew management through the automatic insertion of a balanced buffer tree. The clock tree insertion method minimizes large-capacitive trunks and is especially useful with the hierarchical, synthesized design style being used for high-integration devices. RC values for actual net lengths of the clock tree are used for back annotation after place and route operations. A skew as low as ±100 ps can be achieved.

Accurate Design Verification. Nonlinear timing calculation is a very important requirement of the high-density, deep sub-micron ASIC designs. NEC makes use of the increased accuracy delivered by the nonlinear table look-up delay calculation methodology and offers consistent wire load models to ensure a high accuracy of the design verification.

Design Rule Check. A comprehensive design rule check (DRC) program reports design rule violations as well as chip utilization statistics for the design netlist. The generated report contains such information as net counts, total pin and gate counts, and utilization figures.

Layout. During design synthesis, wire load models are used to get delay estimations in a very early state of the design flow. In general, there's no need for customers to perform the floorplanning to meet the required timing. During layout, enhanced in-place optimization (IPO) features of the layout tools and engineering change order (ECO) capabilities of the synthesis tools are used to optimize critical timing paths defined by the given timing constraints. This feature can reduce the total design time.

Test Support

The CMOS-9 family supports automatic test generation through a scan test methodology. It includes internal scan, boundary scan (JTAG) and built-in-self-test (BIST) architecture for easy and high-performance production RAM testing. This allows higher fault coverage, easier testing and faster development time.

NEC ASIC DESIGN CENTERS

WEST

- 3033 Scott Boulevard
  Santa Clara, CA 95054

  TEL 408-588-5008
  FAX 408-588-5017

- One Embassy Centre
  9020 S.W. Washington Square Road,
  Suite 400
  Tigard, OR 97223

  TEL 503-671-0177
  FAX 503-643-5911

SOUTH CENTRAL/SOUTHEAST

- Three Galleria Tower
  13155 Noel Road, Suite 1100
  Dallas, TX 75240

  TEL 972-855-5150
  FAX 972-503-3993

- Research Triangle Park
  2000 Regency Parkway, Suite 455
  Cary, NC 27511

  TEL 919-460-1890
  FAX 919-469-5926

- Two Chasewood Park
  20405 SH 249, Suite 580
  Houston, TX 77070

  TEL 713-320-0524
  FAX 713-320-0574

NORTH CENTRAL/NORTHEAST

- The Meadows, 2nd Floor
  161 Worcester Road
  Framingham, MA 01701

  TEL 508-935-2200
  FAX 508-935-2234

- Greenspoint Tower
  2800 W. Higgins Road, Suite 765
  Hoffman Estates, IL 60195

  TEL 708-519-3945
  FAX 708-882-7564

THIRD-PARTY DESIGN CENTERS

SOUTH CENTRAL/SOUTHEAST

- Koos Technical Services, Inc.
  385 Commerce Way, Suite 101
  Longwood, FL 32750

  TEL 407-260-8727
  FAX 407-260-6227

- Integrated Silicon Systems Inc.
  2222 Chapel Hill Nelson Highway
  Durham, NC 27713

  TEL 919-361-5814
  FAX 919-361-2019

- Applied Systems, Inc.
  1761 W. Hillsboro Blvd., Suite 328
  Deerfield Beach, FL 33442

  TEL 305-428-0534
  FAX 305-428-5906

NEC Electronics Inc.
CORPORATE HEADQUARTERS
2880 Scott Boulevard
P.O. Box 58062
Santa Clara, CA 95052
TEL 408-588-6000

For literature, call toll-free 7 a.m. to 6 p.m. Pacific time: **1-800-366-9782**
or FAX your request to: **1-800-729-9288**

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