

USS-820D USB Device Controller



Features

- Full compliance with the *Universal Serial Bus Specification Revision 1.1*.
- Backward compatible with USS-820B and USS-820C revisions.
- Self-powered or bus-powered USB device. Meets USB power specifications for bus-powered devices.
- Full-speed USB device (12 Mbits/s).
- USB device controller with protocol control and administration for up to 16 USB endpoints.
- Supports control, interrupt, bulk, and isochronous transfers for all 16 endpoints.
- Programmable endpoint types and FIFO sizes and internal 1120-byte logical (2240-byte physical for dual-packet mode) shared FIFO storage allow a wide variety of configurations.
- Dual-packet mode of FIFOs reduces latency.
- Supports USB remote wake-up feature.
- On-chip crystal oscillator allows external 12 MHz crystal or 3 V/5 V clock source.
- On-chip analog PLL creates 48 MHz clock from internal 12 MHz clock.
- Integrated USB transceivers.
- 5 V tolerant I/O buffers allow operation in 3 V or 5 V system environment.
- Implemented in Agere Systems Inc. 0.25 μ m, 3 V standard-cell library.
- 44-pin MQFP (USS-820D).
- 48-pin TQFP (USS-820TD).
- Evaluation kit available.

New Features After Revision B

- New, centralized FIFO status bits and interrupt output pin reduce firmware load.
- New, additional nonisochronous transmit mode allows NAK response to cause interrupt.
- Isochronous behavior enhancements simplify firmware control.
- Additional FIFO sizes for nonisochronous endpoints.
- USB reset can be programmed to clear device address.
- USB reset output status pin.
- Firmware ability to wake up and reset a suspended device.

- Lower power.
- 5 V supply no longer required for 5 V tolerant operation.

Applications

- Suitable for peripherals with embedded microprocessors.
- Glueless interface to microprocessor buses.
- Support of multifunction USB implementations, such as printer/scanner and integrated multimedia applications.
- Suitable for a broad range of device class peripherals in the USB standard.

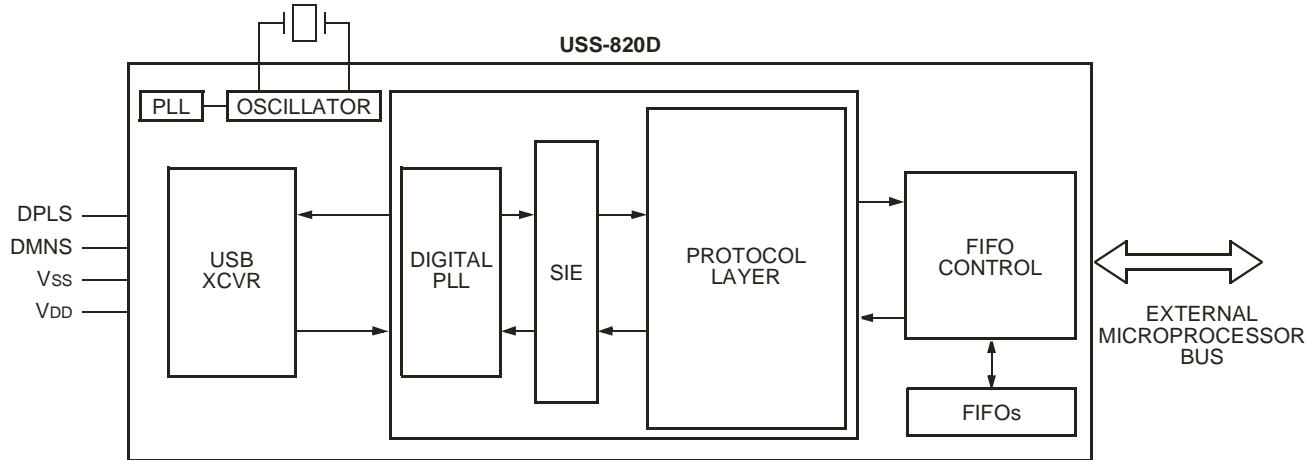
Description

USS-820D is a USB device controller that provides a programmable bridge between the USB and a local microprocessor bus. It is available in two package types: 44-pin MQFP (USS-820D) and 48-pin TQFP (USS-820TD, formerly USS-825). The USS-820D allows PC peripherals to upgrade to USB connectivity without major redesign effort. It is programmable through a simple read/write register interface that is compatible with industry-standard USB microcontrollers.

USS-820D is designed in 100% compliance with the USB industry standard, allowing device-side USB products to be reliably installed using low-cost, off-the-shelf cables and connectors.

The integrated USB transceiver supports 12 Mbits/s full-speed operation. FIFO options support all four transfer types: control, interrupt, bulk, and isochronous, as described in *Universal Serial Bus Specification Revision 1.1*, with a wide range of packet sizes. Its double sets of FIFO enable the dual-packet mode feature. The dual-packet mode feature reduces latency by allowing simultaneous transfers on the host and microprocessor sides of a given unidirectional endpoint.

Description (continued)



5-8121 (F)

Figure 1. Block Diagram

The USS-820D supports a maximum of eight bidirectional endpoints with 16 FIFOs (eight for transmit and eight for receive) associated with them. The FIFOs are on-chip, and sizes are programmable up to a total of 1120 logical bytes. When the dual-packet mode feature is enabled, the device uses a maximum of 2240 bytes of physical storage. This additional physical FIFO storage is managed by the device hardware and is transparent to the user.

The FIFO sizes supported are 8 bytes, 16 bytes, 32 bytes, and 64 bytes for nonisochronous pipes and 64 bytes, 256 bytes, 512 bytes, and 1024 bytes for isochronous pipes. The FIFO size of a given endpoint defines the upper limit to maximum packet size that the hardware can support for that endpoint. This flexibility covers a wide range of data rates, data types, and combinations of applications.

The USS-820D can be clocked either by connecting a 12 MHz crystal to the XTAL1 and XTAL2 pins, or by using a 12 MHz external oscillator. The internal 12 MHz clock period, which is a function of either of these clock sources, is referred to as the device clock period (tCLK) throughout this data sheet.

Serial Interface Engine

The SIE is the USB protocol interpreter. It serves as a communicator between the USS-820D and the host through the USB lines.

The SIE functions include the following:

- Package protocol sequencing
- SOP (start of packet), EOP (end of packet), RESUME, and RESET signal detection and generation
- NRZI data encoding/decoding and bit stuffing
- CRC generation and checking for token and data
- Serial-to-parallel and parallel-to-serial data conversion

Protocol Layer

The protocol layer manages the interface between the SIE and FIFO control blocks. It passes all USB OUT and SETUP packets through to the appropriate FIFO. It is the responsibility of firmware to correctly interpret and execute each USB SETUP command via the register interface. The protocol layer tracks the setup, data, and status stages of control transfers.

FIFO Control

USS-820D's FIFO control manager handles the data flow between the FIFOs and the device controller's protocol layer. It handles flow control and error handling/fault recovery to monitor transaction status and to relay control events via interrupt vectors.

Pin Information

Table 1. Pin Descriptions

44-Pin MQFP (USS-820D)	48-Pin TQFP (USS-820TD)	Symbol ^{*,†}	Type	Name/Description
1	2	VDDA	P	3.3 V Power Supply for Analog PLL.
2	3	XTAL1	I	Crystal/Clock Input.
3	4	XTAL2	O	Crystal/Clock Output.
4	5	VDDT	P	3.3 V Power Supply for USB Transceiver.
5	6	DMNS	I/O	USB Differential Data Bus Minus.
6	7	DPLS	I/O	USB Differential Data Bus Plus.
7	8	VSST	P	Device Ground for USB Transceiver.
12, 11, 10, 9, 8	13, 12, 11, 10, 9	A[4:0]	I	Address Bus.
13	14	VSSX	P	Device Ground.
14, 20, 21, 22, 23, 24, 34, 40	15, 22, 23, 24, 25, 26, 37, 43	VSS0, VSS1, VSS2, VSSX	P	Device Ground.
15	16	DSA	O	Data Set Available.
18	19	USBR	O	USB Reset Detected.
16	1, 17, 20, 21, 27	NC	—	No Connect.
17, 44	18, 47	VDD0, VDD1	P	3.3 V Power Supply.
19	48	DPPU	O	DPLS Pull-Up.
25	28	RWUPN	I	Remote Wake-Up (Active-Low).
26	29	SUSPN	O	Suspend (Active-Low).
27	30	IRQN	O	Interrupt (Programmable Active-Low or Active-High).
28	31	SOFN	O	Start of Frame (Active-Low).
29	32	RESET	I	Reset.
30	33	NC	—	No Connect. Can be connected to a signal or power without harm.
31	34	IOCSN	I	Chip Select (Active-Low).
32	35	WRN	I	Control Register Write (Active-Low).
33	36	RDN	I	Control Register Read (Active-Low).
35, 36, 37, 38, 39, 41, 42, 43	38, 39, 40, 41, 42, 44, 45, 46	D[7:0]	I/O	Data Bus.

* Active-low signals within this document are indicated by an N following the symbol names.

† Pins marked as NC must have no external connections, except where noted.

USS-820 ARM[®] Reference Design Kit (RDK)

Features

- An Agere USS-820D hardware evaluation platform
- *Windows*[®] graphical user interface program
- Custom USB device driver and firmware
- Sample applications

Contents

The USS-820 ARM RDK comes complete with the following:

- Agere USS-820D evaluation board
- 12 V power supply

- A-B USB cable
- 9-pin male to 9-pin female serial cable
- 25-pin to 9-pin serial cable adapter
- CD-ROM
- USS-820D chip samples
- User and hardware reference manuals
- License agreement and warranty
- Technical support sheet and order form
- Product information briefs

The USB-IF logo is a trademark of the Universal Serial Bus Implementers Forum, Inc.

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