US1881

CMOS Multi-Purpose Latch

Features and Benefits

- Chopper Stabilized Amplifier Stage
- Optimized for BDC Motor Applications
- New Miniature Package/Thin, High Reliability Package
- Operation Down to 3.5V
- CMOS for Optimum Stability, Quality and Cost

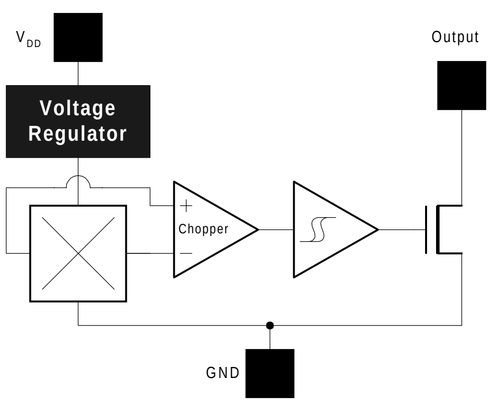
Applications

- Solid State Switch
- Brushless DC Motor Commutation
- Speed Sensing
- Linear Position Sensing
- Angular Position Sensing
- Current Sensing

Ordering Information

Part No.	*Temperature Suffix*	*Package*	*Temperature Range*
US1881	C	SO or UA	0^oC to 70^oC Commercial
US1881	S	SO or UA	-20^oC to 85^oC Industrial
US1881	E	SO or UA	-40^oC to 85^oC Extended
US1881	K	SO or UA	-40^oC to 125^oC Severe
US1881	L	SO or UA	-40^oC to 150^oC Full Temp.
MLX1881	L	SO or UA	-40^oC to 150^oC Automotive

Functional Diagram



UA Package
Pin 1 - V_{DD}
Pin 2 - GND
Pin 3 - Output

SO Package
Pin 1 - V_{DD}
Pin 2 - Output
Pin 3 - GND

Note: *Static sensitive device, please observe ESD precautions. Reverse V_{DD} protection is not included. For reverse voltage protection, a 100Ω resistor in series with V_{DD} is recommended.*

Description

The US1881 is the industry's first Hall integrated circuit in a SOT-23 package. The above table of part numbers provide six selections of Hall effect device (HED) sensor ICs, in two package styles, based on guaranteed temperature specifications.

The temperature ranges are defined by room temperature (25°C) test guardbands and are not 100% tested at either temperature extreme. Special testing is available as in the case of the MLX series. Contact the Melexis marketing office with any questions. Though there are many other applications for this HED, the design, specifications and performance have been optimized for commutation applications in 5V and 12V brushless DC motors.

The output transistor will be "latched on" (B_{OP}) in the presence of a sufficiently strong South pole magnetic field facing the marked side of the package. Similarly, the output will be "latched off" (B_{RP}) in the presence of a North field.

The SOT-23 device is reversed from the UA package. The SOT-23 output transistor will be "latched on" (B_{OP}) in the presence of a sufficiently strong North pole magnetic field subjected to the marked face.

US1881 Electrical Specifications

DC Operating Parameters T_A = 25°C, V_{DD} = 12V (unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Voltage	V_{DD}	Operating	3.5		20	V
Supply Current	I_{DD}	$B<B_{OP}$	1.5	**2.5**	4.0	mA
Saturation Voltage	$V_{DS(on)}$	I_{OUT} = 20 mA, $B>B_{OP}$		**0.4**	0.5	V
Output Leakage	I_{OFF}	$B<B_{RP}$, V_{OUT} = 20V		**0.01**	5.0	µA
Output Rise Time	t_r	V_{DD} = 12V, R_L = 1.1KΩ, C_L = 20pf		**0.04**		µs
Output Fall Time	t_f	V_{DD} = 12V, R_L = 1.1KΩ, C_L = 20pf		**0.18**		µs

US1881 Magnetic Specifications

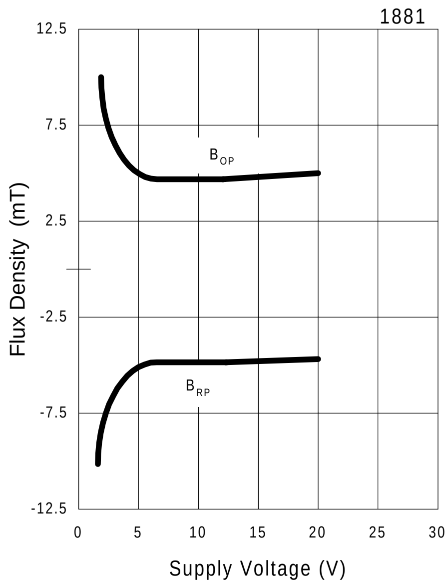
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Operating Point	B_{OP}		1.0	**5.0**	9.0	mT
Release Point	B_{RP}		-9.0	**-5.0**	-1.0	mT
Hysteresis	B_{hys}		7.0	**10.0**	12.0	mT

Notes: *1mT=10Gauss*

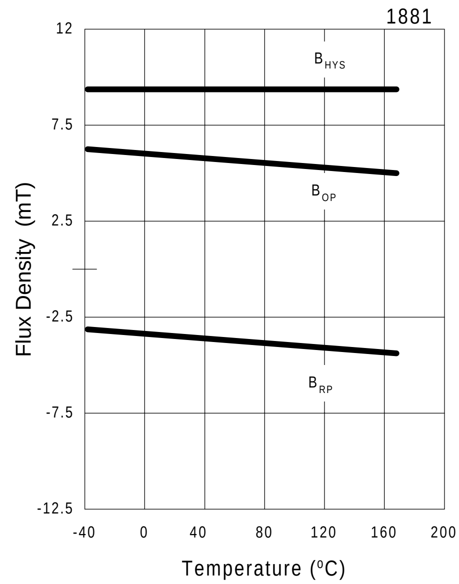
The SOT-23 device is reversed from the UA package. The SOT-23 output transistor will be "latched on" (B_{OP}) in the presence of a sufficiently strong North pole magnetic field subjected to the marked face.

Performance Graphs

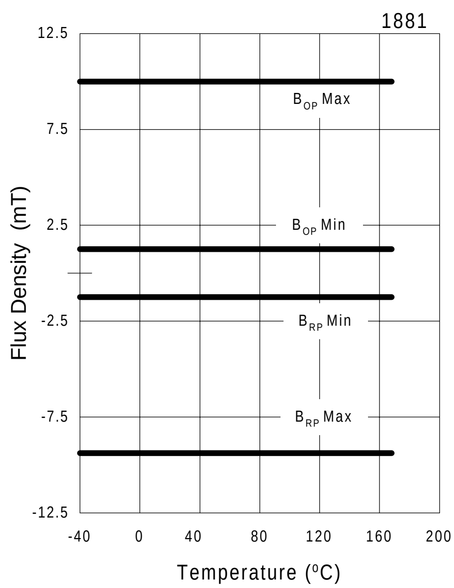
Typical Magnetic Switch Points versus Supply Voltage



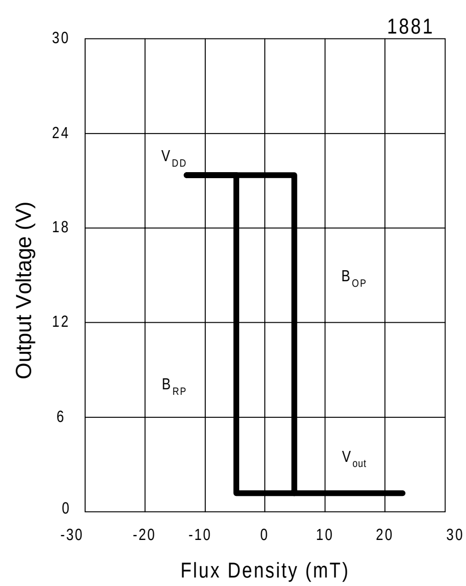
Typical Magnetic Switch Points versus Temperature



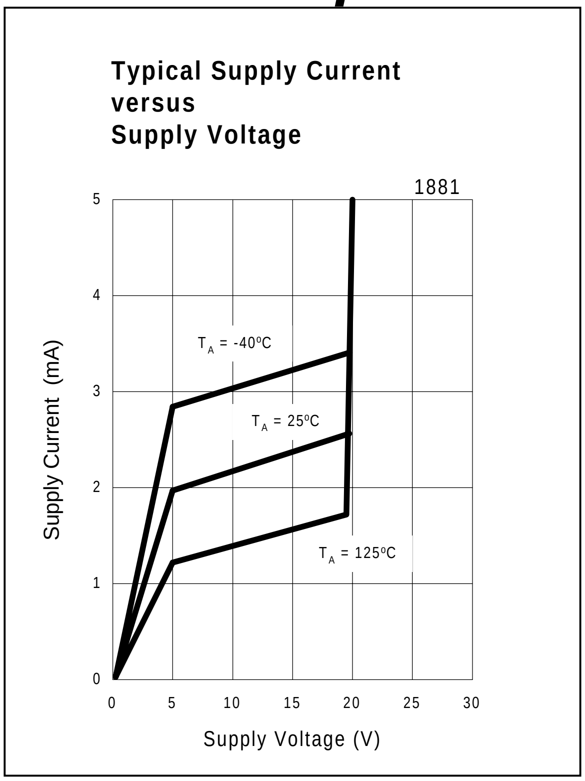
Min/Max Magnetic Switch Range versus Temperature

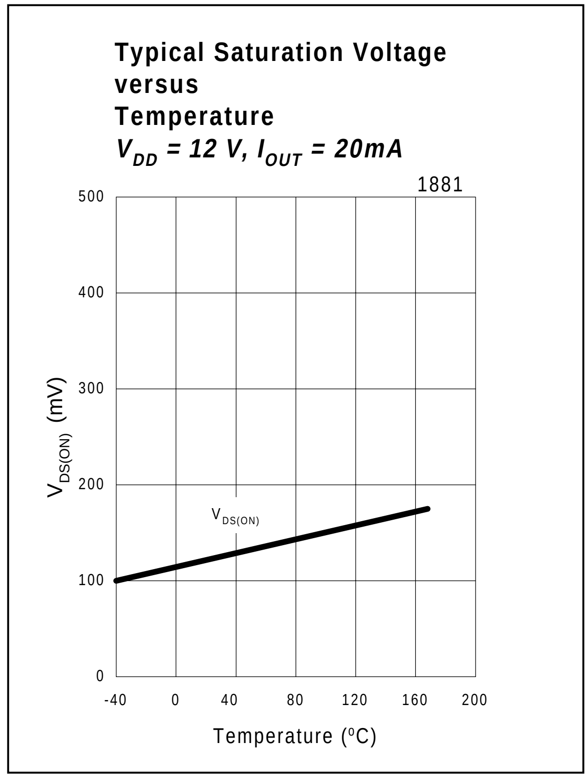


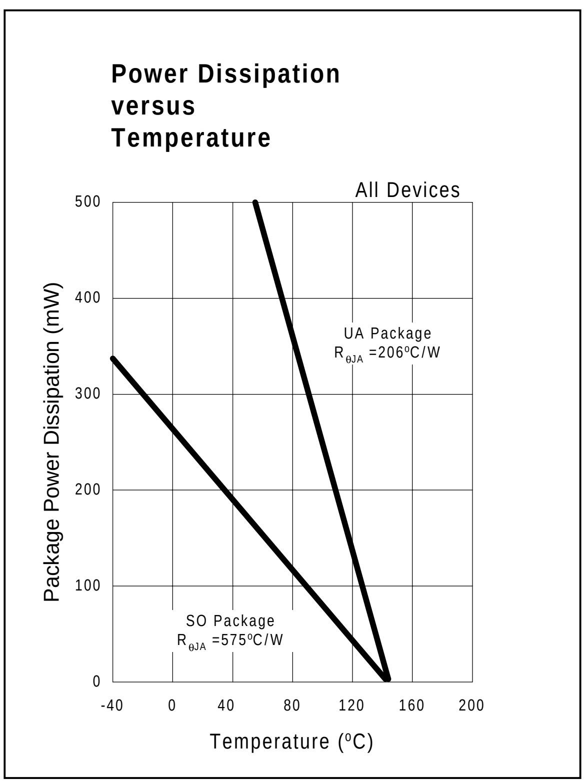
Output Voltage versus Flux Density

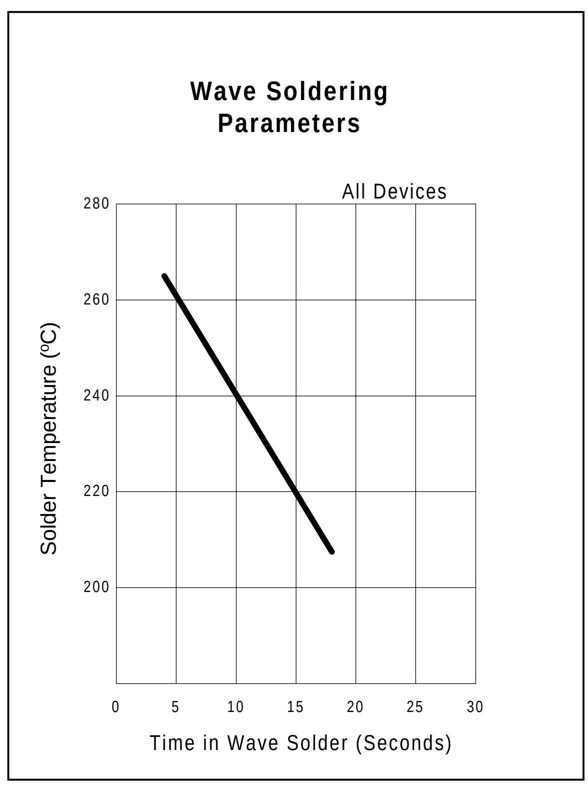


Performance Graphs









Unique Features

CMOS Hall IC Technology

The Chopper Stabilized Amplifier, using switched capacitor techniques, eliminates the amplifier offset voltage, which in bipolar devices is a major source of temperature sensitive drift. CMOS makes this advanced technique possible.
The CMOS chip is also much smaller than the Bipolar chip, allowing very sophisticated circuitry to be placed in less space. The small chip size also contributes to lower physical stress and less power consumption.

ESD Precautions

Observe ESD control procedures.

Installation Comments

Consider Temperature Coefficients of Hall IC and magnetics, as well as air gap and life time variations.

Observe temperature limits during wave soldering.

Application Comments

If reverse supply protection is desired, use a resistor in series with the V_{DD} pin that will limit the Supply Current(Fault), I_{DD}, to 50 mA. For severe EMC conditions use the application circuit on the following page.

Cross Reference

Highly advanced CMOS technology results in a Hall IC small enough to fit inside of a SOT package. Due to its extraordinary small size, the US1881SO series has no equivalent.

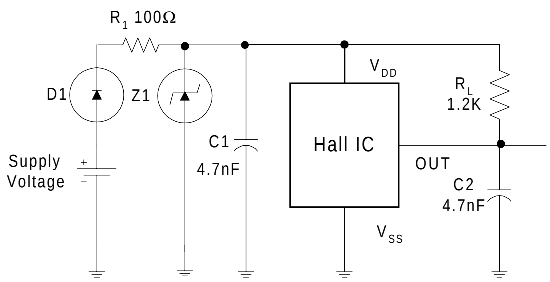
The US1881UA series can replace the following:
Allegro & Sprague - UGN3175/77UA, UGN3075/77UA, A3132/33/34UA
ITT - HAL105, HAL115, HAL125
Honeywell - SS41, SS400 series

Absolute Maximum Ratings

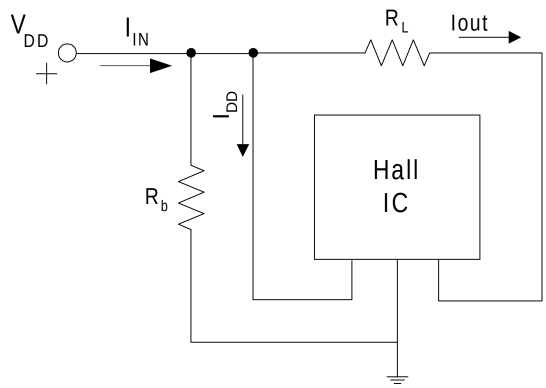
Supply Voltage (Operating), V_{DD}	3.5V to 20V
Supply Current (Fault), I_{DD}	50mA
Output Voltage, V_{OUT}	3.5V to 20V
Output Current (Fault), I_{OUT}	50mA
Power Dissipation, P_D	100mW
Operating Temperature Range, T_A	-40°C to 150°C
Storage Temperature Range, T_S	-65°C to 150°C
Maximum Junction Temp, T_J	175°C
ESD Sensitivity (All Pins)	+/- 4KV

Applications Examples

Automotive and Severe Environment Protection Circuit



Two Wire Optional Current Biasing Circuit

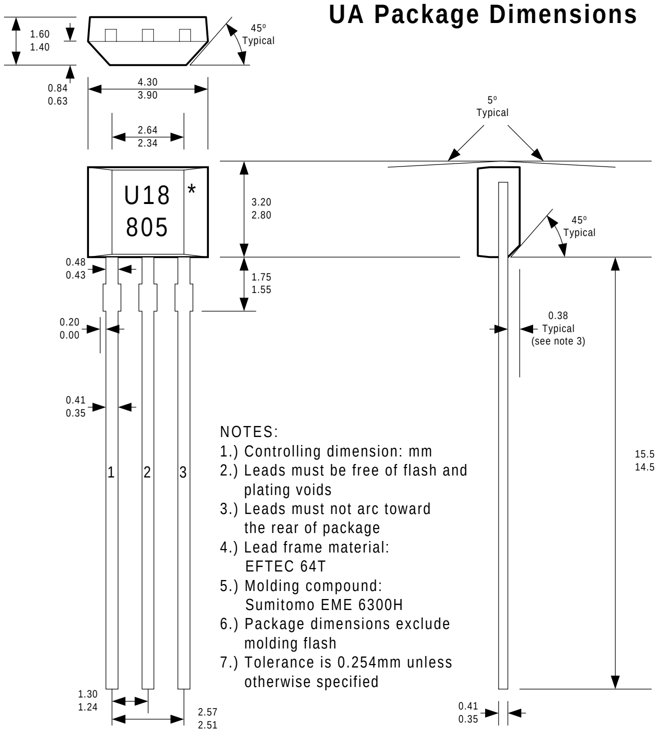


The resistors R_b and R_L can be used to bias the input current, Iin. Refer to the part specification for limiting values. This circuit will help in getting the precise ON and OFF currents desired.

B_{RP} = Ioff = (V_{DD} / Rb + I_{DD})
B_{OP} = Ion = (Ioff + V_{DD} / R_L)

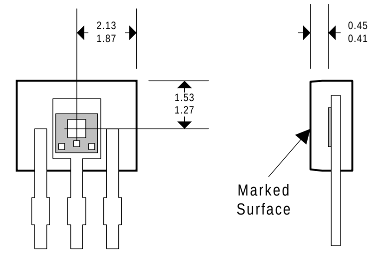
Physical Characteristics

UA Package Dimensions



NOTES:
1.) Controlling dimension: mm
2.) Leads must be free of flash and plating voids
3.) Leads must not arc toward the rear of package
4.) Lead frame material: EFTEC 64T
5.) Molding compound: Sumitomo EME 6300H
6.) Package dimensions exclude molding flash
7.) Tolerance is 0.254mm unless otherwise specified

UA Hall Plate / Chip Location



All Dimensions in millimeters

* MARKING:
Line 1:

1st digit (U)	= Supplier (Melexis)
2nd and 3rd digits (18)	= Series (1880)

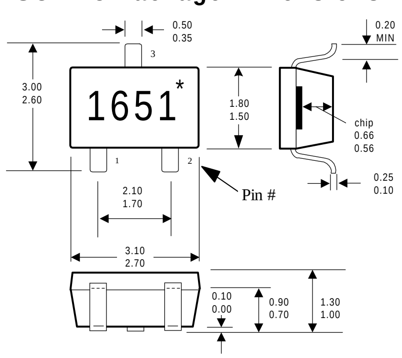
Line 2:

1st digit (8)	= Year (1998)
2nd and 3rd digits(05)	= Week of Year

PINOUT:

Pin 1	V_{DD}
Pin 2	GND
Pin 3	Output

SOT-23 Package Dimensions

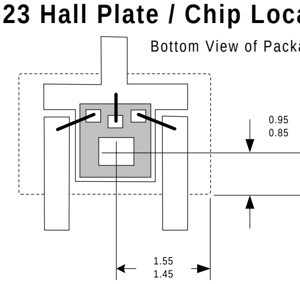


* MARKING:
1st Digit (1) = Series (1880)
2nd Digit(6) = Year - 1996
Last Digits (51) = Week of Year

NOTES:
1.) Controlling dimension: mm
2.) Lead frame material: EFTEC 64T or 1/2H
3.) Molding compound: Sumitomo EME 6300H
4.) Lead thickness after solder plating will be 0.254 mm maximum
5.) Package dimensions exclude molding flash
6.) The end flash shall not exceed 0.127 mm on each side of package
7.) Tolerance is 0.254mm unless otherwise specified

SOT-23 Hall Plate / Chip Location

Bottom View of Package



PINOUT:

Pin 1	V_{DD}
Pin 2	Output
Pin 3	GND

For more information, please contact:

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