

MOS FIELD EFFECT POWER TRANSISTORS

 μ PA1703

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

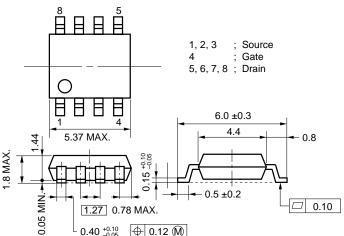
DESCRIPTION

This product is N-Channel MOS Field Effect Transistor designed for power management applications of notebook computers.

FEATURES

- Super Low On-Resistance RDS(on)1 = 10.5 m Ω MAX. (VGS = 10 V, ID = 5.0 A) RDS(on)2 = 17 m Ω MAX. (VGS = 4 V, ID = 5.0 A)
- Low Ciss Ciss = 2180 pF TYP.
- · Built-in G-S Protection Diode
- Small and Surface Mount Package (Power SOP8)

PACKAGE DIMENSIONS (in millimeter)



ABSOLUTE MAXIMUM RATINGS (TA = 25 °C, all terminals are connected)

Drain to Source Voltage	VDSS	30	V
Gate to Source Voltage	Vgss	±20	V
Drain Current (DC)	ID(DC)	±10	Α
Drain Current (pulse) Notes1	D(pulse)	±40	Α
Total Power Dissipation (T _A = 25 °C) ^{Notes2}	Рт	2.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C



Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1 %

2. Mounted on ceramic substrate of 1200 mm $^2 \times 0.7$ mm

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device acutally used, an additional protection circuit is externally required if voltage exceeding the rated voltage may be applied to this device.

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Drain

Source

Body Diode

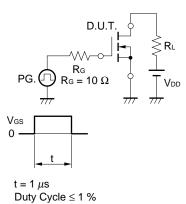


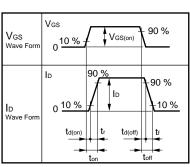
ELECTRICAL CHARACTERISTICS (TA = 25 °C, all terminals are connected)

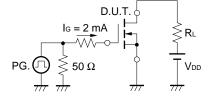
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source	RDS(on)1	Vgs = 10 V, ID = 5.0 A		8.5	10.5	mΩ
On-state Resistance	RDS(on)2	Vgs = 4 V, ID = 5.0 A		12	17	mΩ
Gate to Source Cutoff Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.0	1.6	2.0	V
Forward Transfer Admittance	yfs	V _{DS} = 10 V, I _D = 5.0 A	8.0	18		S
Drain Leakage Current	Ipss	V _{DS} = 30 V, V _{GS} = 0			10	μΑ
Gate to Source Leakage Current	Igss	Vgs = ±20 V, Vps = 0			±10	μΑ
Input Capacitance	Ciss	V _{DS} = 10 V		2180		pF
Output Capacitance	Coss	V _G s = 0		890		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		370		pF
Turn-On Delay Time	td(on)	ID = 5.0 A		25		ns
Rise Time	tr	VGS(on) = 10 V		210		ns
Turn-Off Delay Time	t _{d(off)}	V _{DD} = 15 V		120		ns
Fall Time	t f	$R_G = 10 \Omega$		75		ns
Total Gate Charge	Q _G	ID = 10 A		40		nC
Gate to Source Charge	Qgs	VDD = 24 V		5.6		nC
Gate to Drain Charge	Q _{GD}	Vgs = 10 V		9.6		nC
Body Diode Forward Voltage	VF(S-D)	IF = 10 A, VGS = 0		0.73		V
Reverse Recovery Time	trr	IF = 10 A, VGS = 0		46		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		45		nC

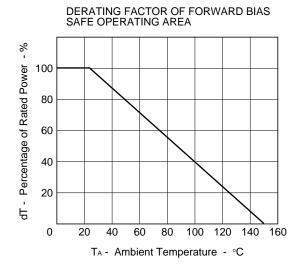
TEST CIRCUIT 1 Switching Time

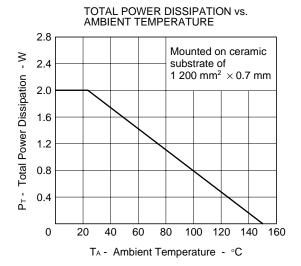
TEST CIRCUIT 2 Gate Charge

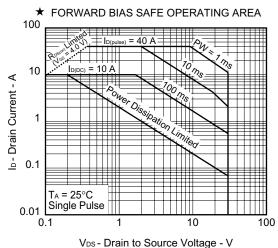






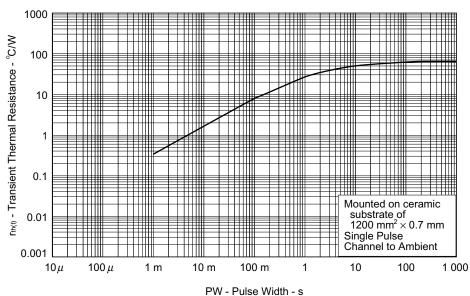


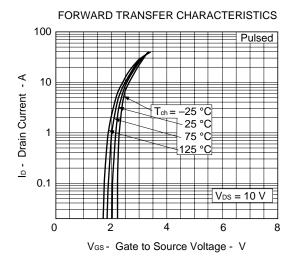


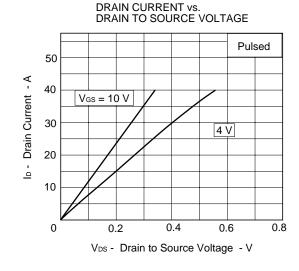


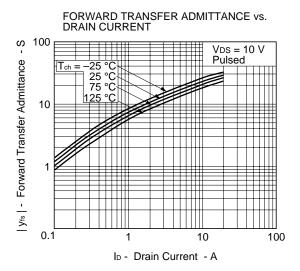
Mounted on ceramic substrate of 1200 mm²×0.7 mm

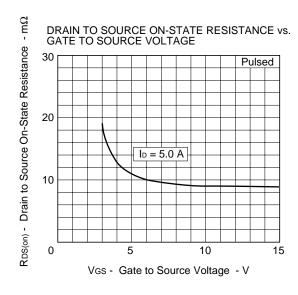
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

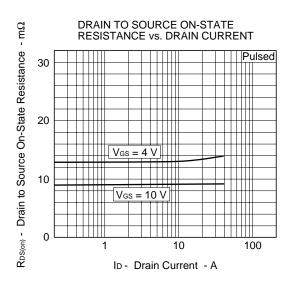


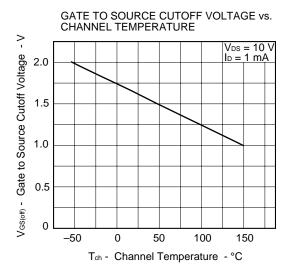




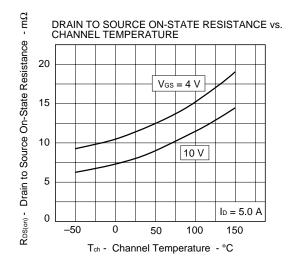


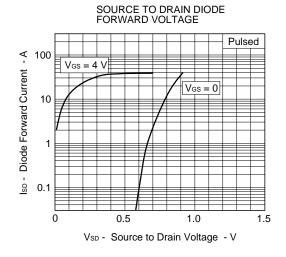


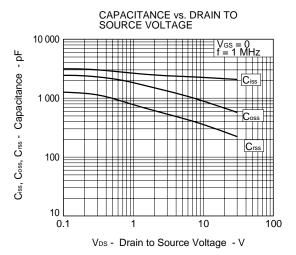


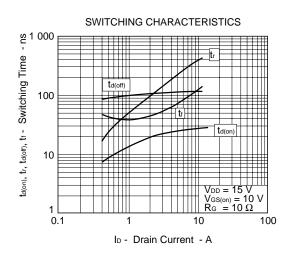


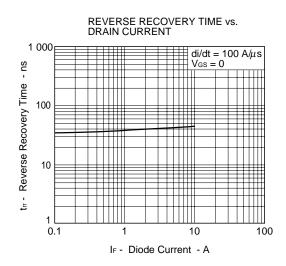


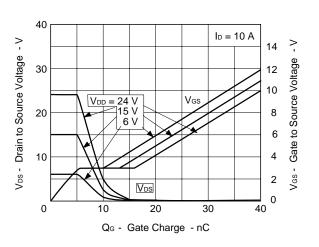












DYNAMIC INPUT/OUTPUT CHARACTERISTICS



REFERENCE

Document Name	Document No.	
NEC semiconductor device reliability/quality control system	C11745E	
Quality grade on NEC semiconductor devices	C11531E	
Semiconductor device mounting technology manual	C10535E	
Semiconductor device package manual	C10943X	
Guide to quality assurance for semiconductor devices	MEI-1202	
Application circuits using Power MOS FET	TEA-1035	
Safe operating area of Power MOS FET	TEA-1037	

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[MEMO]

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