NEC

50 dB AGC AMP + VIDEO AMP | UPC3206GR

FEATURES

- **WIDEBAND OPERATION**
- **BROADBAND AGC DYNAMIC RANGE:** 50 dB MIN
- **SUPPLY VOLTAGE:** V_{CC} = 5 V
- **PACKAGED IN 20 PIN SSOP SUITABLE FOR HIGH-DENSITY SURFACE MOUNT**

DESCRIPTION

The UPC3206GR is a Silicon RFIC designed for digital DBS and digital CATV receivers. This IC consists of a two stage gain control amplifier and a wide band linear video amplifier. This IC is packaged in a 20 pin SSOP package, making it ideal for reducing system size.

NEC's stringent quality assurance and test procedures ensure the highest reliability and performance.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

PART NUMBER / PACKAGE OUTLINE			UPC3206GR S20		
SYMBOLS	**PARAMETERS AND CONDITIONS**	**UNITS**	**MIN**	**TYP**	**MAX**
Total Block ($V_{CC}1$ = 5 V, $V_{CC}2$ = 5 V, f_{IN} = 100 MHz, R_L = 1 kΩ)					
$G_{MAX}1$	Maximum Gain 1, V_{AGC} = 5.0 V, pins G1A - G1B shorted	dB		76	
$G_{MAX}2$	Maximum Gain 2, V_{AGC} = 5.0 V, pins G1A - G1B open	dB		62	
$G_{MIN}1$	Minimum Gain 1, V_{AGC} = 0 V, pins G1A - G1B shorted	dB		10	
Total Block ($V_{CC}1$ = 5 V, $V_{CC}2$ = 9 V, f_{IN} = 100 MHz, R_L = 1 kΩ)					
$G_{MAX}3$	Maximum Gain 3, V_{AGC} = 5.0 V, pins G1A - G1B shorted	dB		80	
$G_{MAX}4$	Maximum Gain 4, V_{AGC} = 5.0 V, pins G1A - G1B open	dB		63	
$G_{MIN}2$	Minimum Gain 2, V_{AGC} = 0 V, pins G1A - G1B shorted	dB		14	
AGC Amplifier Block ($V_{CC}1$ = 5 V, f_{IN} = 100 MHz, R_L = 560 Ω)					
I_{CC1}	Circuit Current 1 (no input signal), V_{AGC} = 5 V	mA	11	16	22
I_{CC2}	Circuit Current 2 (no input signal), V_{AGC} = 0 V	mA	15	22	32
BW1	Bandwidth 1, V_{AGC} = 5 V, P_{IN} = -60 dBm	MHz	100	220	
BW2	Bandwidth 2, V_{AGC} = 0 V, P_{IN} = -15 dBm	MHz	500		
$G_{MAX}5$	Maximum Gain 5, V_{AGC} = 5.0 V, P_{IN} = -60 dBm	dB	36	38.5	41
$G_{MIN}3$	Minimum Gain 3, V_{AGC} = 0 V, P_{IN} = -15 dBm	dB		-28	-15
GCR	Gain Conrol Range, V_{AGC} = 0 to 5.0 V, P_{IN} = -35 dBm	dB	50	60	
$P_{O(SAT)}$	Maximum Output Power, V_{AGC} = 5.0 V	dBm	0	2	
NF	Noise Figure, V_{AGC} = 5.0 V	dB		5.5	
OIP_3	Output Intercept Point, V_{AGC} = 5 V , f_{IN} 2 = 106 MHz,	dBm		+4.5	
Video Amplifier Block, ($V_{CC}2$ = 9 V, f_{IN} = 100 MHz, R_L = 1k Ω)					
$I_{CC}3$	Circuit Current 3 (no input signal)	mA	16	24	34.5
V_{OUT}	Output Voltage, Single Ended	V_{P-P}		2.0	
G1	Differential Gain 1, pins G1A and G1B shorted,	V/V	160	260	400
G2	Differential Gain 2, pins G1A and G1B open	V/V	22	25	30
$A_{VS}1$	Single End Gain 1, pins G1A and G1B shorted	V/V		130	
$A_{VS}2$	Single End Gain 2, pins G1A and G1B open	V/V		12	
$IIP_3$1	Input Intercept Point 1, pins G1A and G1B shorted, f_{IN} 2 = 106 MHz	dBm		-16	
$IIP_3$2	Input Intercept Point 2, pins G1A and G1B open, f_{IN} 2 = 106 MHz	dBm		+4	
Video Amplifier Block, ($V_{CC}2$ = 5 V, f_{IN} = 100 MHz, R_L = 1k Ω)					
$I_{CC}4$	Circuit Current 4 (no input signal)	mA	8	12.5	18
G3	Differential Gain 3, pins G1A and G1B shorted	V/V	80	140	230
G4	Differential Gain 4, pins G1A and G1B open	V/V	16	22	30
$A_{VS}3$	Single End Gain 1, pins G1A and G1B shorted	V/V		70	
$A_{VS}4$	Single End Gain 2, pins G1A and G1B open	V/V		11	
$IIP_3$3	Input Intercept Point 3, pins G1A and G1B shorted, f_{IN} 2 = 106 MHz	dBm		-15	
$IIP_3$4	Input Intercept Point 4, pins G1A and G1B open, f_{IN} 2 = 106 MHz	dBm		+2	
Video Amplifier Block, ($V_{CC}2$ = 5 V, 9 V Common, f_{IN} = 100 MHz, R_L = 1k Ω, single-ended)					
BWG1	Bandwidth 1, pins G1A and G1B shorted, 3 dB down from Gain @ 5 MHz	MHz		100	

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C, unless otherwise specified)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{CC1}	Supply Voltage 1	V	6.0
V_{CC2}	Supply Voltage 2	V	10.0
P_{D1}	Power Dissipation[2], T_A = 85°C	mW	433
T_{OP1}	Operating Temp. Range	°C	-40 to +85
T_{STG}	Storage Temperature	°C	-50 to +150
P_{IN}(MAX)	Maximum Input Power	dBm	+10

Notes:
1. Operation in excess of any one of these parameters may result in permanent damage.
2. Mounted on a 50 x 50 x 1.6 mm double epoxy glass board.

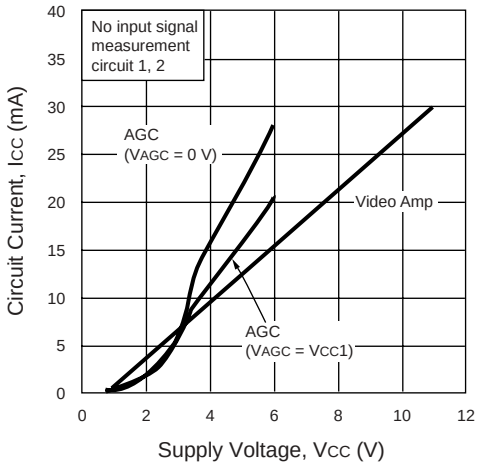
RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	UNITS	MIN	TYP	MAX
V_{CC1}	Supply Voltage 1	V	4.5	5.0	5.5
V_{CC2}	Supply Voltage 2	V	4.5	9.0	10.0
T_{OP1}[1]	Operating Temp. Range 1	°C	-40	+25	+85
T_{OP2}[2]	Operating Temp. Range 2	°C	-40	+25	+75

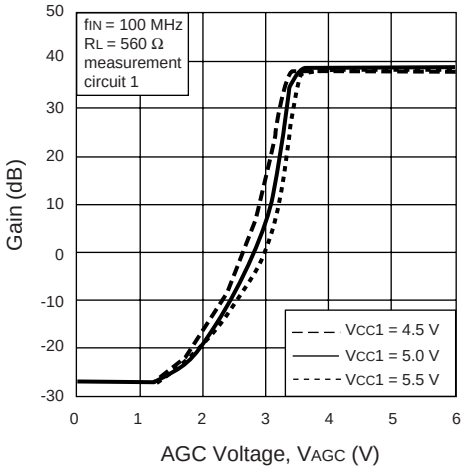
Notes:
1. V_{CC1} = V_{CC2} = 4.5 to 5.5 V.
2. V_{CC1} = 4.5 to 5.5 V, V_{CC2} = 4.5 to 10 V.

TYPICAL PERFORMANCE CURVES (T_A = 25°C)

CIRCUIT CURRENT vs. SUPPLY VOLTAGE

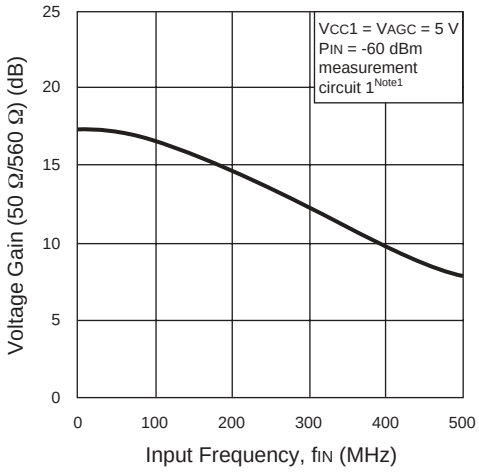


GAIN vs. AGC VOLTAGE

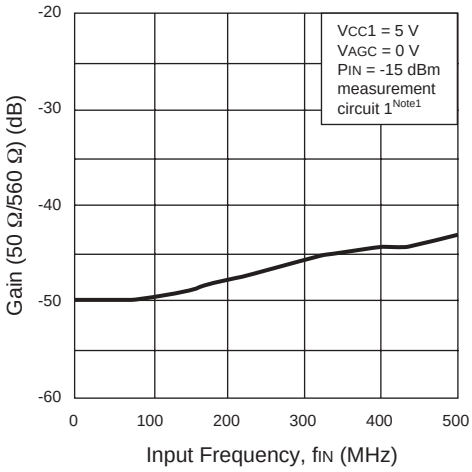


TYPICAL PERFORMANCE CURVES (T_A = 25°C)

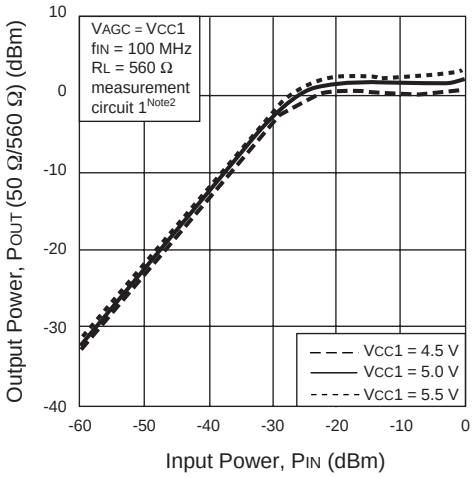
VOLTAGE GAIN vs. INPUT FREQUENCY



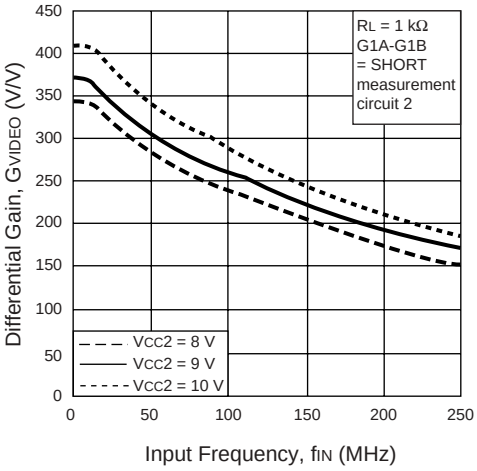
GAIN vs. INPUT FREQUENCY



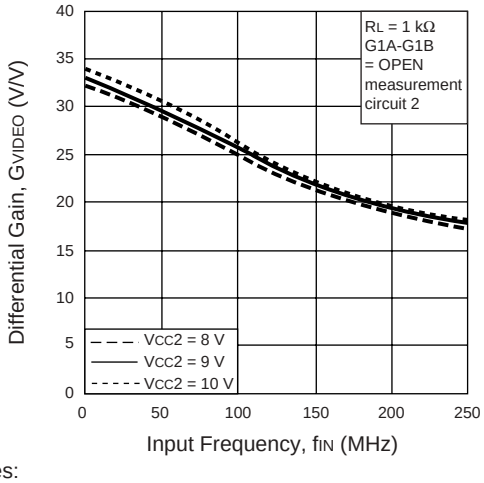
OUTPUT POWER vs. INPUT POWER



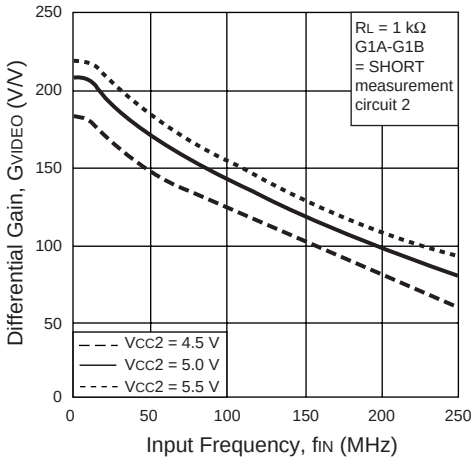
DIFFERENTIAL GAIN vs. INPUT FREQUENCY



DIFFERENTIAL GAIN vs. INPUT FREQUENCY



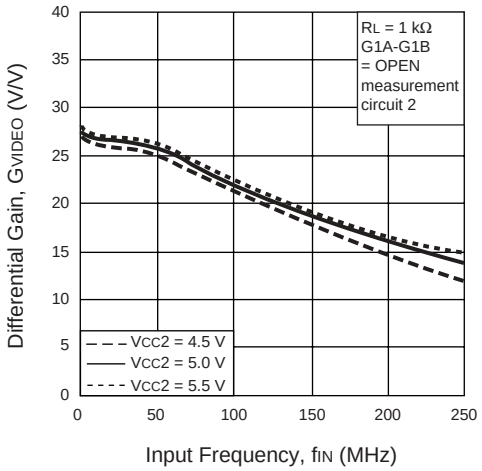
DIFFERENTIAL GAIN vs. INPUT FREQUENCY



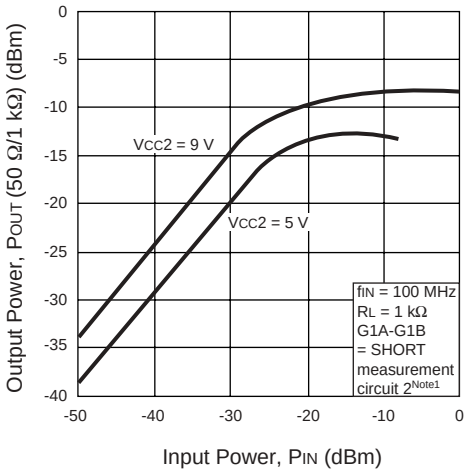
Notes:
1. Gain = (Gain at Spectrum Analyzer) +20 log (560 Ω/50 Ω).
2. Output Power = (Output Power at Spectrum Analyzer) +10 log (560 Ω/50 Ω).

TYPICAL PERFORMANCE CURVES (T_A = 25°C)

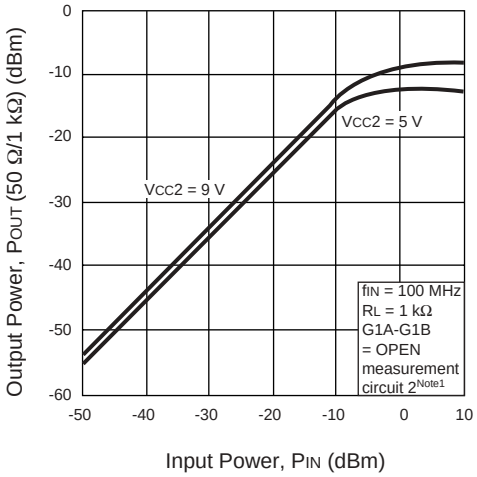
DIFFERENTIAL GAIN vs. INPUT FREQUENCY



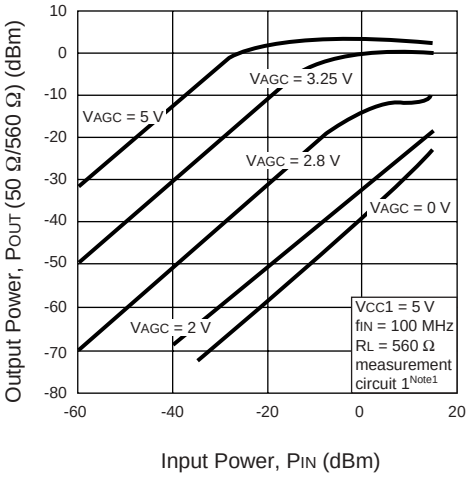
OUTPUT POWER vs. INPUT POWER



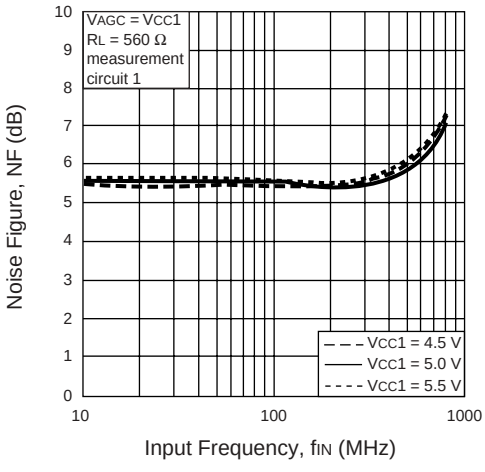
OUTPUT POWER vs. INPUT POWER



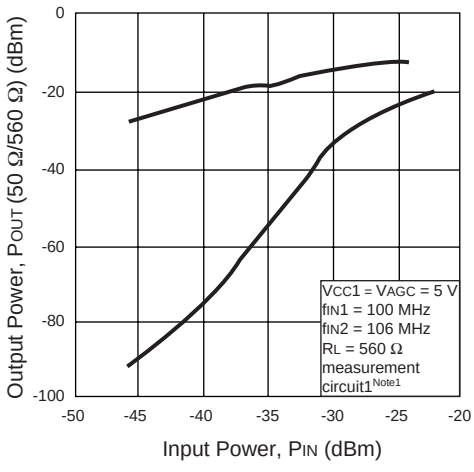
OUTPUT POWER vs. INPUT POWER



NOISE FIGURE vs. INPUT FREQUENCY



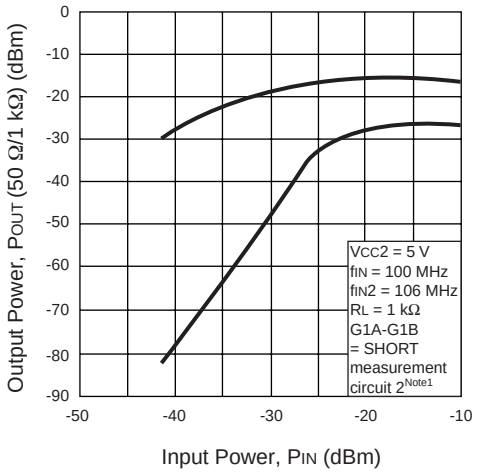
3RD ORDER INTERMODULATION DISTORTION



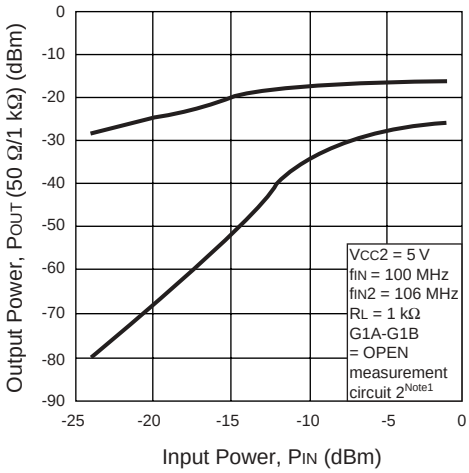
Notes:
1. Output Power = (Output Power at Spectrum Analyzer) +10 log (560 Ω/50 Ω).

TYPICAL PERFORMANCE CURVES (T_A = 25°C)

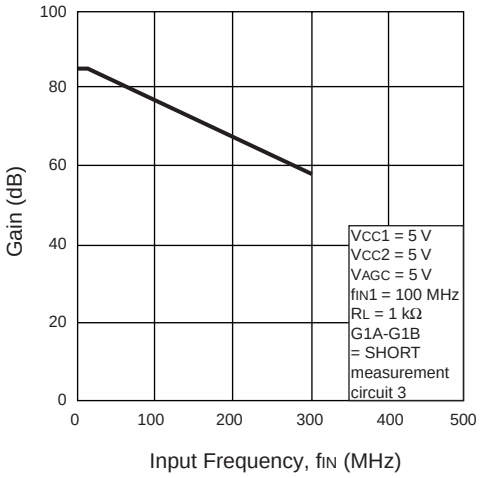
3RD ORDER INTERMODULATION DISTORTION



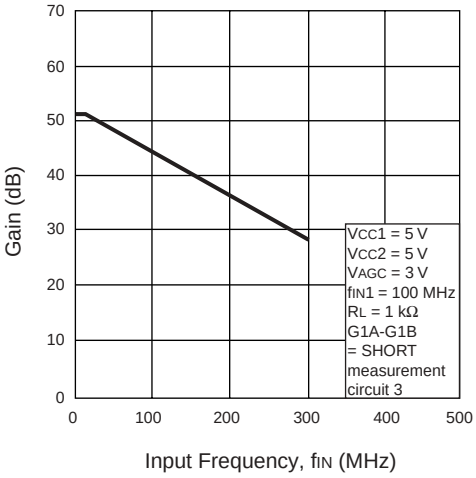
3RD ORDER INTERMODULATION DISTORTION



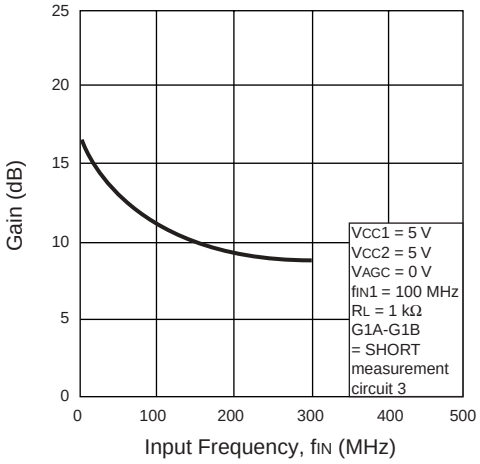
GAIN vs. INPUT FREQUENCY



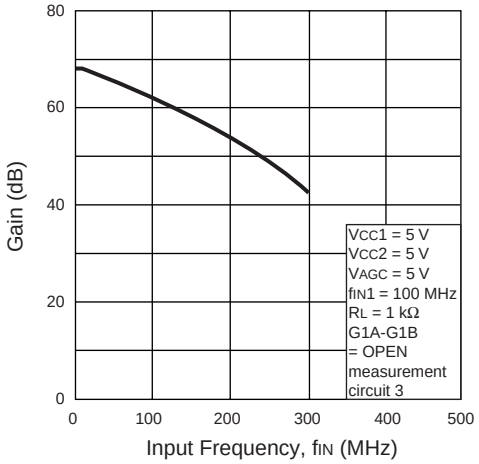
GAIN vs. INPUT FREQUENCY



GAIN vs. INPUT FREQUENCY



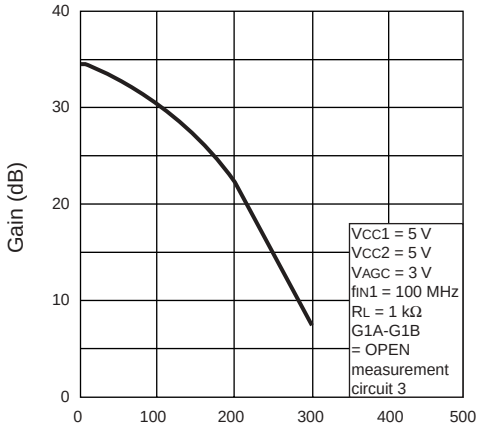
GAIN vs. INPUT FREQUENCY



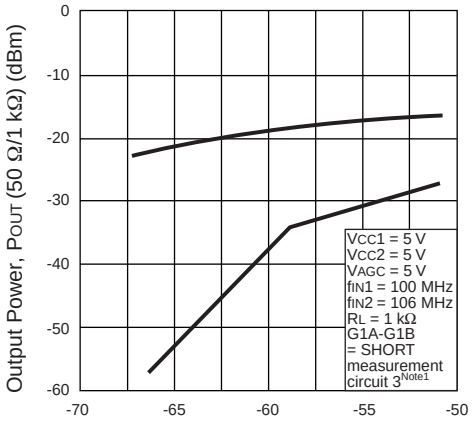
Notes:
1. Output Power = (Output Power at Spectrum Analyzer) +10 log (1 kΩ/50 Ω).

TYPICAL PERFORMANCE CURVES (T_A = 25°C)

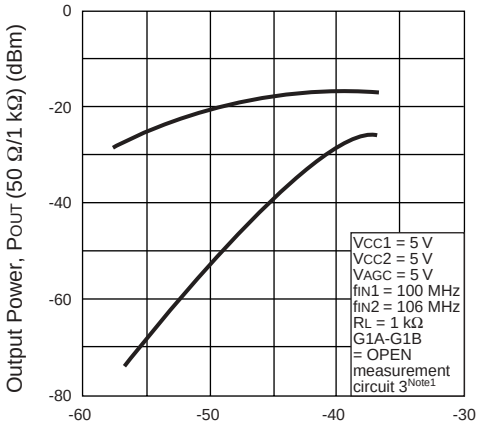
GAIN vs. INPUT FREQUENCY



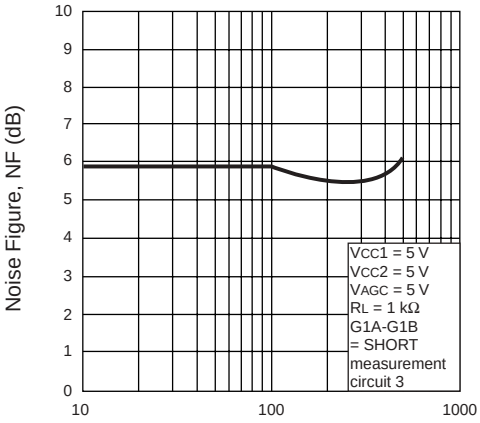
3RD ORDER INTERMODULATION DISTORTION



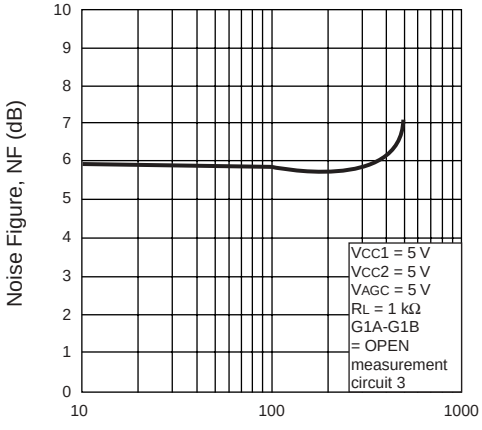
3RD ORDER INTERMODULATION DISTORTION



NOISE FIGURE vs. INPUT FREQUENCY



NOISE FIGURE vs. INPUT FREQUENCY

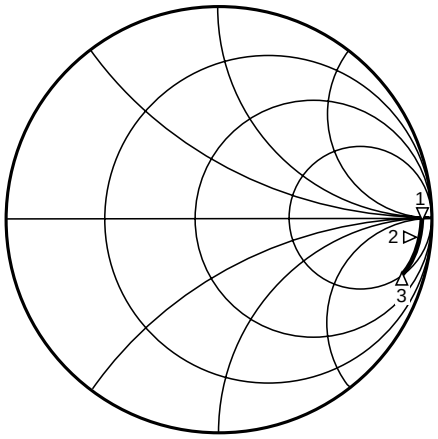


Notes:

1. Output Power = (Output Power at Spectrum Analyzer) +10 log (1 kΩ/50 Ω).

STANDARD PERFORMANCE CURVES (T_A = 25°C)

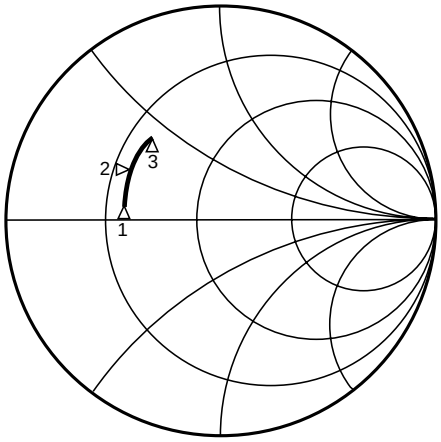
AGC IN 1 IMPEDANCE (PIN 2)



MARKER		Z_{IN}
1	45 MHz	938.4 Ω - j604.8 Ω
2	100 MHz	434.7 Ω - j573.8 Ω
3	250 MHz	122.5 Ω - j324.9 Ω

Start: 45 MHz
Stop: 250 MHz
Conditions: T_A = 25° C, $V_{CC}1$ = 5 V

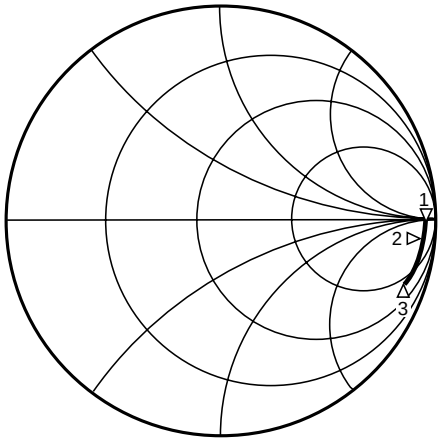
AGC OUT 1 IMPEDANCE (PIN 20)



MARKER		Z_{IN}
1	45 MHz	19.86 Ω + 3.83 Ω
2	100 MHz	20.28 Ω + 9.26 Ω
3	250 MHz	22.28 Ω + 22.48 Ω

Start: 45 MHz
Stop: 250 MHz
Conditions: T_A = 25° C, $V_{CC}1$ = 5 V

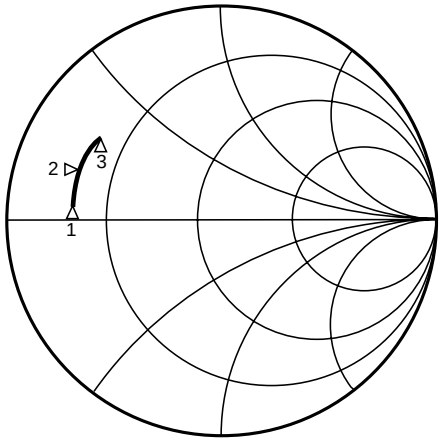
AGC IN 2 IMPEDANCE (PIN 19)



MARKER		Z_{IN}
1	45 MHz	965.8 Ω - j601.2 Ω
2	100 MHz	446.6 Ω - j661.8 Ω
3	250 MHz	126.8 Ω - j312.4 Ω

Start: 45 MHz
Stop: 250 MHz
Conditions: T_A = 25° C, $V_{CC}1$ = 5 V

AGC OUT 2 IMPEDANCE (PIN 17)

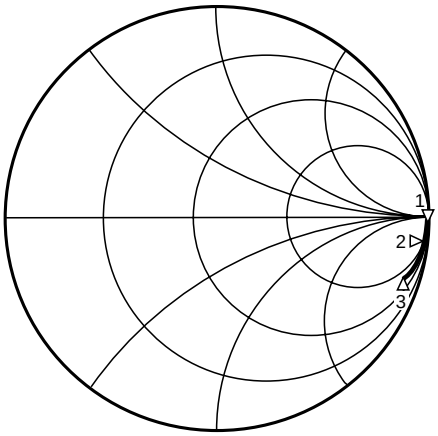


MARKER		Z_{IN}
1	45 MHz	10.32 Ω + j2.88 Ω
2	100 MHz	10.86 Ω + j6.42 Ω
3	250 MHz	12.67 Ω + j15.39 Ω

Start: 45 MHz
Stop: 250 MHz
Conditions: T_A = 25° C, $V_{CC}1$ = 5 V

STANDARD PERFORMANCE CURVES (T_A = 25°C)

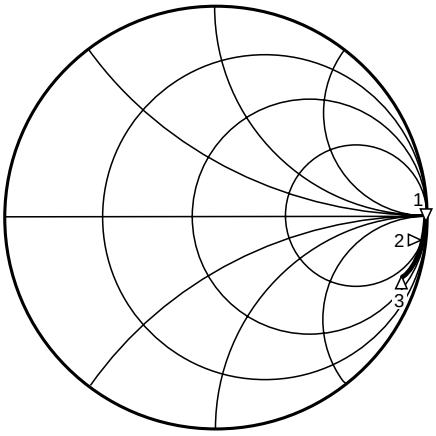
VIDEO AMP INPUT IMPEDANCE (PIN 15)



MARKER		Z_{IN}
1	45 MHz	840.0 Ω - j2560 Ω
2	100 MHz	50.19 Ω - j1259 Ω
3	250 MHz	52.03 Ω - j475.6 Ω

Start: 45 MHz
Stop: 250 MHz
Conditions: T_A = 25° C, $V_{CC}2$ = 5 V

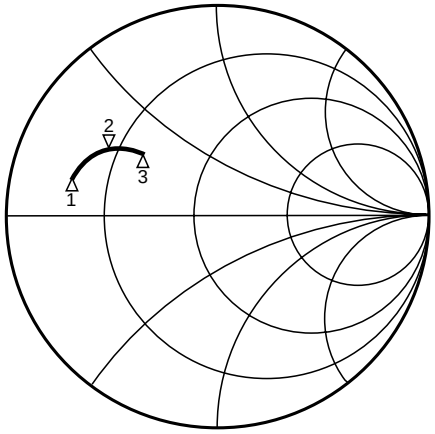
VIDEO AMP INPUT IMPEDANCE (PIN 15)



MARKER		Z_{IN}
1	45 MHz	478.3 Ω - j3091 Ω
2	100 MHz	106.13 Ω - j1368 Ω
3	250 MHz	55.11 Ω - j501.3 Ω

Start: 45 MHz
Stop: 250 MHz
Conditions: T_A = 25° C, $V_{CC}2$ = 9 V

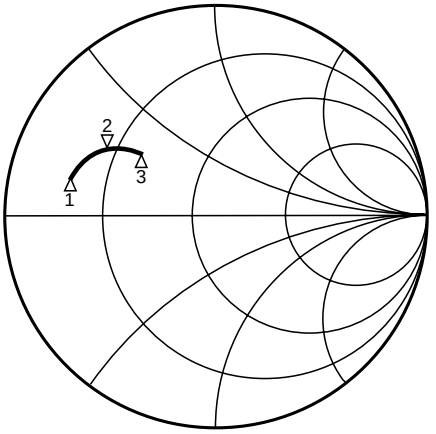
VIDEO AMP OUTPUT IMPEDANCE (PIN 12)



MARKER		Z_{IN}
1	45 MHz	9.88 Ω + j6.25 Ω
2	100 MHz	14.21 Ω + j11.78 Ω
3	250 MHz	23.64 Ω + j15.73 Ω

Start: 45 MHz
Stop: 250 MHz
Conditions: T_A = 25° C, $V_{CC}2$ = 5 V, 11 pin is grounded through 50 Ω resistor.

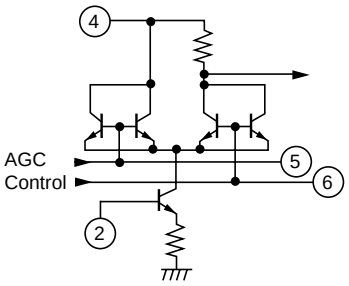
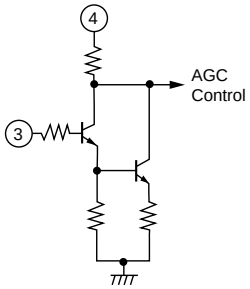
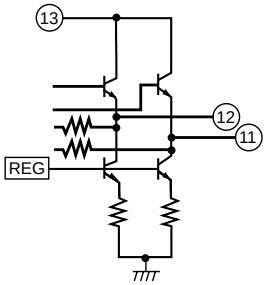
VIDEO AMP OUTPUT IMPEDANCE (PIN 12)



MARKER		Z_{IN}
1	45 MHz	7.36 Ω + j4.85 Ω
2	100 MHz	10.50 Ω + j9.58 Ω
3	250 MHz	19.37 Ω + j13.70 Ω

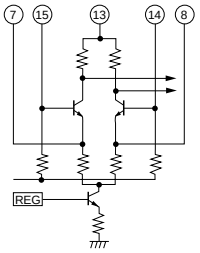
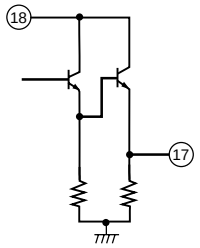
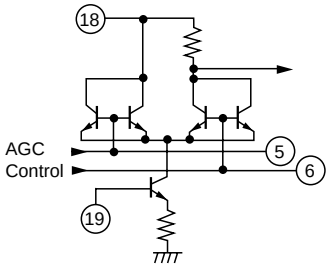
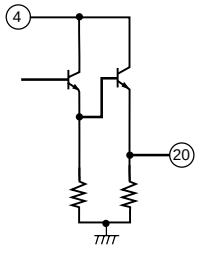
Start: 45 MHz
Stop: 250 MHz
Conditions: T_A = 25° C, $V_{CC}2$ = 9 V, 11 pin is grounded through 50 Ω resistor.

PIN FUNCTIONS

Pin No.	Symbol	Pin Voltage (V)	Description	Equivalent Circuit
1	AGC GND1	0	Ground pin of AGC amplifier 1. Form ground pattern as wide as possible to minimize ground impedance.	
2	AGC IN1 Note 1	1.02 1.02	Input pin to AGC amplifier 1.	
3	VAGC	0 to 5	Gain control pin. V_{AGC} up = gain up. It is recommended to use a 100k Ω voltage divider at this pin.	
4	AGC $V_{CC}1$	5	Power supply pin of AGC amplifier 1. This pin should be externally equipped with a bypass capacitor to minimize ground impedance.	
5	BPCAP4 Note 1	2.61 2.61	Bypass pins of AGC amplifier 1 and 2. These pins should be externally equipped with bypass capacitors to ground.	Refer to Equivalent circuit of pin 1 and pin 2.
6	BPCAP2 Note 1	2.84 2.49		
7	G1A Note 2	1.72 3.34	Gain control pins of the video amplifier. The gain may be adjusted by varying the value of the resistor between pins 7 and 8. Maximum gain = short. Minimum gain = open.	Refer to Equivalent circuit of pin 14 and pin 15.
8	G1B Note 2	1.72 3.34		
9	VAMP GND1	0	Ground pins of the video amplifier. Form ground pattern as wide as possible to minimize ground impedance.	
10	VAMP GND2	0		
11	VAMP OUT2 Note 2	2.52 4.92	Output pins of the video amplifier. With R_L = 1k Ω, the single-ended output voltage is 2 Vp-p. OUT1 and INA are in phase. OUT2 and INB are in phase. In the case of a single-ended output, bypass the unused pin to ground through a capacitor.	
12	VAMP OUT1 Note 2	2.52 4.92		

Notes:
1. Top: V_{AGC} = $V_{CC}1$ Bottom: V_{AGC} = 0 V
2. Top: $V_{CC}2$ = 5 V Bottom: $V_{CC}2$ = 9 V

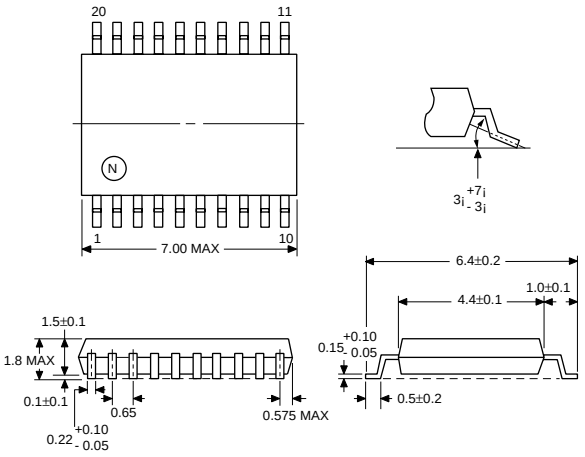
PIN FUNCTIONS

Pin No.	Symbol	Pin Voltage (V)	Description	Equivalent Circuit
13	VAMP $V_{CC}2$	5 to 9	Power supply pin of the video amplifier. This pin should be externally equipped with a bypass capacitor to minimize ground impedance.	
14	INB Note 2	2.49 4.13	Input pins to the video amplifier. In the case of a single-ended input, bypass the unused pin to ground through a capacitor.	
15	INA Note 2	2.49 4.13		
16	AGC GND2	0	Ground pin of AGC amplifier 2. Form ground pattern as wide as possible to minimize ground impedance.	
17	AGC OUT2 Note 1	1.69 3.31	Output pin of AGC amplifier 2.	
18	AGC $V_{CC}1$	5	Power supply pin of AGC amplifier 2. This pin should be externally equipped with a bypass capacitor to minimize ground impedance.	
19	AGC IN2 Note 1	1.01 1.01	Input pin to AGC amplifier 2.	
20	AGC OUT1 Note 1	1.71 3.35	Output pin to AGC amplifier 1.	

Notes:
1. Top: $V_{AGC} = V_{CC}1$ Bottom: $V_{AGC} = 0$ V
2. Top: $V_{CC}2 = 5$ V Bottom: $V_{CC}2 = 9$ V

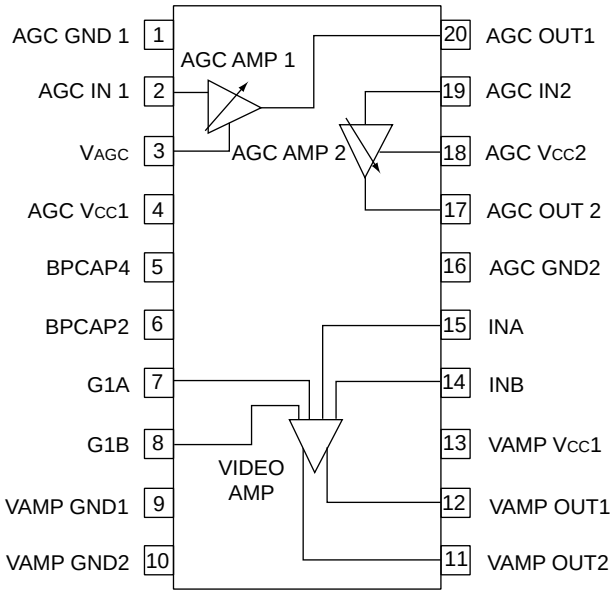
OUTLINE DIMENSIONS (Units in mm)

PACKAGE OUTLINE S20

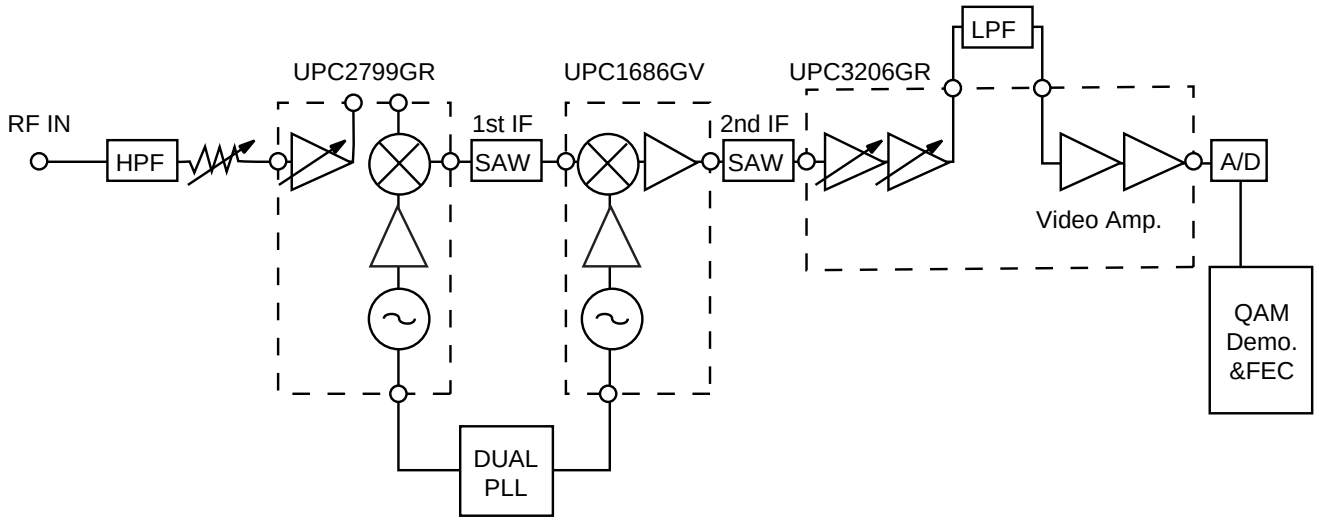


All dimensions are typical unless specified otherwise.

INTERNAL BLOCK DIAGRAM

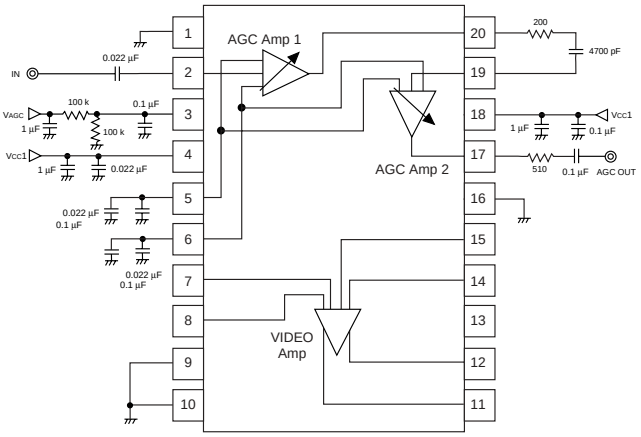


TYPICAL APPLICATION



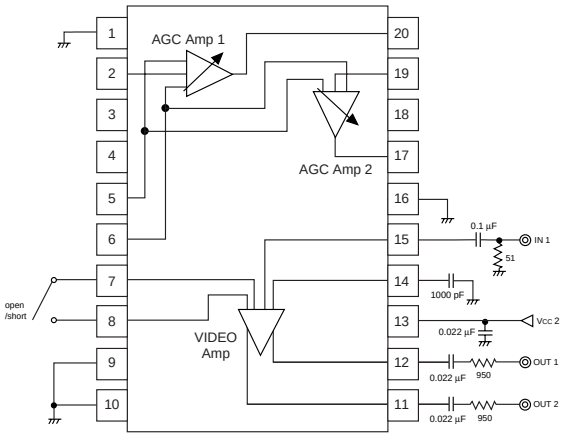
MEASUREMENT CIRCUIT 1

AGC AMP BLOCK



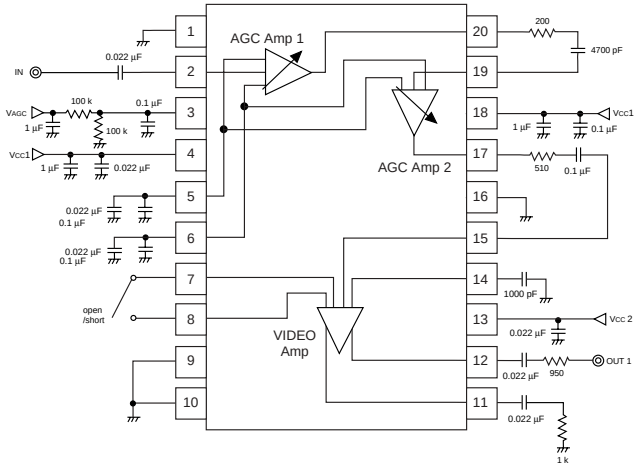
MEASUREMENT CIRCUIT 2

VIDEO AMP BLOCK



MEASUREMENT CIRCUIT 3

TOTAL BLOCK



ORDERING INFORMATION

PART NUMBER	QUANTITY
UPC3206GR-E1	2.5 k/Reel

Notes:
Embossed tape, 12 mm wide. Pin 1 indicates pull-out direction of tape.