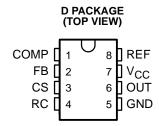
- Controlled Baseline
  - One Assembly/Test Site, One Fabrication Site
- Extended Temperature Performance of –40°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product Change Notification
- Qualification Pedigree<sup>†</sup>
- ESD Protection Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- 100 μA Typical Starting Supply Current
- 500 μA Typical Operating Supply Current

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- Operation to 1MHz
- Internal Soft Start
- Internal Fault Soft Start
- Internal Leading-Edge Blanking of the Current Sense Signal
- 1 Amp Totem-Pole Output
- 70 ns Typical Response from Current-Sense to Gate Drive Output
- 1.5% Tolerance Voltage Reference
- Same Pinout as UC3842 and UC3842A



#### description

The UCC2800/1/2/3/4/5 family of high-speed, low-power integrated circuits contain all of the control and drive components required for off-line and DC-to-DC fixed frequency current-mode switching power supplies with minimal parts count.

These devices have the same pin configuration as the UC2842/3/4/5 family, and also offer the added features of internal full-cycle soft start and internal leading-edge blanking of the current-sense input.

The UCC2800/1/2/3/4/5 family offers choice of maximum duty cycle and critical voltage levels. Lower reference parts such as the UCC2803 and UCC2805 fit best into battery operated systems, while the higher reference and the higher UVLO hysteresis of the UCC2802 and UCC2804 make these ideal choices for use in off-line power supplies.

PART NUMBER	MAXIMUM DUTY CYCLE	REFERENCE VOLTAGE	TURN-ON THRESHOLD	TURN-OFF THRESHOLD
UCC2800	100%	5 V	7.2 V	6.9 V
UCC2801	50%	5 V	9.4 V	7.4 V
UCC2802	100%	5 V	12.5 V	8.3 V
UCC2803	100%	4 V	4.1 V	3.6 V
UCC2804	50%	5 V	12.5 V	8.3 V
UCC2805	50%	4 V	4.1 V	3.6 V



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

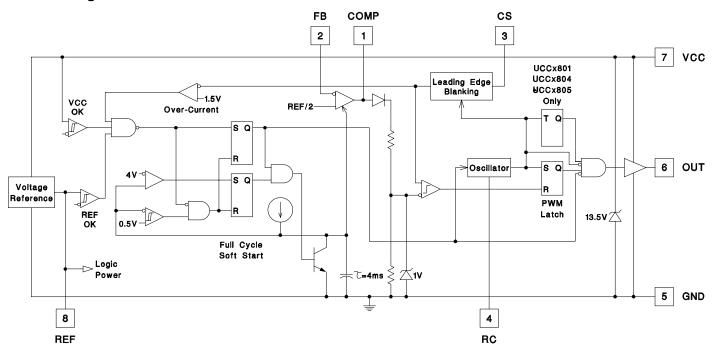


#### **ORDERING INFORMATION**

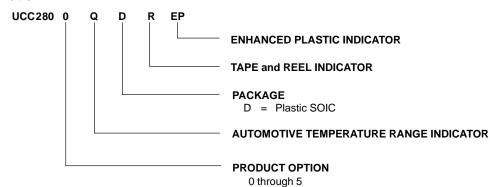
TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
–40°C to 125°C	SOP - D	Tape and reel	UCC2800QDREP	2800EP	
	SOP - D	Tape and reel	UCC2801QDREP	2801EP	
	SOP – D	Tape and reel	UCC2802QDREP	2802EP	
	SOP – D	Tape and reel UCC2803QDREP		2803EP	
	SOP – D	Tape and reel	UCC2804QDREP	2804EP	
	SOP - D	Tape and reel	UCC2805QDREP	2805EP	

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

# block diagram



# **Ordering Information**





# UCC2800/2801/2802/2803/2804/2805-EP LOW-POWER BICMOS CURRENT-MODE PWM

SGLS135B - SEPTEMBER 2002 - REVISED MARCH 2003

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)  $\begin{array}{c} V_{CC} \text{ voltage } \$ & 12 \text{ V} \\ V_{CC} \text{ current } \$ & 30 \text{ mA} \\ \text{Output current, I}_O & \pm 1 \text{ A} \\ \text{Output energy (Capacitive Load)} & 20 \text{ }\mu\text{J} \\ \text{Analog Inputs (FB, CS)} & -0.3 \text{ V to } 6.3 \text{ V} \\ \text{Power Dissipation at T}_A < +25^{\circ}\text{C (D package)} & 0.65 \text{ W} \\ \text{Storage temperature range, T}_{\text{stg}} & -65^{\circ}\text{C to } 150^{\circ}\text{C} \\ \text{Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds} & 300^{\circ}\text{C} \\ \end{array}$ 

# electrical characteristics, $T_A=-40\,^{\circ}C$ to $125\,^{\circ}C,\,V_{CC}$ = 10 V (see Note 1), $R_T$ = 100 $\,k\Omega$ from REF to RC, $C_T$ = 330 pF from RC to GND, 0.1 F capacitor from $V_{CC}$ to GND, 0.1 F capacitor from $V_{REF}$ to GND and $T_A$ = $T_J$ (unless otherwise stated)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS	
Reference Section							
Outrot with an	00	UCC2800/01/02/04	4.925	5.0	5.075	V	
Output voltage	$T_J = 25^{\circ}C, I = 0.2 \text{ mA}$	UCC2803/05	3.94	4.0	4.06		
Load regulation voltage	I = 0.2 mA to 5 mA	I = 0.2 mA to 5 mA			30	mV	
Line we wild the western	40.74	T <sub>J</sub> = 25°C			1.9		
Line regulation voltage	V <sub>CC</sub> = 10 V to clamp	$T_J = -40^{\circ}C$ to $125^{\circ}C$			2.5	mV/V	
Tatalandadan		UCC2800/01/02/04	4.88	5.0	5.1	V	
Total variation voltage	See Note 5	UCC2803/05	3.9	4.0	4.08		
Output noise voltage	f = 10 Hz to 10 kHz, See Note 7	T <sub>J</sub> = 25°C		130		μV	
Long term stability	1000 hours, See Note 7	T <sub>A</sub> = 125°C		5		mV	
Output short-circuit current			-5		-35	mA	



<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

<sup>‡</sup>Unless otherwise indicated, voltages are reference to ground and currents are positive into and negative out of the specified terminals.

<sup>§</sup> In normal operation V<sub>CC</sub> is powered through a current limiting resistor. Absolute maximum of 12 V applies when V<sub>CC</sub> is driven from a low impedance source such that I<sub>CC</sub> does not exceed 30 mA (which includes gate drive current requirement).

# UCC2800/2801/2802/2803/2804/2805-EP LOW-POWER BICMOS CURRENT-MODE PWM

SGLS135B - SEPTEMBER 2002 - REVISED MARCH 2003

electrical characteristics,  $T_A=-40\,^{\circ}C$  to  $125\,^{\circ}C$ ,  $V_{CC}=10$  V (see Note 1),  $R_T=100~k\Omega$  from REF to RC,  $C_T=330$  pF from RC to GND, 0.1 F capacitor from  $V_{CC}$  to GND, 0.1 F capacitor from  $V_{REF}$  to GND and  $T_A=T_J$  (unless otherwise stated)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNITS	
Oscillator Section	<u>.</u>							
0			UCC2800/01/02/04	40	46	52		
Oscillator frequency	See Note 2		UCC2803/05	26	31	36	kHz	
Temperature stability	See Note 7	See Note 7			2.5		%	
Amplitude peak-to-peak				2.25	2.4	2.55	V	
Oscillator peak voltage					2.45		V	
Error Amplifier Section								
Input voltage	COMP = 2.5 V		UCC2800/01/02/04	2.44	2.5	2.56	- V	
	COMP = 2.0 V		UCC2803/05	1.95	2.0	2.05		
Input bias current				-1		1	μΑ	
Open loop voltage gain				60	80		db	
COMP sink current	FB = 2.7 V, C0	OMP = 1	.1 V	0.3		3.5	mA	
COMP source current	FB = 1.8 V, C0	OMP = F	REF – 1.2 V	-0.2	-0.5	-0.8	mA	
Gain bandwidth product	See Note 7				2		MHz	
PWM Section	<u>.</u>						•	
			UCC2800/02/03	97	99	100	- %	
Maximum duty cycle			UCC2801/04/05	48	49	50		
Minimum duty cycle	COMP = 0 V					0	%	
Current Sense Section	•							
Gain	See Note 3			1.1	1.65	1.8	V/V	
Maximum input signal	COMP = 5 V, Se	ee Note	4	0.9	1	1.1	V	
Input bias current				-200		200	nA	
CS blank time				50	100	150	ns	
Over-current threshold voltage				1.42	1.55	1.68	V	
COMP to CS offset voltage	CS = 0 V		0.45	0.9	1.35	V		
Output Section (OUT)	•			•				
	I <sub>OUT</sub> = 20 mA		All parts		0.1	0.4	- v	
Low-level output voltage	I <sub>OUT</sub> = 200 mA		All parts		0.35	0.9		
	I <sub>OUT</sub> = 50 mA, V <sub>CC</sub>	= 5 V	UCC2803/05		0.15	0.4		
	I <sub>OUT</sub> = 20 mA, V <sub>CC</sub>		All parts		0.7	1.2		
	I <sub>OUT</sub> = -20 mA		All parts		0.15	0.4	) v	
High-level output voltage V <sub>SAT</sub> (V <sub>CC</sub> - OUT)	I <sub>OUT</sub> = -200 mA		All parts		1	1.9		
	I <sub>OUT</sub> = -50 mA, V <sub>CC</sub>	) = 5 V	UCC2803/05		0.4	0.9		
Rise time	C <sub>L</sub> = 1 nF				41	70	ns	
Fall time	C <sub>L</sub> = 1 nF				44	75	ns	



# UCC2800/2801/2802/2803/2804/2805-EP LOW-POWER BICMOS CURRENT-MODE PWM

SGLS135B - SEPTEMBER 2002 - REVISED MARCH 2003

# electrical characteristics, $T_A=-40\,^{\circ}C$ to $125\,^{\circ}C,\,V_{CC}=10$ V (see Note 1), $R_T=100\,$ k $\Omega$ from REF to RC, $C_T=330$ pF from RC to GND, 0.1 F capacitor from $V_{CC}$ to GND, 0.1 F capacitor from $V_{REF}$ to GND and $T_A=T_J$ (unless otherwise stated)

PARAMETER	-	TEST CONDITIONS			TYP	MAX	UNITS		
Undervoltage Lockout Section									
		U	ICC2800	6.6	7.2	7.8	V		
Others there are also	On a Nata O	U	ICC2801	8.6	9.4	10.2			
Start threshold	See Note 6	U	ICC2802/04	11.5	12.5	13.5			
		U	ICC2803/05	3.7	4.1	4.5			
		U	ICC2800	6.3	6.9	7.5	- v		
		U	ICC2801	6.8	7.4	8			
Stop threshold	See Note 6	U	ICC2802/04	7.6	8.3	9			
		U	ICC2803/05	3.2	3.6	4			
		U	ICC2800	0.12	0.3	0.48			
		U	ICC2801	1.6	2	2.4	] ,,		
Start to stop hysteresis		U	ICC2802/04	3.5	4.2	5.1	- V		
		U	ICC2803/05	0.2	0.5	0.8			
Soft Start Section	·	·							
COMP rise time	FB = 1.8 V,	Rise from 0.5	5 V to REF – 1 V		4	10	ms		
Overall Section	·								
Start-up current	V <sub>CC</sub> < Start Threshold				0.1	0.2	mA		
Operating supply current	FB = 0 V,	CS = 0 V			0.5	1	mA		
V <sub>CC</sub> internal zener voltage	I <sub>CC</sub> = 10 mA,	See Notes 6	and 8	12	13.5	15	V		
V <sub>CC</sub> internal zener voltage minus start threshold voltage	See Note 6	U	ICC2802/04	0.5	1.0		V		

NOTES: 1. Adjust  $V_{CC}$  above the start threshold before setting at 10 V.

2. Oscillator frequency for the UCC2800, UCC2802 and UCC2803 is the output frequency. Oscillator frequency for the UCC2801, UCC2804 and UCC2805 is twice the output frequency.

 $A = \frac{\Delta V_{COMP}}{\Delta V_{CS}}$ 

3. Gain is defined by:

 $0 \le V_{CS} \le 0.8 \text{ V}.$ 

- 4. Parameter measured at trip point of latch with Pin 2 at 0 V.
- 5. Total Variation includes temperature stability and load regulation.
- 6. Start Threshold, Stop Threshold and Zener Shunt Thresholds track one another.
- 7. Not production tested.
- 8. The device is fully operating in clamp mode as the forcing current is higher than the normal operating supply current.



# UCC2800/2801/2802/2803/2804/2805-EP LOW-POWER BICMOS CURRENT-MODE PWM

SGLS135B - SEPTEMBER 2002 - REVISED MARCH 2003

## detailed terminal descriptions

#### **COMP**

COMP is the output of the error amplifier and the input of the PWM comparator.

Unlike other devices, the error amplifier in the UCC2800 family is a true, low output-impedance, 2 MHz operational amplifier. As such, the COMP terminal can both source and sink current. However, the error amplifier is internally current limited, so that one can command zero duty cycle by externally forcing COMP to GND.

The UCC2800 family features built-in full cycle Soft Start. Soft Start is implemented as a clamp on the maximum COMP voltage.

#### CS

CS is the input to the current sense comparators. The UCC2800 family has two different current sense comparators: the PWM comparator and an over-current comparator.

The UCC2800 family contains digital current sense filtering, which disconnects the CS terminal from the current sense comparator during the 100 ns interval immediately following the rising edge of the OUT pin. This digital filtering, also called leading-edge blanking, means that in most applications, no analog filtering (RC filter) is required on CS. Compared to an external RC filter technique, the leading-edge blanking provides a smaller effective CS to OUT propagation delay. Note, however, that the minimum non-zero On-Time of the OUT signal is directly affected by the leading-edge-blanking and the CS to OUT propagation delay.

The over-current comparator is only intended for fault sensing, and exceeding the over-current threshold will cause a soft start cycle.

#### FB

FB is the inverting input of the error amplifier. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.

## ground (GND)

GND is reference ground and power ground for all functions on this part.

#### OUT

OUT is the output of a high-current power driver capable of driving the gate of a power MOSFET with peak currents exceeding  $\pm 750$  mA. OUT is actively held low when  $V_{CC}$  is below the UVLO threshold.

The high-current power driver consists of FET output devices, which can switch all of the way to GND and all of the way to  $V_{CC}$ . The output stage also provides a very low impedance to overshoot and undershoot. This means that in many cases, external schottky clamp diodes are not required.



# detailed descriptions (continued)

#### **RC**

RC is the oscillator timing pin. For fixed frequency operation, set timing capacitor charging current by connecting a resistor from REF to RC. Set frequency by connecting timing capacitor from RC to GND. For best perfomance, keep the timing capacitor lead to GND as short and direct as possible. If possible, use separate ground traces for the timing capacitor and all other functions.

The frequency of oscillation can be estimated with the following equations:

$$\label{eq:UCC2800/01/02/04} \begin{split} & \text{UCC2800/01/02/04}: \ F = \frac{1.5}{R \times C} \\ & \text{UCC2803/UCC2805}: \ F = \frac{1.0}{R \times C} \end{split}$$

(1)

where frequency is in Hz, resistance is in ohms, and capacitance is in farads. The recommended range of timing resistors is between 10k and 200k and timing capacitor is 100 pF to 1000 pF. Never use a timing resistor less than 10k.

To prevent noise problems, bypass  $V_{CC}$  to GND with a ceramic capacitor as close to the  $V_{CC}$  pin as possible. An electrolytic capacitor may also be used in addition to the ceramic capacitor.

#### voltage reference (REF)

REF is the voltage reference for the error amplifier and also for many other functions on the IC. REF is also used as the logic power supply for high speed switching logic on the IC.

When  $V_{CC}$  is greater than 1 V and less than the UVLO threshold, REF is pulled to ground through a 5k ohm resistor. This means that REF can be used as a logic output indicating power system status. It is important for reference stability that REF is bypassed to GND with a ceramic capacitor as close to the pin as possible. An electrolytic capacitor may also be used in addition to the ceramic capacitor. A minimum of 0.1  $\mu$ F ceramic is required. Additional REF bypassing is required for external loads greater than 2.5 mA on the reference.

To prevent noise problems with high speed switching transients, bypass REF to ground with a ceramic capacitor very close to the IC package.

#### power (V<sub>CC</sub>)

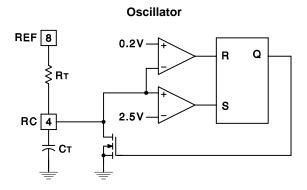
 $V_{CC}$  is the power input connection for this device. In normal operation  $V_{CC}$  is powered through a current limiting resistor. Although quiescent  $V_{CC}$  current is very low, total supply current will be higher, depending on OUT current. Total  $V_{CC}$  current is the sum of quiescent  $V_{CC}$  current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge  $(Q_q)$ , average OUT current can be calculated from:

$$I_{OUT} = Q_g \times F.$$

(2)



#### PARAMETER MEASUREMENT INFORMATION



The UCC3800/1/2/3/4/5 oscillator generates a sawtooth waveform on RC. The rise time is set by the time constant of RT and CT. The fall time is set by CT and an internal transistor on-resistance of approximately 125. During the fall time, the output is off and the maximum duty cycle is reduced below 50% or 100% depending on the part number. Larger timing capacitors increase the discharge time and reduce the maximum duty cycle and frequency.

Figure 1

# UCC1803/05 V<sub>REF</sub> vs. V<sub>CC</sub>; I<sub>LOAD</sub> = 0.5 mA

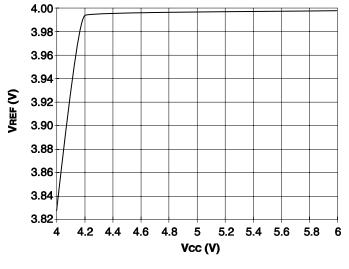
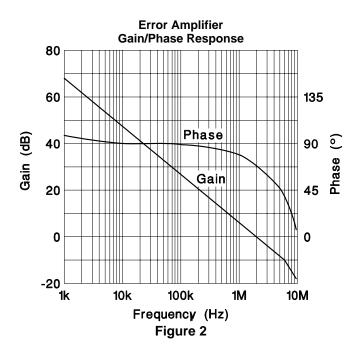


Figure 3



# UCC1800/01/02/04 Oscillator Frequency vs. R<sub>T</sub> and C<sub>T</sub>

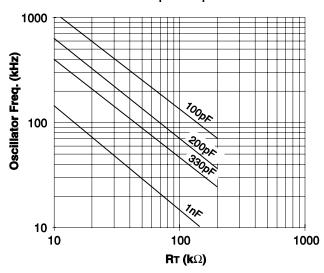
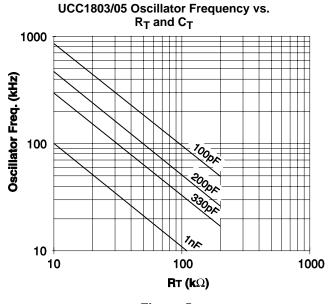


Figure 4



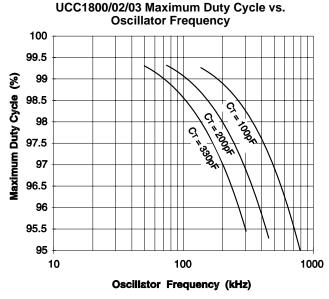
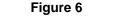
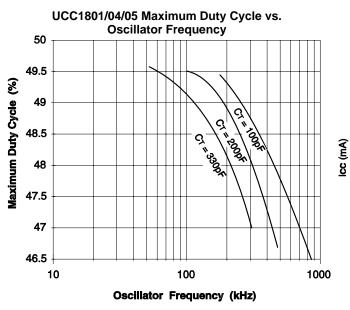


Figure 5



UCC1800 I<sub>CC</sub> vs. Oscillator Frequency



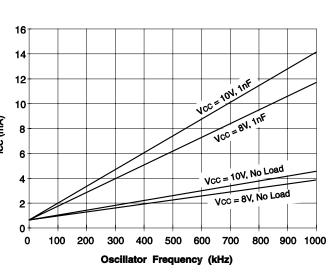


Figure 7

Figure 8

# UCC1805 I<sub>CC</sub> vs Oscillator Frequency

# Dead Time vs. $C_T$ , $R_T = 100k$

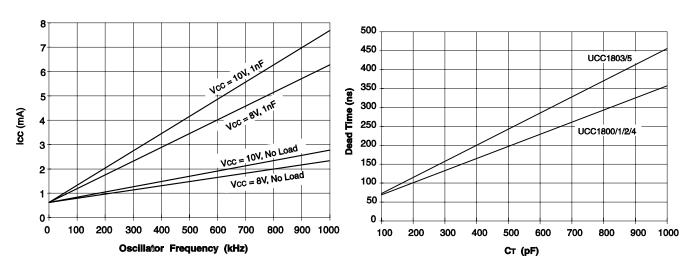


Figure 9

Figure 10

### COMP to CS Offset vs. Temperature, CS = 0 V

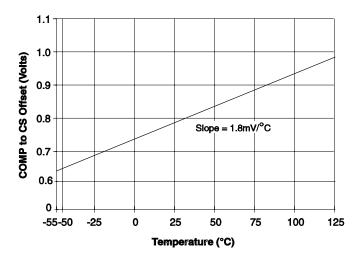


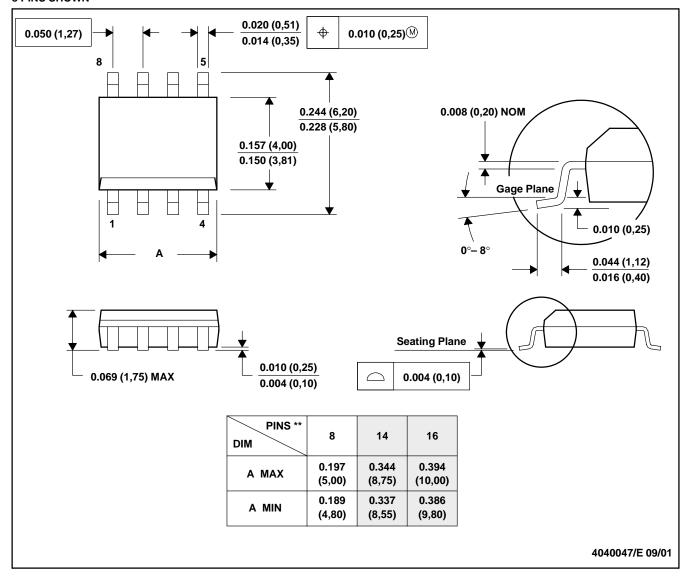
Figure 11

# **MECHANICAL DATA**

# D (R-PDSO-G\*\*)

# 8 PINS SHOWN

## PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-012

#### **IMPORTANT NOTICE**

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third—party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Copyright © 2003, Texas Instruments Incorporated