

## AGC AMPLIFIER

# **UPC3211GR**

#### **FEATURES**

- WIDE GAIN CONTROL RANGE: 55 dB (TYP)
- LOW DISTORTION:

IM3 = 57 dBc (TYP) at POUT = -10 dBmIM2 = 44 dBc (TYP) at POUT = -10 dBm

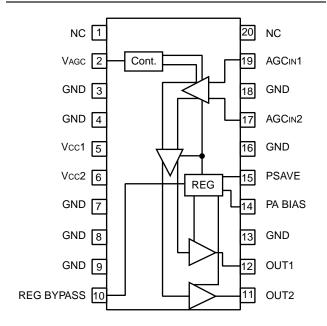
- SUPPLY VOLTAGE: 9 V
- PACKAGED IN 20 PIN SSOP SUITABLE FOR HIGH-DENSITY SURFACE MOUNT

#### **DESCRIPTION**

The UPC3211GR is a Silicon RFIC designed as an AGC amplifier for digital CATV return path applications. This IC consists of an AGC amplifier with 55 dB gain control range which is packaged in a 20 pin SSOP.

NEC's stringent quality assurance and test procedures ensure the highest reliability and performance.

### INTERNAL BLOCK DIAGRAM



### **ELECTRICAL CHARACTERISTICS** (TA = 25°C, VCC = 9 V, VAGC = 0 V, VPS = 9 V, unless otherwise specified)

PART NUMBER PACKAGE OUTLINE			UPC3211GR S20		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
Icc	Circuit Current (no input signal), VAGC = 0 V VAGC = 3 V	mA mA	29	38 43	51
ICC(PS)	Circuit Current in Power Save Mode (no input signal), VPs = 0 V <sup>1</sup>	mA		3	
Gмах	Maximum Gain <sup>2</sup>	dB	14	16	18
GCR	Gain Control Range <sup>2</sup> , VAGC = 0 to 3 V	dB	47	55	
GFLAT	Gain Flatness, fin = 5 to 100 MHz, 6 MHz Bandwidth	dB		±0.1	
PSAT	Saturated Output Power, PIN = -5 dBm	dBm		+5	
IsoL	Isolation in Sleep Mode, VPS = 0 V <sup>1</sup>	dB	60	65	
IM <sub>2</sub>	2nd Order Intermodulation Level, $f_{IN1} = 65$ MHz, $f_{IN2} = 66.8$ MHz, $P_{OUT} = -10$ dBm	dBc		44	40
IМз	3rd Order Intermodulation Level, fin1 = 65 MHz, fin2 = 66.8 MHz, POUT = -10 dBm	dBc		57	50
NF	Noise Figure, fin = 65 MHz	dB		10	
OIP3	Output 3rd Order Intercept Point, fIN1 = 65 MHz, fIN2 = 66.8 MHz	dBm		+16	
TPS (RISE)	Power Save Rise Time, $VPS(OFF) \rightarrow VPS(ON)$	μs		200	
TPS (FALL)	Power Save Fall Time, $VPS(ON) \rightarrow VPS(OFF)$	mS		1.7	

#### Notes:

- 1. Bias VPs through a 5  $k\Omega$  Resistor.
- 2. fin = 65 MHz, Pin = -20 dBm.

### ABSOLUTE MAXIMUM RATINGS<sup>1</sup> (TA = 25°C)

SYMBOLS PARAMETERS		UNITS	RATINGS
Vcc	Supply Voltage	V	11.0
VPS	Power Save Voltage <sup>3</sup>	V	11.0
Vagc	AGC Control Voltage	V	3.6
PD	Power Dissipation <sup>2</sup>	mW	500
TA	Operating Ambient Temp.	°C	-40 to +75
TSTG Storage Temp. Range		°C	-55 to +150
PIN(MAX)	Maximum Input Level	dBm	+5

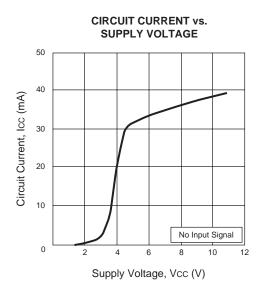
#### Notes:

- Operation in excess of any one of these conditions may result in permanent damage.
- 2. TA = 75°C Mounted on a 50x50x1.6 mm double epoxy glass board.
- 3. Bias VPs through 5 k  $\Omega$  resistor.

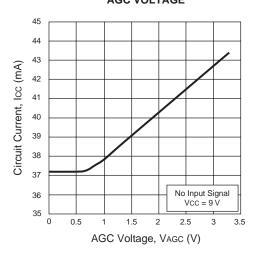
# RECOMMENDED OPERATING CONDITIONS

SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
Vcc	Supply Voltage	V	8.0	9.0	10.0
VPS	Power Save Voltage	V	0	-	10.0
VAGC	AGC Control Voltage	V	0	-	3.3
Та	Operating Ambient Temp.	°C	-40	+25	+75
fin	Input Frequency	MHz	5	-	100
PIN(MAX)	Maximum Input Level	dBm	-	-	0

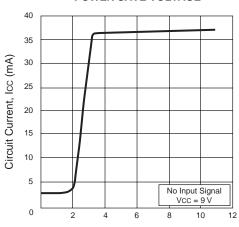
### TYPICAL PERFORMANCE CURVES (TA = 25°C)





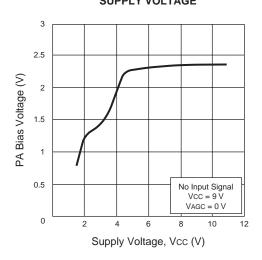


# CIRCUIT CURRENT vs. POWER SAVE VOLTAGE



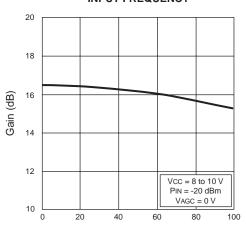
Power Save Voltage, VPS (V)

# PA BIAS VOLTAGE vs. SUPPLY VOLTAGE



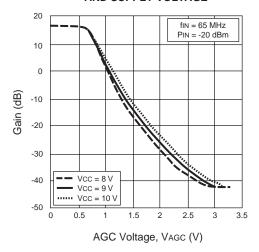
### TYPICAL PERFORMANCE CURVES (TA = 25°C)



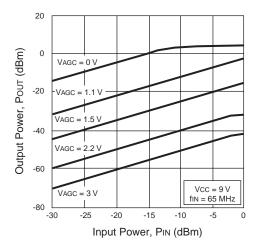


Input Frequency, fin (MHz)

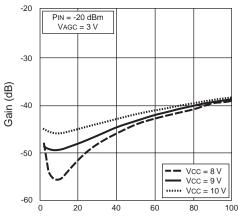
# GAIN vs. AGC VOLTAGE AND SUPPLY VOLTAGE



# OUTPUT POWER vs. INPUT POWER AND AGC VOLTAGE

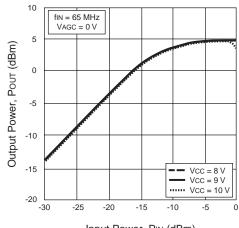


#### GAIN vs. INPUT FREQUENCY AND SUPPLY VOLTAGE



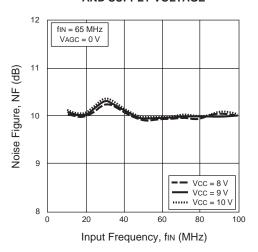
Input Frequency, fin (MHz)

# OUTPUT POWER vs. INPUT POWER AND SUPPLY VOLTAGE



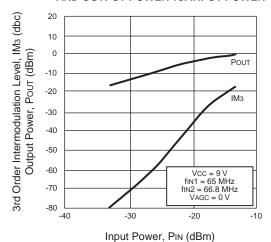
### Input Power, PIN (dBm)

# NOISE FIGURE vs. INPUT FREQUENCY AND SUPPLY VOLTAGE



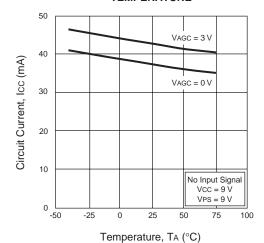
### STANDARD PERFORMANCE CURVES (TA = 25°C)

# 3RD ORDER INTERMODULATION LEVEL AND OUTPUT POWER vs. INPUT POWER

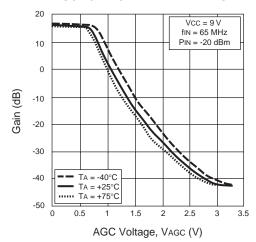


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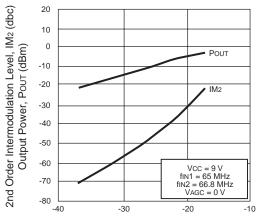
# CIRCUIT CURRENT vs. TEMPERATURE



# GAIN vs. AGC VOLTAGE AND TEMPERATURE

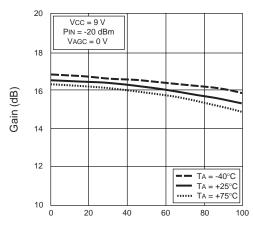


# 2ND ORDER INTERMODULATION LEVEL AND OUTPUT POWER vs. INPUT POWER



Input Power, PIN (dBm)

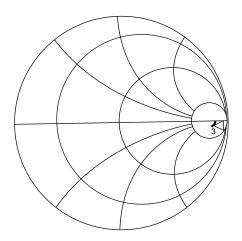
#### GAIN vs. INPUT FREQUENCY AND TEMPERATURE



Input Frequency, fin (MHz)

## STANDARD PERFORMANCE CURVES (TA = 25°C)

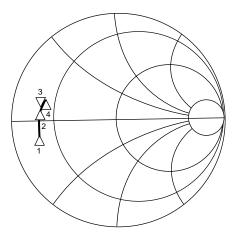
### **INPUT IMPEDANCE (PIN 19)**



 $\begin{array}{ccc} \text{Start 0.1 MHz} & \text{Stop 100 MHz} \\ \Delta \text{ 1: 5 MHz} & 533.6 \ \Omega & -16.4 \ \Omega \\ \Delta 2: 40 \ \text{MHz} & 515.2 \ \Omega & -81.4 \ \Omega \\ \Delta 3: 65 \ \text{MHz} & 493.7 \ \Omega & -123.3 \ \Omega \\ \Delta 4: 100 \ \text{MHz} & 455.9 \ \Omega & -190.3 \ \Omega \\ \end{array}$ 

TA = 25°C VCC = 9 V PIN = -20 dBm

#### **OUTPUT IMPEDANCE (PIN 11)**



#### Start 5 MHz Stop 100 MHz

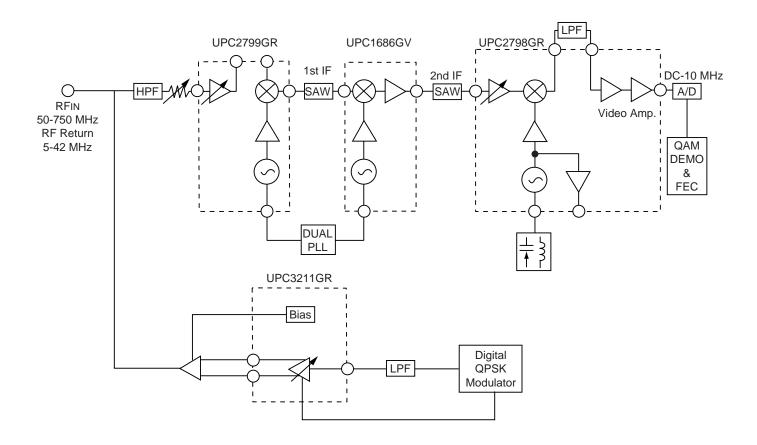
Δ 1: 5 MHz	$9.779 \Omega$	$-2.306 \Omega$
Δ 2: 40 MHz	$10.066 \Omega$	$3.033~\Omega$
Δ 3: 65 MHz	$10.574 \Omega$	$5.237 \Omega$
Δ 4: 100 MHz	$11.88 \Omega$	$7.805 \Omega$

TA = 25°C VCC = 9 V PIN = -20 dBm

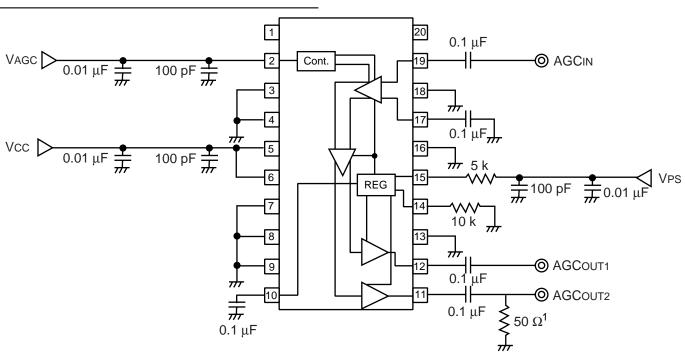
### **PIN FUNCTIONS**

Pin No.	Symbol	Pin Voltage (V)	Description	Equivalent Circuit
1	NC	_	No connection. This pin should be left open.	
2	Vagc	0 to 3	Automatic gain control pin. VAGC Up = Gain Down.	
3	GND	0	Differential amp ground pins. These pins must be connected to system ground. Form ground pattern as wide as possible to minimize ground impedance.	
5	Vcc1	9.0	Supply voltage pin for the AGC amp. This pin should be connected with a bypass capacitor to minimize ground impedance.	
6	Vcc2	9.0	Supply voltage pin for the differential amp and output block. This pin should be connected with a bypass capacitor to minimize ground impedance.	
7	GND	0	Differential amp ground pins. These pins must be	
8			connected to system ground. Form ground pattern as wide as possible to minimize ground	
9			impedance.	
10	REG BYPASS	1.64	Bypass pin of regulator block. This pin should be bypassed to ground through a capacitor.	6
11	OUT2	6.9	Signal output pins. These are emitter-follower outputs, which feature low impedance. In case of	11)(12)
12	OUT1	6.9	single-ended output, the unused pin should be connected to ground through a load resistor.	**************************************
13	GND	0	Output block ground pin. This pin must be connected to system ground. Form ground pattern as wide as possible to minimize ground impedance.	
14	PA_BIAS	2.45	This pin provides the base bias voltage to transistors configured as a power amplifier.	<u> </u>
15	Vps	9.0	Power save control pin can control the On/Sleep state with bias as follows:	VPS \
16	GND	0	AGC amp ground pin. This pin must be connected	
18			to system ground. Form ground pattern as wide as possible to minimize ground impedance.	
17	AGCIN2	2.43	Signal input pins. In the case of single-ended input, bypass the unused pin to ground through a capacitor.	5
19	AGCIN1	2.43		19 W 17
20	NC	_	No connection. This pin should be left open.	

### TYPICAL APPLICATION



### **MEASUREMENT CIRCUIT**

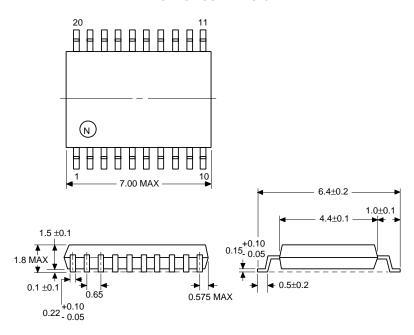


Note:

1. The pin that is not connected to the 50  $\Omega$  test system should be grounded through a 50  $\Omega$  resistor.

### PACKAGE DIMENSIONS (Units in mm)

#### **PACKAGE OUTLINE S20**



Note:

1. All dimensions are typical unless otherwise specified.

### **ORDERING INFORMATION**

PART NUMBER	QUANTITY
UPC3211GR-E1	2.5 k/Reel

Notes:

Embossed tape, 12 mm wide. Pin 1 indicates pull-out direction of