VR5432

64-Bit MIPS® RISC Microprocessor

Description

The VR5432ä microprocessor brings a new level of high-end performance to low-cost embedded design. This member of NEC's VR Seriesä microprocessors operates at either 167 or 200 MHz and uses a gated clock, minimal switching techniques, and a special circuit design to keep power consumption low. Its symmetric dual-issue pipeline with six independent execution units executes any combination of arithmetic logic unit (ALU), floating-point, or rotate instructions, while 32 KB instruction and data caches implement cache line locking to keep critical code and data cached. Multiple outstanding read transactions allow both caches to be filled concurrently, keeping the processor supplied with a steady stream of instructions and data. Mapping of accesses to virtual memory addresses is optimized with a 48-double-entry joint instruction/data translation lookaside buffer (TLB) and two separate four-entry micro TLBs for instructions and data.

Applications

Digital set-top boxes, Internet appliances, and office automation equipment

Features

- Dual-issue superscalar pipeline with six independent units
- Separate 32 KB two-way, set-associative instruction and data caches with cache line locking and parity
- Two unified 64-bit integer/floating-point units, each with 64-bit barrel shifters
- High-speed operating frequency
  - ¾ 316 Dhrystone MIPS at 167 MHz
  - ¾ 377 Dhrystone MIPS at 200 MHz
- 32-bit system bus
  - ¾ 83 MHz SysAD bus speed at 167 MHz
  - ¾ 100 MHz SysAD bus speed at 200 MHz
- On-chip debugging via JTAG, N-wire and N-trace functions
- Low power consumption
  - ¾ 1.8 watts at 167 MHz (typ.)
  - ¾ 2.1 watts at 200 MHz (typ.)
- 64-bit architecture with a 32-bit multiplexed address/data bus interface
- MIPS IV-compliant instruction set architecture
- MIPS architecture extensions
  - ¾ Integer multiply-accumulate instructions and other register-based multiply variations for fast DSP support
  - ¾ Integer rotate instructions for fast 32-bit and 64-bit string operations
  - ¾ Packed data vector operations for fast 8 x 8-bit image and multimedia processing
  - ¾ Cache line locking instructions (both caches) for better cache management

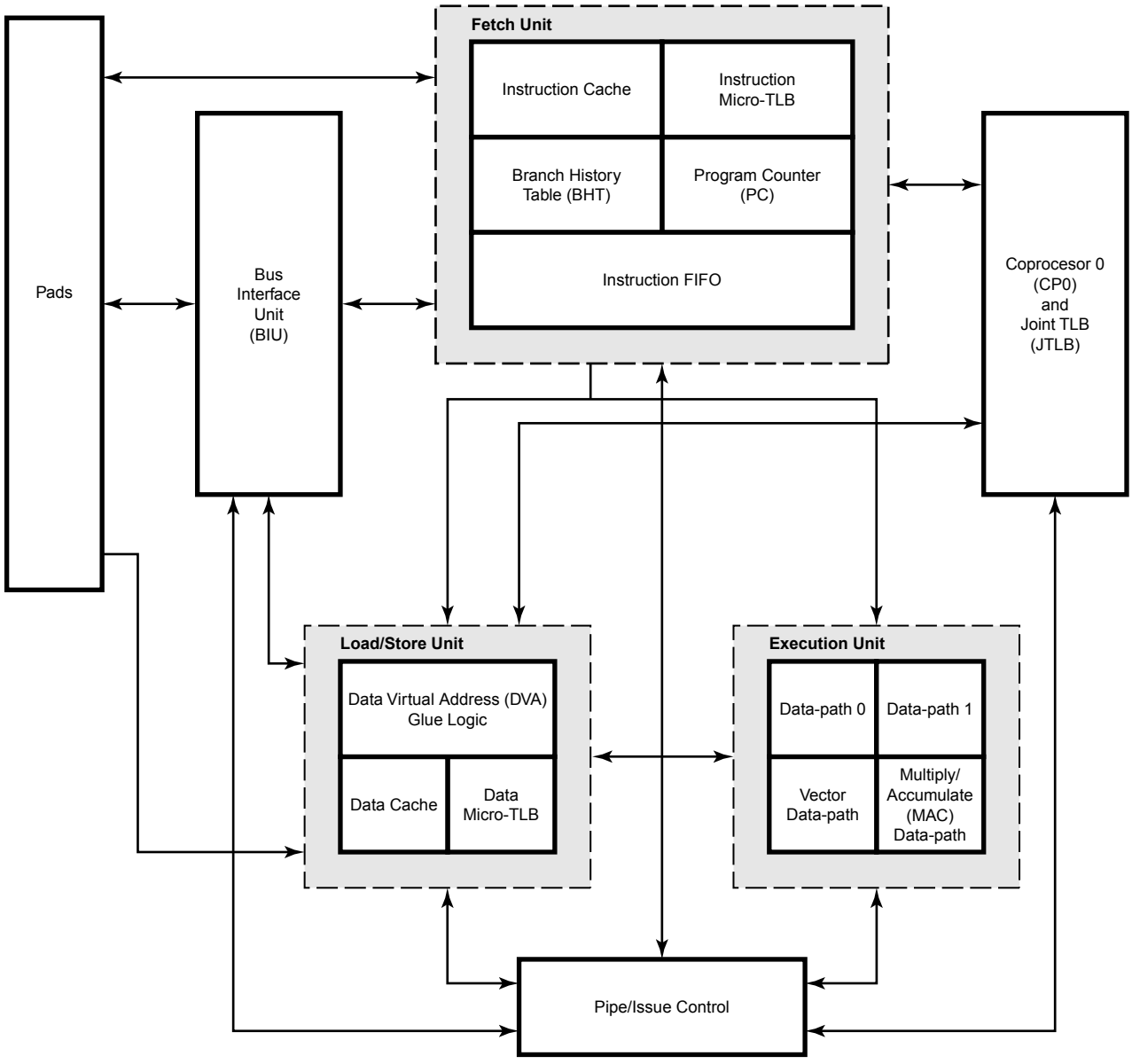
Ordering Information

Device No.	Operating Frequency (Max.)	Package
µPD30541GD-167-WML	167 MHz	208-pin PQFP
µPD30541GD-200-WML	200 MHz	208-pin PQFP

Family Comparison

Description	VR4300™	VR5000™	VR5432
Instruction set architecture	MIPS III	MIPS IV	MIPS IV
			Rotate instructions
			DSP (integer MAC)
			Multimedia
Pipeline	Scalar	Limited two-way superscalar issue	Symmetric two-way superscalar issue
Execution units	Single-issue	Integer and floating-point	Two integer + floating-point + barrel shifter
	Floating-point		Multiply-accumulate
			Packed data vector
			Load/store
			Branch
Load/store architecture	Blocking	Blocking	Nonblocking (hits under misses)
			Up to four outstanding data cache misses
Instruction cache size	16 KB	32 KB	32 KB
Data cache size	8 KB	32 KB	32 KB
Instruction TLB	Two-entry	Two-entry	Four-entry
	4 KB fixed page size	4 KB fixed page size	Variable page sizes
Data TLB	None	Two-entry	Four-entry
		4 KB fixed page size	Variable page sizes
Hardware debugging features	JTAG	None	JTAG
			N-wire
			N-trace
			Hardware and software breakpoints
			Instruction jamming
Performance counters for software tuning	None	None	Two 32-bit counters; any 2 of 16 events selectable

Block Diagram



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