NEC

MOS INTEGRATED CIRCUIT

μPD44164085, 44164185, 44164365

18M-BIT CMOS SYNCHRONOUS FAST SRAM DOUBLE DATA RATE SEPARATE I/O 2-WORD BURST OPERATION

Description

The μPD44164085 is a 2,097,152-word by 8-bit, the μPD44164185 is a 1,048,576-word by 18-bit and the μPD44164365 is a 524,288-word by 36-bit synchronous double data rate static RAM fabricated with advanced CMOS technology using full CMOS six-transistor memory cell.

The μPD44164085 and μPD44164185 integrates unique synchronous peripheral circuitry and a burst counter. All input registers controlled by an input clock pair (K and /K) and are latched on the positive edge of K and /K.

These products are suitable for applications which require synchronous operation, high speed, low voltage, high density and wide bit configuration.

These products are packaged in 165-pin PLASTIC FBGA package.

Features

- 1.8 ± 0.1 V power supply and HSTL I/O
- DLL circuitry for wide output data valid window and future frequency scaling
- Separate independent read and write data ports
- DDR read or write operation initiated each cycle
- Pipelined double data rate operation
- Separate data input/output bus
- Two-tick burst for low DDR transaction size
- Two input clocks (K and /K) for precise DDR timing at clock rising edges only
- Two output clocks (C and /C) for precise flight time and clock skew matching-clock and data delivered together to receiving device
- Internally self-timed write control
- Clock-stop capability with μs restart
- User programmable impedence output
- Fast clock cycle time : 3.0 ns (333 MHz), 3.3 ns (300 MHz), 4.0 ns (250 MHz) , 5.0 ns (200 MHz) , 6.0 ns (167 MHz)
- Simple control logic for easy depth expansion
- JTAG boundary scan

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Ordering Information

Part number	Cycle Time ns	Clock Frequency MHz	Organization (word x bit)	Core Supply Voltage V	I/O Interface	Package
μPD44164085 Fx-E30-EQx	3.0	333	2 M x 8-bit	1.8 ± 0.1	HSTL	165-pin PLASTIC FBGA (13 x 15)
μPD44164085 Fx-E33-EQx	3.3	300				
μPD44164085 Fx-E40-EQx	4.0	250				
μPD44164085 Fx-E50-EQx	5.0	200				
μPD44164085 Fx-E60-EQx	6.0	167				
μPD44164185 Fx-E30-EQx	3.0	333	1 M x 18-bit			
μPD44164185 Fx-E33-EQx	3.3	300				
μPD44164185 Fx-E40-EQx	4.0	250				
μPD44164185 Fx-E50-EQx	5.0	200				
μPD44164185 Fx-E60-EQx	6.0	167				
μPD44164365 Fx-E30-EQx	3.0	333	512 K x 36-bit			
μPD44164365 Fx-E33-EQx	3.3	300				
μPD44164365 Fx-E40-EQx	4.0	250				
μPD44164365 Fx-E50-EQx	5.0	200				
μPD44164365 Fx-E60-EQx	6.0	167				

Remark "Fx" and "EQx" of part number are package specifications. However, these are not available.

Pin Configuration (Marking Side)

/××× indicates active low signal.

165-pin PLASTIC FBGA (13 x 15)
(Top View)
[μPD44164085Fx]

	1	2	3	4	5	6	7	8	9	10	11
A	/CQ	V_{SS}	Ax	R, /W	/NW1	/K	NC	/LD	Ax	V_{SS}	CQ
B	NC	NC	NC	Ax	NC	K	/NW0	Ax	NC	NC	Q3
C	NC	NC	NC	V_{SS}	Ax	Ax	Ax	V_{SS}	NC	NC	D3
D	NC	D4	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	Q4	$V_{DD}Q$	V_{SS}	V_{SS}	V_{SS}	$V_{DD}Q$	NC	D2	Q2
F	NC	NC	NC	$V_{DD}Q$	V_{DD}	V_{SS}	V_{DD}	$V_{DD}Q$	NC	NC	NC
G	NC	D5	Q5	$V_{DD}Q$	V_{DD}	V_{SS}	V_{DD}	$V_{DD}Q$	NC	NC	NC
H	/DLL	V_{REF}	$V_{DD}Q$	$V_{DD}Q$	V_{DD}	V_{SS}	V_{DD}	$V_{DD}Q$	$V_{DD}Q$	V_{REF}	ZQ
J	NC	NC	NC	$V_{DD}Q$	V_{DD}	V_{SS}	V_{DD}	$V_{DD}Q$	NC	Q1	D1
K	NC	NC	NC	$V_{DD}Q$	V_{DD}	V_{SS}	V_{DD}	$V_{DD}Q$	NC	NC	NC
L	NC	Q6	D6	$V_{DD}Q$	V_{SS}	V_{SS}	V_{SS}	$V_{DD}Q$	NC	NC	Q0
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D0
N	NC	D7	NC	V_{SS}	Ax	Ax	Ax	V_{SS}	NC	NC	NC
P	NC	NC	Q7	Ax	Ax	C	Ax	Ax	NC	NC	NC
R	TDO	TCK	Ax	Ax	Ax	/C	Ax	Ax	Ax	TMS	TDI

Ax	: Address inputs	TMS	: IEEE 1149.1 Test input
D0 to D7	: Data inputs	TDI	: IEEE 1149.1 Test input
Q0 to Q7	: Data outputs	TCK	: IEEE 1149.1 Clock input
/LD	: Synchronous load	TDO	: IEEE 1149.1 Test output
R , /W	: Read Write input	CQ ,/CQ	: Echo clock
/NW0, /NW1	: Nybble Write data select	V_{REF}	: HSTL input reference input
K, /K	: Input clock	V_{DD}	: Power Supply
C, /C	: Output clock	$V_{DD}Q$	: Power Supply
ZQ	: Output impedance matching	V_{SS}	: Ground
/DLL	: DLL disable	NC	: No connection

Remark Refer to **Package Drawing** for 1-pin index mark.

165-pin PLASTIC FBGA (13 x 15)
(Top View)
[μPD44164185Fx]

	1	2	3	4	5	6	7	8	9	10	11
A	/CQ	V_{SS}	NC	R, /W	/BW1	/K	NC	/LD	Ax	V_{SS}	CQ
B	NC	Q9	D9	Ax	NC	K	/BW0	Ax	NC	NC	Q8
C	NC	NC	D10	V_{SS}	Ax	Ax	Ax	V_{SS}	NC	Q7	D8
D	NC	D11	Q10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D7
E	NC	NC	Q11	$V_{DD}Q$	V_{SS}	V_{SS}	V_{SS}	$V_{DD}Q$	NC	D6	Q6
F	NC	Q12	D12	$V_{DD}Q$	V_{DD}	V_{SS}	V_{DD}	$V_{DD}Q$	NC	NC	Q5
G	NC	D13	Q13	$V_{DD}Q$	V_{DD}	V_{SS}	V_{DD}	$V_{DD}Q$	NC	NC	D5
H	/DLL	V_{REF}	$V_{DD}Q$	$V_{DD}Q$	V_{DD}	V_{SS}	V_{DD}	$V_{DD}Q$	$V_{DD}Q$	V_{REF}	ZQ
J	NC	NC	D14	$V_{DD}Q$	V_{DD}	V_{SS}	V_{DD}	$V_{DD}Q$	NC	Q4	D4
K	NC	NC	Q14	$V_{DD}Q$	V_{DD}	V_{SS}	V_{DD}	$V_{DD}Q$	NC	D3	Q3
L	NC	Q15	D15	$V_{DD}Q$	V_{SS}	V_{SS}	V_{SS}	$V_{DD}Q$	NC	NC	Q2
M	NC	NC	D16	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	Q1	D2
N	NC	D17	Q16	V_{SS}	Ax	Ax	Ax	V_{SS}	NC	NC	D1
P	NC	NC	Q17	Ax	Ax	C	Ax	Ax	NC	D0	Q0
R	TDO	TCK	Ax	Ax	Ax	/C	Ax	Ax	Ax	TMS	TDI

Ax : Address inputs
D0 to D17 : Data inputs
Q0 to Q17 : Data outputs
/LD : Synchronous load
R , /W : Read Write input
/BW0, /BW1 : Byte Write data select
K, /K : Input clock
C, /C : Output clock
ZQ : Output impedance matching
/DLL : DLL disable
TMS : IEEE 1149.1 Test input
TDI : IEEE 1149.1 Test input
TCK : IEEE 1149.1 Clock input
TDO : IEEE 1149.1 Test output
CQ ,/CQ : Echo clock
V_{REF} : HSTL input reference input
V_{DD} : Power Supply
$V_{DD}Q$: Power Supply
V_{SS} : Ground
NC : No connection

Remark Refer to **Package Drawing** for 1-pin index mark.

165-pin PLASTIC FBGA (13 x 15)

(Top View)

[μPD44164365Fx]

	1	2	3	4	5	6	7	8	9	10	11
A	/CQ	V_{SS}	NC	R, /W	/BW2	/K	/BW1	/LD	NC	V_{SS}	CQ
B	Q27	Q18	D18	Ax	/BW3	K	/BW0	Ax	D17	Q17	Q8
C	D27	Q28	D19	V_{SS}	Ax	Ax	Ax	V_{SS}	D16	Q7	D8
D	D28	D20	Q19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q16	D15	D7
E	Q29	D29	Q20	$V_{DD}Q$	V_{SS}	V_{SS}	V_{SS}	$V_{DD}Q$	Q15	D6	Q6
F	Q30	Q21	D21	$V_{DD}Q$	V_{DD}	V_{SS}	V_{DD}	$V_{DD}Q$	D14	Q14	Q5
G	D30	D22	Q22	$V_{DD}Q$	V_{DD}	V_{SS}	V_{DD}	$V_{DD}Q$	Q13	D13	D5
H	/DLL	V_{REF}	$V_{DD}Q$	$V_{DD}Q$	V_{DD}	V_{SS}	V_{DD}	$V_{DD}Q$	$V_{DD}Q$	V_{REF}	ZQ
J	D31	Q31	D23	$V_{DD}Q$	V_{DD}	V_{SS}	V_{DD}	$V_{DD}Q$	D12	Q4	D4
K	Q32	D32	Q23	$V_{DD}Q$	V_{DD}	V_{SS}	V_{DD}	$V_{DD}Q$	Q12	D3	Q3
L	Q33	Q24	D24	$V_{DD}Q$	V_{SS}	V_{SS}	V_{SS}	$V_{DD}Q$	D11	Q11	Q2
M	D33	Q34	D25	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D10	Q1	D2
N	D34	D26	Q25	V_{SS}	Ax	Ax	Ax	V_{SS}	Q10	D9	D1
P	Q35	D35	Q26	Ax	Ax	C	Ax	Ax	Q9	D0	Q0
R	TDO	TCK	Ax	Ax	Ax	/C	Ax	Ax	Ax	TMS	TDI

Ax	: Address inputs	TMS	: IEEE 1149.1 Test input
D0 to D35	: Data inputs	TDI	: IEEE 1149.1 Test input
Q0 to Q35	: Data outputs	TCK	: IEEE 1149.1 Clock input
/LD	: Synchronous load	TDO	: IEEE 1149.1 Test output
R , /W	: Read Write input	CQ ,/CQ	: Echo clock
/BW0 to /BW3	: Byte Write data select	V_{REF}	: HSTL input reference input
K, /K	: Input clock	V_{DD}	: Power Supply
C, /C	: Output clock	$V_{DD}Q$	: Power Supply
ZQ	: Output impedance matching	V_{SS}	: Ground
/DLL	: DLL disable	NC	: No connection

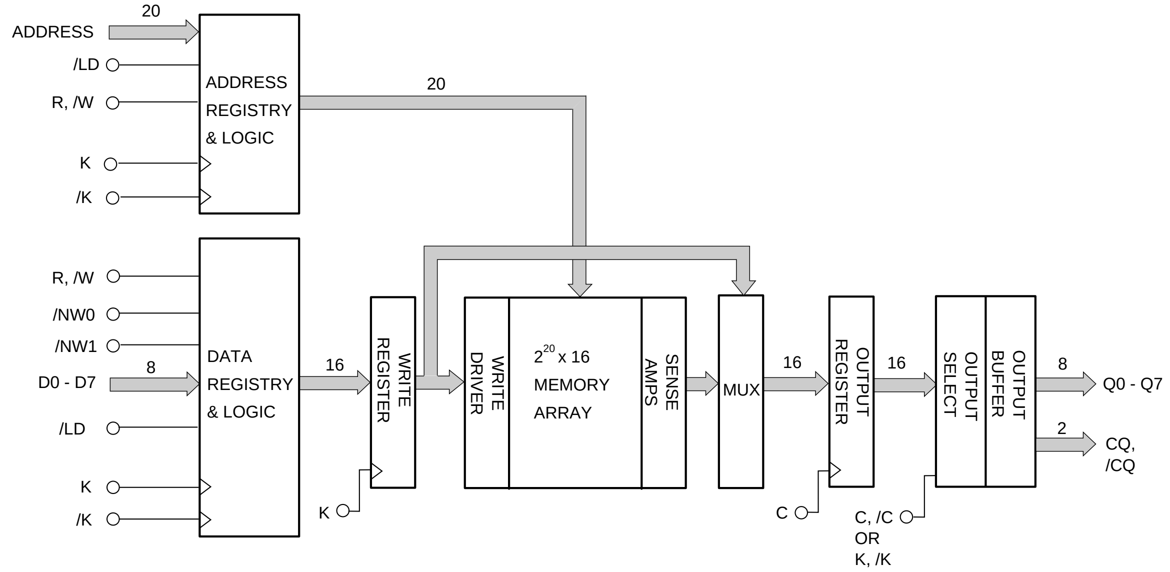
Remark Refer to **Package Drawing** for 1-pin index mark.

Pin Identification

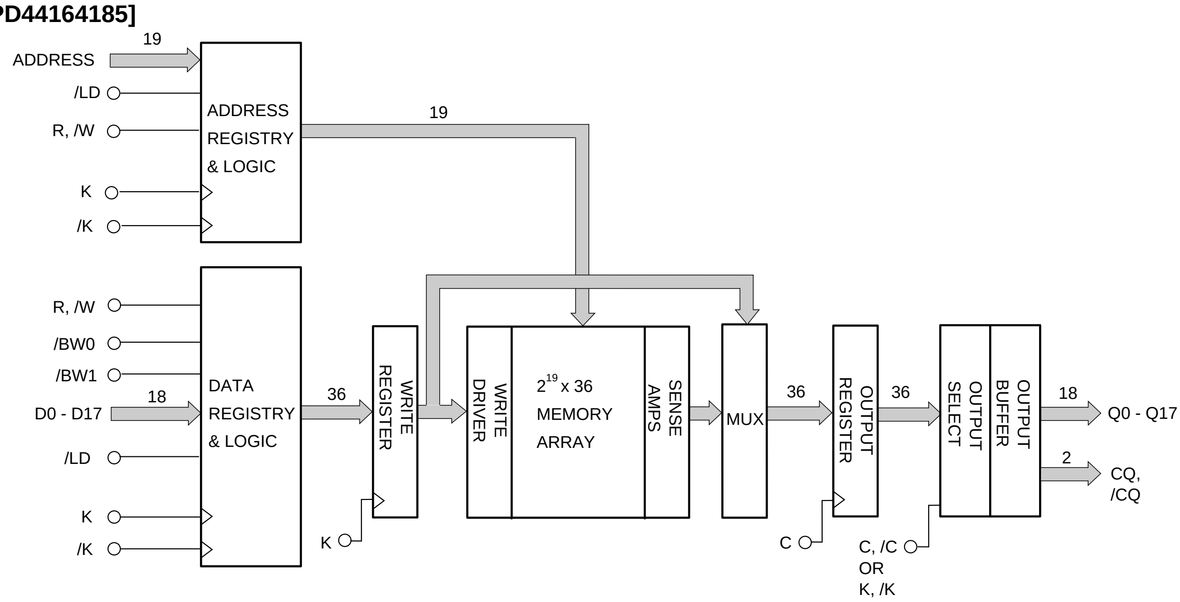
Symbol	Description
Ax	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of K. Balls 9A, 3A, 10A, and 2A are reserved for the next higher-order address inputs on future devices. All transactions operate on a burst of two words (one clock period of bus activity). These inputs are ignored when device is deselected.
/LD	Synchronous Load: This input is brought LOW when a bus cycle sequence is to be defined. This definition includes address and read/write direction. All transactions operate on a burst of 2 data (one clock periods of bus activity).
R , /W	Synchronous Read/Write Input: When /LD is LOW, this input designates the access type (READ when /R,W is HIGH, WRITE when /R,W is LOW) for the loaded address. /R,W must meet the setup and hold times around the rising edge of K.
/NWx /BWx	Synchronous Byte Writes (Nybble Writes on x8): When LOW these inputs cause their respective byte or nybble to be registered and written during WRITE cycles. These signals must meet setup and hold times around the rising edges of K and /K for each of the two rising edges comprising the WRITE cycle. See pin assignment figures for signal to data relationships.
K , /K	Input Clock: This input clock pair registers address and control inputs on the rising edge of K, and registers data on the rising edge of K and the rising edge of /K. /K is ideally 180 degrees out of phase with K. All synchronous inputs must meet setup and hold times around the clock rising edges.
C , /C	Output Clock: This clock pair provides a user controlled means of tuning device output data. The rising edge of C is used as the output timing reference for first output data. The rising edge of /C is used as the output reference for second output data. Ideally, /C is 180 degrees out of phase with C. C and /C may be tied HIGH to force the use of K and /K as the output reference clocks instead of having to provide C and /C clocks. If tied HIGH, C and /C must remain HIGH and not be toggled during device operation.
/DLL	DLL Disable: When LOW, this input causes the DLL to be bypassed for stable low frequency operation.
ZQ	Output Impedance Matching Input: This input is used to tune the device outputs to the system data bus impedance. DQ and CQ output impedance are set to 0.2 x RQ, where RQ is a resistor from this bump to ground. Alternately, this pin can be connected directly to V_{DD}, which enables the minimum impedance mode. This pin cannot be connected directly to GND or left unconnected.
TMS TDI	IEEE 1149.1 Test Inputs: 1.8V I/O levels. These balls may be left Not Connected if the JTAG function is not used in the circuit.
TCK	IEEE 1149.1 Clock Input: 1.8V I/O levels. This pin must be tied to V_{SS} if the JTAG function is not used in the circuit.
V_{REF}	HSTL Input Reference Voltage: Nominally $V_{DD}Q/2$. Provides a reference voltage for the input buffers.
D0 to Dxx	Synchronous Data Inputs: Input data must meet setup and hold times around the rising edges of K and K# during WRITE operations. See pin assignment figures for ball site location of individual signals. x8 device uses D0-D7. Remaining signals are NC. x18 device uses D0-D17. Remaining signals are NC. x36 device uses D0-D35. NC signals are read in the JTAG scan chain as the logic level applied to the ball site.
CQ, /CQ	Synchronous Echo Clock Outputs. The rising edges of these outputs are tightly matched to the synchronous data outputs and can be used as a data valid indication. These signals run freely and do not stop when Q tristates.
TDO	IEEE 1149.1 Test Output: 1.8V I/O level.
Q0 to Qxx	Synchronous Data Outputs: Output data is synchronized to the respective C and /C or to K and /K rising edges if C and /C are tied HIGH. This bus operates in response to /R commands. See pin assignment figures for ball site location of individual signals. x8 device uses Q0-Q7. Remaining signals are NC. x18 device uses Q0-Q17. Remaining signals are NC. x36 device uses Q0-Q35. NC signals are read in the JTAG scan chain as the logic level applied to the ball site.
V_{DD}	Power Supply: 1.8V nominal. See DC Electrical Characteristics and Operating Conditions for range.
$V_{DD}Q$	Power Supply: Isolated Output Buffer Supply. Nominally 1.5V. 1.8V is also permissible. See DC Electrical Characteristics and Operating Conditions for range.
V_{SS}	Power Supply: Ground
NC	No Connect: These signals are internally connected and appear in the JTAG scan chain as the logic level applied to the ball sites. These signals may be connected to ground to improve package heat dissipation.

Block Diagram

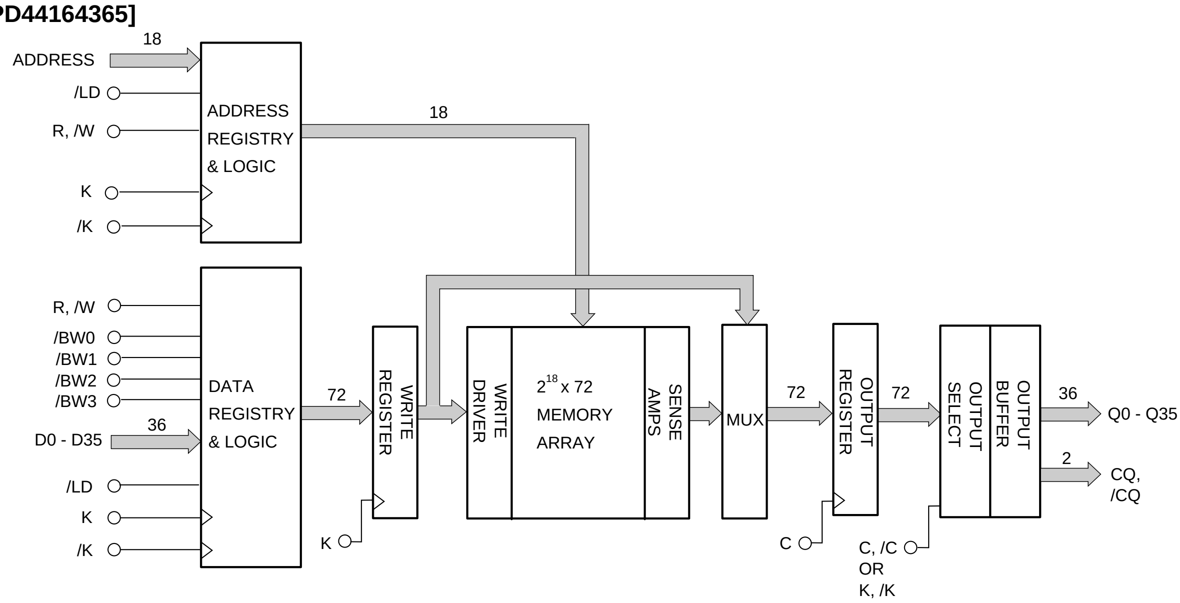
[μPD44164085]



[μPD44164185]



[μPD44164365]



Truth Table

Operation	/LD	R, /W	CLK	D or Q		
WRITE cycle Load address, input write data on two consecutive K and /K rising edge	L	L	L → H	Data in		
				Input data	D(A+0)	D(A+1)
				Input clock	K(t+1) ↑	/K(t+1) ↑
READ cycle Load address, read data on two consecutive C and /C rising edge	L	H	L → H	Data out		
				Output data	Q(A+0)	Q(A+1)
				Output clock	/C(t+1) ↑	C(t+2) ↑
NOP (No operation)	H	X	L → H	Hi-Z		
STANDBY(Clock stopped)	X	X	Stopped	Previous state		

Remarks 1. H : High level , L : Low level , × : don't care, ↑ : rising edge.

2. Data inputs are registered at K and /K rising edges. Data outputs are delivered at C and /C rising edges except if C and /C are HIGH then Data outputs are delivered at K and /K rising edges.

3. All control inputs in the truth table must meet setup/hold times around the rising edge (LOW to HIGH) of K. All control inputs are registered during the rising edge of K.

4. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.

5. Refer to state diagram and timing diagrams for clarification.

6. It is recommended that K = /K = C = /C when clock is stopped. This is not essential but permits most rapid restart by overcoming transmission line charging symmetrically.

Byte Write Operation

[μPD44164085]

Operation	K	/K	/NW0	/NW1
Write D0-7	L → H	–	0	0
	–	L → H	0	0
Write D0-3	L → H	–	0	1
	–	L → H	0	1
Write D4-7	L → H	–	1	0
	–	L → H	1	0
Write nothing	L → H	–	1	1
	–	L → H	1	1

Remark H : High level , L : Low level , → : rising edge.

[μPD44164185]

Operation	K	/K	/BW0	/BW1
Write D0-17	L → H	–	0	0
	–	L → H	0	0
Write D0-8	L → H	–	0	1
	–	L → H	0	1
Write D9-17	L → H	–	1	0
	–	L → H	1	0
Write nothing	L → H	–	1	1
	–	L → H	1	1

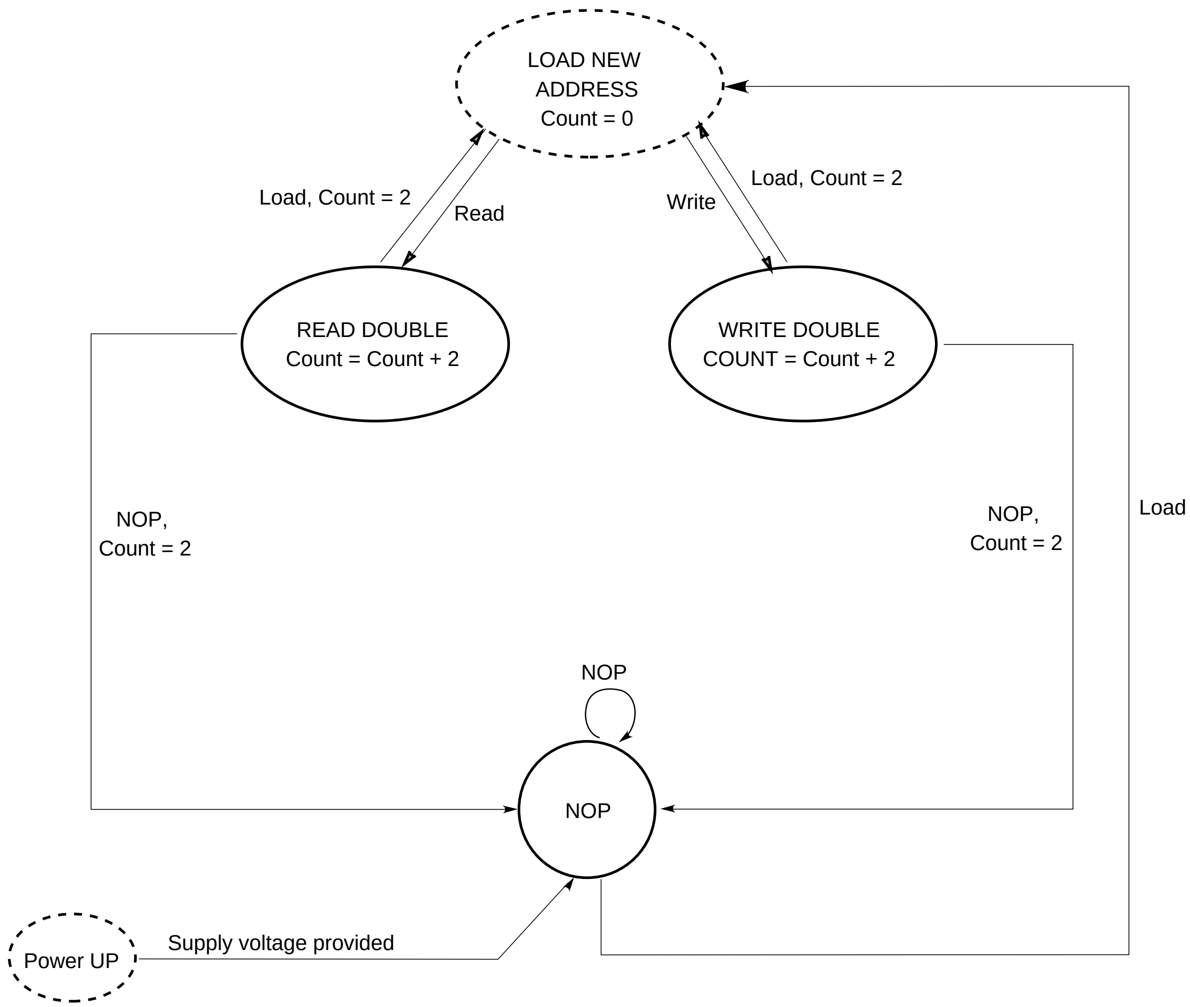
Remark H : High level , L : Low level , → : rising edge.

[μPD44164365]

Operation	K	/K	/BW0	/BW1	/BW2	/BW3
Write D0-35	L → H	–	0	0	0	0
	–	L → H	0	0	0	0
Write D0-8	L → H	–	0	1	1	1
	–	L → H	0	1	1	1
Write D9-17	L → H	–	1	0	1	1
	–	L → H	1	0	1	1
Write D18-26	L → H	–	1	1	0	1
	–	L → H	1	1	0	1
Write D27-35	L → H	–	1	1	1	0
	–	L → H	1	1	1	0
Write nothing	L → H	–	1	1	1	1
	–	L → H	1	1	1	1

Remark H : High level , L : Low level , → : rising edge.

Bus Cycle State Diagram



Remark State machine control timing sequence is controlled by K.

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		–0.5		+2.9	V
Output supply voltage	$V_{DD}Q$		–0.5		V_{DD}	V
Input voltage	V_{IN}		–0.5		V_{DD} + 0.5 (2.9 V MAX.)	V
Input / Output voltage	$V_{I/O}$		–0.5		$V_{DD}Q$ + 0.5 (2.9 V MAX.)	V
Junction temperature	T_j				+125	°C
Storage temperature	T_{stg}		–55		+125	°C

Caution **Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.**

Recommended DC Operating Conditions (T_j = 20 to 110 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V_{DD}		1.7		1.9	V	
Output supply voltage	$V_{DD}Q$		1.4		V_{DD}	V	
High level input voltage	V_{IH}		V_{REF} + 0.1		$V_{DD}Q$ + 0.3	V	1
Low level input voltage	V_{IL}		–0.3		V_{REF} – 0.1	V	1
Clock input voltage	V_{IN}		–0.3		$V_{DD}Q$ + 0.3	V	1
Reference voltage	V_{REF}		0.68		0.95	V	

Note1 Overshoot: $V_{IH (AC)} \leq V_{DD} + 0.7$ V for $t \leq t_{KHKH}/2$

Undershoot: $V_{IL (AC)} \geq -0.5$V for $t \leq t_{KHKH}/2$

Power-up: $V_{IH} \leq V_{DD}Q + 0.3$V and $V_{DD} \leq 1.7$V and $V_{DD}Q \leq 1.4$V for $t \leq 200$ ms

During normal operation, $V_{DD}Q$ must not exceed V_{DD}.

Control input signals may not have pulse widths less than $t_{KHKL(MIN)}$ or operate at cycle rates less than $t_{KHKH (MIN)}$.

Capacitance (T_A = 25 °C, f = 1MHz)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V		4	5	pF
Input / Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V		6	7	pF
Clock Input capacitance	C_{clk}	V_{clk} = 0 V		5	6	pF

Remark These parameters are periodically sampled and not 100% tested.

DC Characteristics (T_j = 20 to 110°C, V_{DD} = 1.8 ± 0.1 V)

Parameter	Symbol	Test condition		MIN.	TYP.	MAX.		Unit	Note
						x8, x18	x36		
Input leakage current	I_{LI}			–2	–	+2		μA	
I/O leakage current	I_{LO}			–2	–	+2		μA	
Operating supply current (Read Write cycle)	I_{DD}	$V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$, $I_{I/O}$ = 0 mA Cycle = MAX.	–E30			525	710	mA	
			–E33			475	640		
			–E40			400	545		
			–E50			330	445		
			–E60			280	380		
Standby supply current (NOP)	I_{SB1}	$V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$, $I_{I/O}$ = 0 mA Cycle = MAX.	–E30			255	265	mA	
			–E33			235	240		
			–E40			200	210		
			–E50			170	180		
			–E60			150	160		
High level output voltage	$V_{OH(Low)}$	$\lvert I_{OH}\rvert \leq$ 0.1 mA		$V_{DD}Q$ – 0.2	–	$V_{DD}Q$		V	3,4
	V_{OH}	Note1		$V_{DD}Q$/2–0.08	–	$V_{DD}Q$/2+0.08		V	3,4
Low level output voltage	$V_{OL(Low)}$	$I_{OL} \leq$ 0.1 mA		V_{SS}	–	0.2		V	3,4
	V_{OL}	Note2		$V_{DD}Q$/2–0.08	–	$V_{DD}Q$/2+0.08		V	3,4

Notes 1. Outputs are impedance-controlled. $\lvert I_{OH} \rvert$ = ($V_{DD}Q$/2)/(RQ/5) for values of 175 Ω ≤ RQ ≤ 350 Ω.

2. Outputs are impedance-controlled. I_{OL} = ($V_{DD}Q$/2)/(RQ/5) for values of 175 Ω ≤ RQ ≤ 350 Ω.

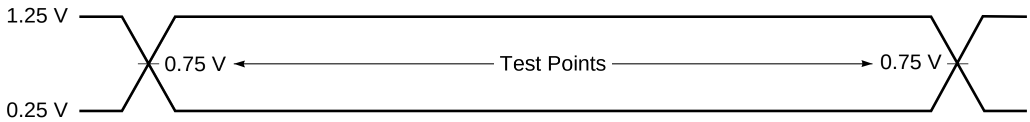
3. AC load current is higher than the shown DC values. AC I/O curves are available upon request.

4. HSTL outputs meet JEDEC HSTL Class I and Class II standards.

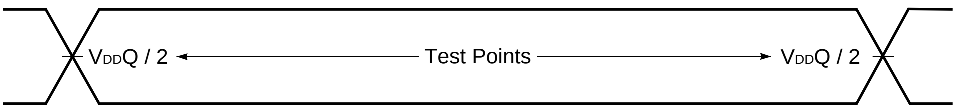
AC Characteristics (T_j = 20 °C to 110 °C, V_{DD} = 1.8 ± 0.1 V)

AC Test Conditions

Input waveform (Rise / Fall time ≤ 0.3 ns)

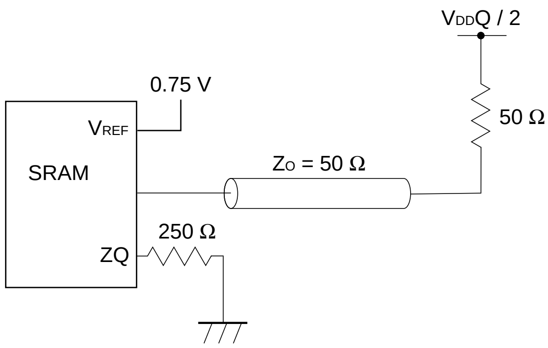


Output waveform



Output load condition

Figure 1. External load at test



Remark C_L includes capacitances of the probe and jig, and stray capacitances.

Read and Write Cycle

Parameter	Symbol	-E30 (333 MHz)		-E33 (300 MHz)		-E40 (250 MHz)		-E50 (200 MHz)		-E60 (167 MHz)		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Clock													
Average Clock cycle time (K, /K, C, /C)	TKHKH	3.0	3.6	3.3	4.0	4.0	5.0	5.0	6.0	6.0	7.5	ns	
Clock phase jitter (K, /K, C, /C)	TKC var	–	0.08	–	0.08	–	0.10	–	0.13	–	0.15	ns	
Clock HIGH time (K, /K, C, /C)	TKHKL	1.20	–	1.32	–	1.6	–	2.0	–	2.4	–	ns	
Clock LOW time (K, /K, C, /C)	TKLKH	1.20	–	1.32	–	1.6	–	2.0	–	2.4	–	ns	
Clock to /clock (K to /K., C→/C.)	TKH /KH	1.35	1.65	1.49	1.82	1.8	2.2	2.2	2.75	2.7	3.3	ns	
Clock to data clock (K→C., /K→/C.)	TKHCH	0	1.30	0	1.45	0	1.8	0	2.3	0	2.8	ns	
DLL lock time (K,C)	TKC lock	1,024	–	1,024	–	1,024	–	1,024	–	1,024	–	Cycle	2
K static to DLL reset	TKC reset	30	–	30	–	30	–	30	–	30	–	ns	
Output Times													
C, /C HIGH to output valid	TCHQV	–	0.27	–	0.29	–	0.35	–	0.38	–	0.40	ns	
C, /C HIGH to output hold	TCHQX	– 0.27	–	– 0.29	–	– 0.35	–	– 0.38	–	– 0.40	–	ns	
C, /C HIGH to echo clock valid	TCHCQV	–	0.25	–	0.27	–	0.33	–	0.36	–	0.38	ns	
C, /C HIGH to echo clock hold	TCHCQX	– 0.25	–	– 0.27	–	– 0.33	–	– 0.36	–	– 0.38	–	ns	
CQ, /CQ HIGH to output valid	TCQHQV	–	0.27	–	0.29	–	0.35	–	0.38	–	0.40	ns	
CQ, /CQ HIGH to output hold	TCQHQX	– 0.27	–	– 0.29	–	– 0.35	–	– 0.38	–	– 0.40	–	ns	
C HIGH to output High-Z	TCHQZ	–	0.27	–	0.29	–	0.35	–	0.38	–	0.40	ns	
C HIGH to output Low-Z	TCHQX1	– 0.27	–	– 0.29	–	– 0.35	–	– 0.38	–	– 0.40	–	ns	
Setup Times													
Address valid to K rising edge	TAVKH	0.4	–	0.4	–	0.4	–	0.6	–	0.7	–	ns	1
Control inputs valid to K rising edge	TIVKH	0.4	–	0.4	–	0.4	–	0.6	–	0.7	–	ns	1
Data-in valid to K, /K rising edge	TDVKH	0.4	–	0.4	–	0.4	–	0.6	–	0.7	–	ns	1
Hold Times													
K rising edge to address hold	TKHAX	0.4	–	0.4	–	0.4	–	0.6	–	0.7	–	ns	1
K rising edge to control inputs hold	TKHIX	0.4	–	0.4	–	0.4	–	0.6	–	0.7	–	ns	1
K, /K rising edge to data-in hold	TKHDX	0.4	–	0.4	–	0.4	–	0.6	–	0.7	–	ns	1

Notes 1. This is a synchronous device. All addresses, data and control lines must meet the specified setup and hold times for all latching clock edges.

2. V_{DD} slew rate must be less than 0.1 V DC per 50 ns for DLL lock retention. DLL lock time begins once V_{DD} and input clock are stable.

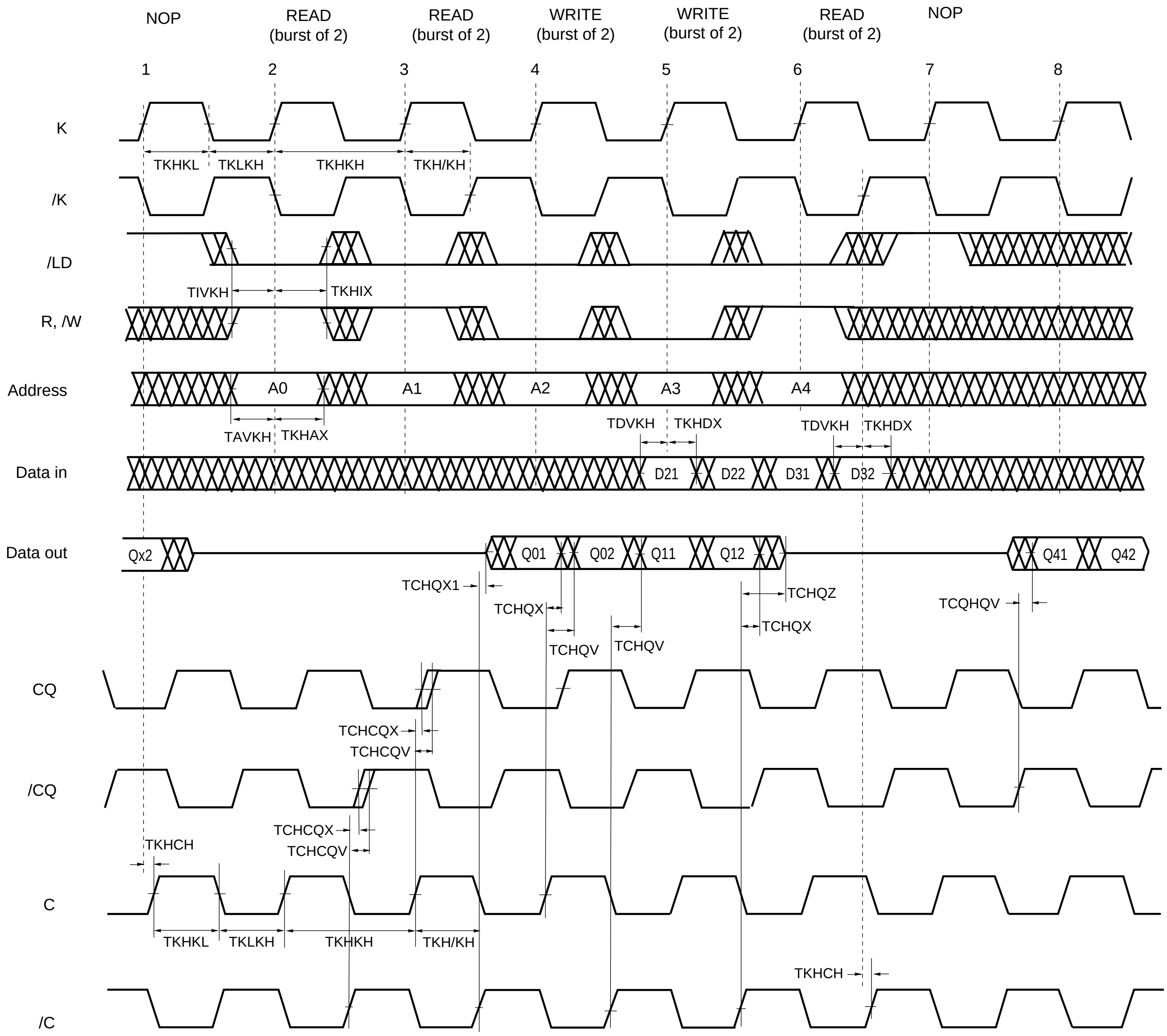
Remarks 1. This parameter is sampled.

2. Test conditions as specified with the output loading as shown in AC Test Conditions unless otherwise noted.

3. Control input signals may not be operated with pulse widths less than TKHKL (MIN).

4. If C, /C are tied HIGH, K, /K become the references for C, /C timing parameters.

Read and Write Timing



Remarks 1. Q01 refers to output from address A0+0.

Q02 refers to output from the next internal burst address following A0,i.e.,A0+1.

2. Outputs are disable (High-Z) one clock cycle after a NOP.

3. In this example, if address A3=A4, data Q41=D31, Q42=D32.

Write data is forwarded immediately as read results.

JTAG Specification

These products support a limited set of JTAG functions as in IEEE standard 1149.1.

Test Access Port (TAP) Pins

Pin name	Pin assignments	Description
TCK	2R	Test Clock Input. All input are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	10R	Test Mode Select. This is the command input for the TAP controller state machine.
TDI	11R	Test Data Input. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is deter-mined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction.
TDO	1R	Test Data Output. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

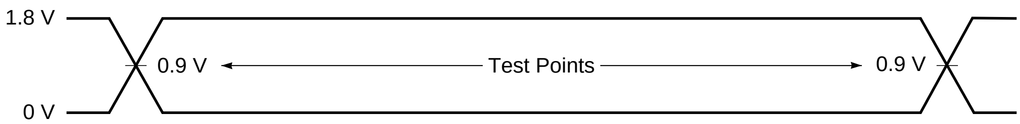
Remark The device does not have TRST (TAP reset). The Test-Logic Reset state is entered while TMS is held high for five rising edges of TCK. The TAP controller state is also reset on the SRAM POWER-UP.

JTAG DC Characteristics (20 °C ≤ Tj ≤ 110 °C, 1.7 V ≤ V_{DD} ≤ 1.9 V, unless otherwise noted)

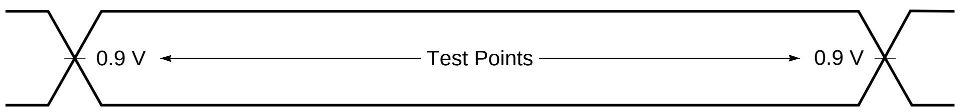
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
JTAG Input leakage current	I_{LI}	0 V ≤ V_{IN} ≤ V_{DD}	–5.0	–	+5.0	μA	
JTAG I/O leakage current	I_{LO}	0 V ≤ V_{IN} ≤ $V_{DD}Q$, Outputs disabled	–5.0	–	+5.0	μA	
JTAG input high voltage	V_{IH}		1.3	–	V_{DD}+0.3	V	
JTAG input low voltage	V_{IL}		–0.3	–	+0.5	V	
JTAG output high voltage	V_{OH1}	| I_{OHC} | = 100 μA	1.6	–	–	V	
	V_{OH2}	| I_{OHT} | = 2 mA	1.4	–	–	V	
JTAG output low voltage	V_{OL1}	I_{OLC} = 100 μA	–	–	0.2	V	
	V_{OL2}	I_{OLT} = 2 mA	–	–	0.4	V	

JTAG AC Test Conditions

Input waveform (Rise / Fall time ≤ 1 ns)

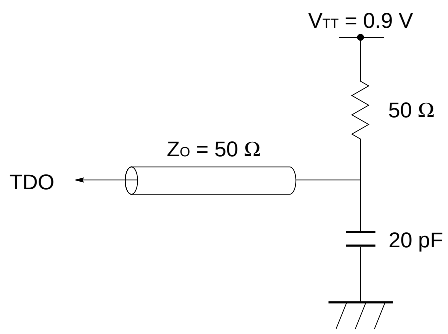


Output waveform



Output load

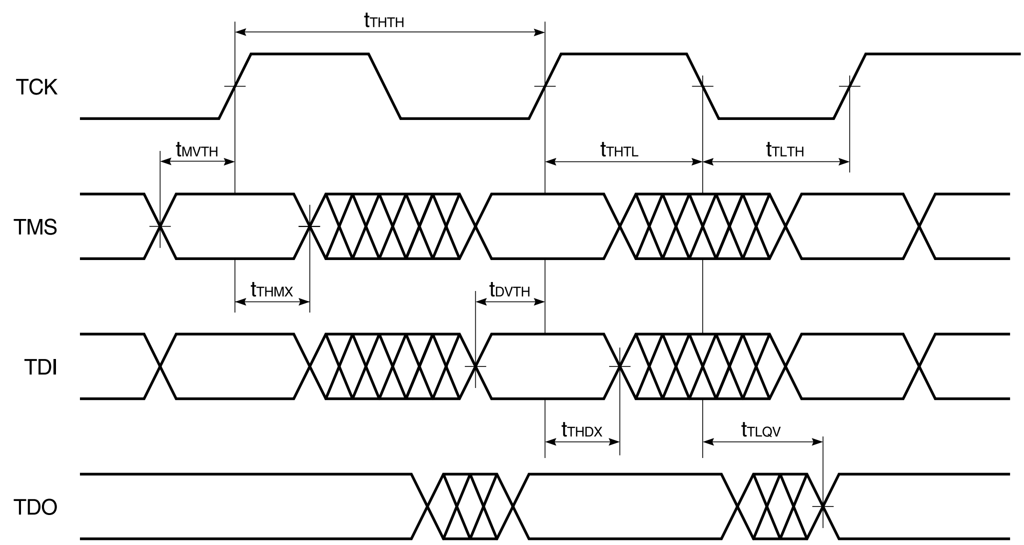
Figure 2. External load at test



JTAG AC Characteristics (T_j = 5 to 110 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Clock							
Clock cycle time	t_{THTH}		100	–	–	ns	
Clock frequency	f_{TF}		–	–	10	MHz	
Clock high time	t_{THTL}		40	–	–	ns	
Clock low time	t_{TLTH}		40	–	–	ns	
Output time							
TCK low to TDO unknown	t_{TLOX}		0	–	–	ns	
TCK low to TDO valid	t_{TLOV}		–	–	20	ns	
TDI valid to TCK high	t_{DVTH}		10	–	–	ns	
TCK high to TDI invalid	t_{THDX}		10	–	–	ns	
Setup time							
TMS setup time	t_{MVTH}		10	–	–	ns	
Capture setup time	t_{CS}		10	–	–	ns	
Hold time							
TDI hold time	t_{THMX}		10	–	–	ns	
Capture hold time	t_{CH}		10	–	–	ns	

JTAG Timing Diagram



Scan Register Definition (1)

Register name	Description
Instruction register	The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run-test/idle or the various data register state. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power-up whenever the controller is placed in test-logic-reset state.
Bypass register	The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.
ID register	The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture-DR state with the IDCODE command loaded in the instruction register. The register is then placed between the TDI and TDO pins when the controller is moved into shift-DR state.
Boundary register	The boundary register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to shift-DR state. Several TAP instructions can be used to activate the boundary register. The Scan Exit Order tables describe which device bump connects to each boundary register location. The first column defines the bit's position in the boundary register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the input or I/O at the bump and the third column is the bump number.

Scan Register Definition (2)

Register name		Unit
Instruction register	3	bit
Bypass register	1	bit
ID register	32	bit
Boundary register	107	bit

ID Register Definition

Part number	Organization	ID [31:28] vendor revision no.	ID [27:12] part no.	ID [11:1] vendor ID no.	ID [0] fix bit
μPD44164085	2M x 8	XXXX	0000 0000 0001 1000	00000010000	1
μPD44164185	1M x 18	XXXX	0000 0000 0001 1001	00000010000	1
μPD44164365	512K x 36	XXXX	0000 0000 0001 1010	00000010000	1

SCAN Exit Order

Bit no.	Signal name x8	x18	x36	Bump ID
1	/C			6R
2	C			6P
3	Ax			6N
4	Ax			7P
5	Ax			7N
6	Ax			7R
7	Ax			8R
8	Ax			8P
9	Ax			9R
10	NC	Q0	Q0	11P
11	NC	D0	D0	10P
12	NC	NC	D9	10N
13	NC	NC	Q9	9P
14	NC	Q1	Q1	10M
15	NC	D1	D1	11N
16	NC	NC	D10	9M
17	NC	NC	Q10	9N
18	Q0	Q2	Q2	11L
19	D0	D2	D2	11M
20	NC	NC	D11	9L
21	NC	NC	Q11	10L
22	NC	Q3	Q3	11K
23	NC	D3	D3	10K
24	NC	NC	D12	9J
25	NC	NC	Q12	9K
26	Q1	Q4	Q4	10J
27	D1	D4	D4	11J
28	ZQ			11H
29	NC	NC	D13	10G
30	NC	NC	Q13	9G
31	NC	Q5	Q5	11F
32	NC	D5	D5	11G
33	NC	NC	D14	9F
34	NC	NC	Q14	10F
35	Q2	Q6	Q6	11E
36	D2	D6	D6	10E

Bit no.	Signal name x8	x18	x36	Bump ID
37	NC	NC	D15	10D
38	NC	NC	Q15	9E
39	NC	Q7	Q7	10C
40	NC	D7	D7	11D
41	NC	NC	D16	9C
42	NC	NC	Q16	9D
43	Q3	Q8	Q8	11B
44	D3	D8	D8	11C
45	NC	NC	D17	9B
46	NC	NC	Q17	10B
47	CQ			11A
48	NC			10A
49	Ax	Ax	NC	9A
50	Ax			8B
51	Ax			7C
52	Ax			6C
53	/LD			8A
54	NC	NC	/BW1	7A
55	/NW0	/BW0	/BW0	7B
56	K			6B
57	/K			6A
58	NC	NC	/BW3	5B
59	/NW1	/BW1	/BW2	5A
60	R, /W			4A
61	Ax			5C
62	Ax			4B
63	Ax	NC	NC	3A
64	NC			2A
65	/CQ			1A
66	NC	Q9	Q18	2B
67	NC	D9	D18	3B
68	NC	NC	D27	1C
69	NC	NC	Q27	1B
70	NC	Q10	Q19	3D
71	NC	D10	D19	3C
72	NC	NC	D28	1D

Bit no.	Signal name x8	x18	x36	Bump ID
73	NC	NC	Q28	2C
74	Q4	Q11	Q20	3E
75	D4	D11	D20	2D
76	NC	NC	D29	2E
77	NC	NC	Q29	1E
78	NC	Q12	Q21	2F
79	NC	D12	D21	3F
80	NC	NC	D30	1G
81	NC	NC	Q30	1F
82	Q5	Q13	Q22	3G
83	D5	D13	D22	2G
84	NC	NC	D31	1J
85	NC	NC	Q31	2J
86	NC	Q14	Q23	3K
87	NC	D14	D23	3J
88	NC	NC	D32	2K
89	NC	NC	Q32	1K
90	Q6	Q15	Q24	2L
91	D6	D15	D24	3L
92	NC	NC	D33	1M
93	NC	NC	Q33	1L
94	NC	Q16	Q25	3N
95	NC	D16	D25	3M
96	NC	NC	D34	1N
97	NC	NC	Q34	2M
98	Q7	Q17	Q26	3P
99	D7	D17	D26	2N
100	NC	NC	D35	2P
101	NC	NC	Q35	1P
102	Ax			3R
103	Ax			4R
104	Ax			4P
105	Ax			5P
106	Ax			5N
107	Ax			5R

JTAG Instructions

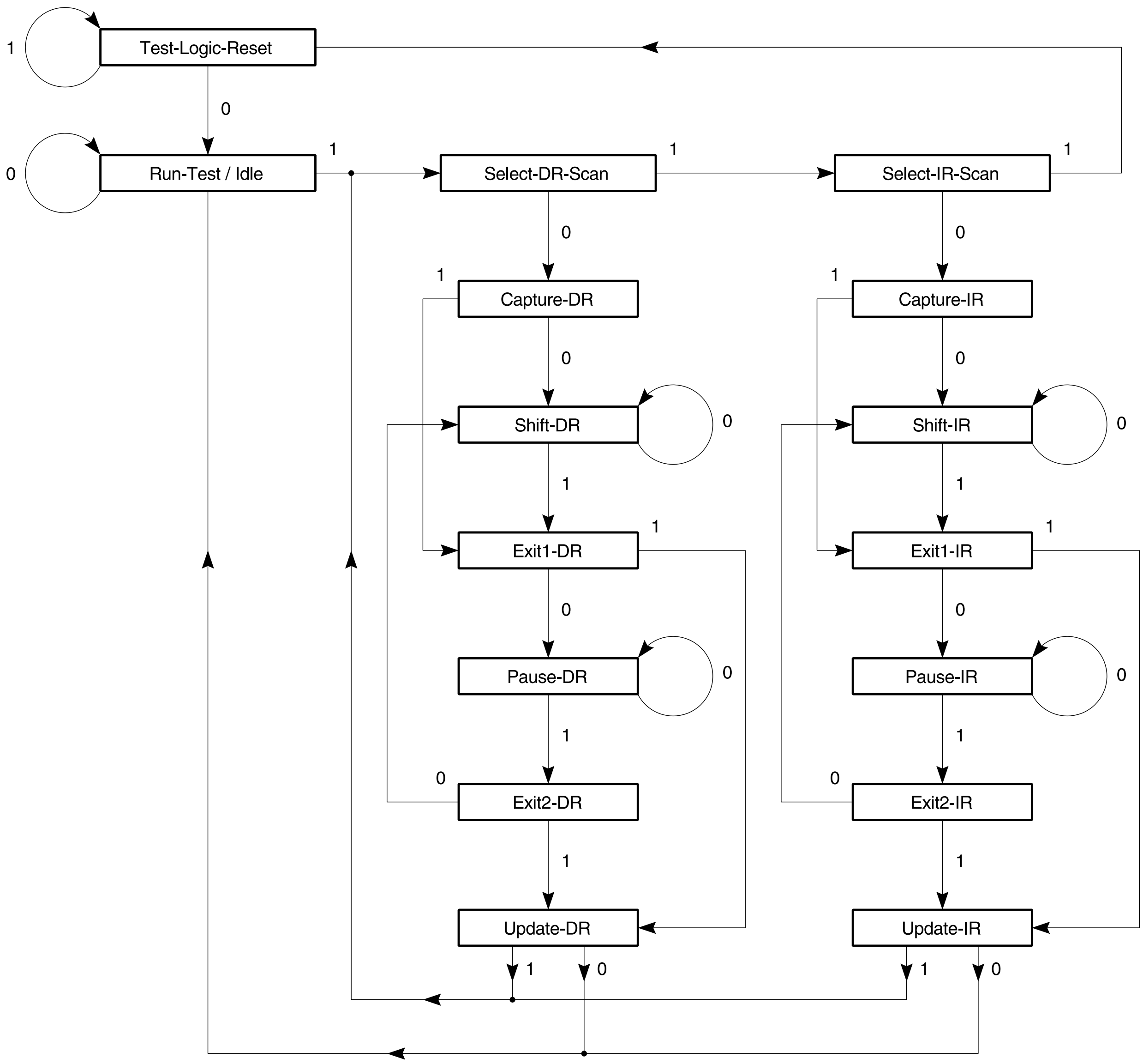
Instructions	Description
EXTEST	EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic 0s. EXTEST is not implemented in this device. Therefore this device is not 1149.1 compliant. Nevertheless, this RAMs TAP does respond to an all zeros instruction, as follows. With the EXTEST (000) instruction loaded in the instruction register the RAM responds just as it does in response to the SAMPLE instruction, except the RAM output are forced to Hi-Z any time the instruction is loaded.
IDCODE	The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture-DR mode and places the ID register between the TDI and TDO pins in shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test-logic-reset state.
BYPASS	The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.
SAMPLE	SAMPLE is a Standard 1149.1 mandatory public instruction. When the SAMPLE instruction is loaded in the instruction register, moving the TAP controller into the capture-DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e., in a metastable state). Although allowing the TAP to SAMPLE metastable input will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture setup plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register. Moving the controller to shift-DR state then places the boundary scan register between the TDI and TDO pins. This functionality is not Standard 1149.1 compliant.
SAMPLE-Z	If the SAMPLE-Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (Hi-Z) and the boundary register is connected between TDI and TDO when the TAP controller is moved to the shift-DR state.

JTAG Instruction Coding

IR2	IR1	IR0	Instruction	Note
0	0	0	EXTEST	1
0	0	1	IDCODE	
0	1	0	SAMPLE-Z	1
0	1	1	RESERVED	
1	0	0	SAMPLE	
1	0	1	RESERVED	
1	1	0	RESERVED	
1	1	1	BYPASS	

Note 1. TRISTATE all data drivers and CAPTURE the pad values into a SERIAL SCAN LATCH.

TAP Controller State Diagram



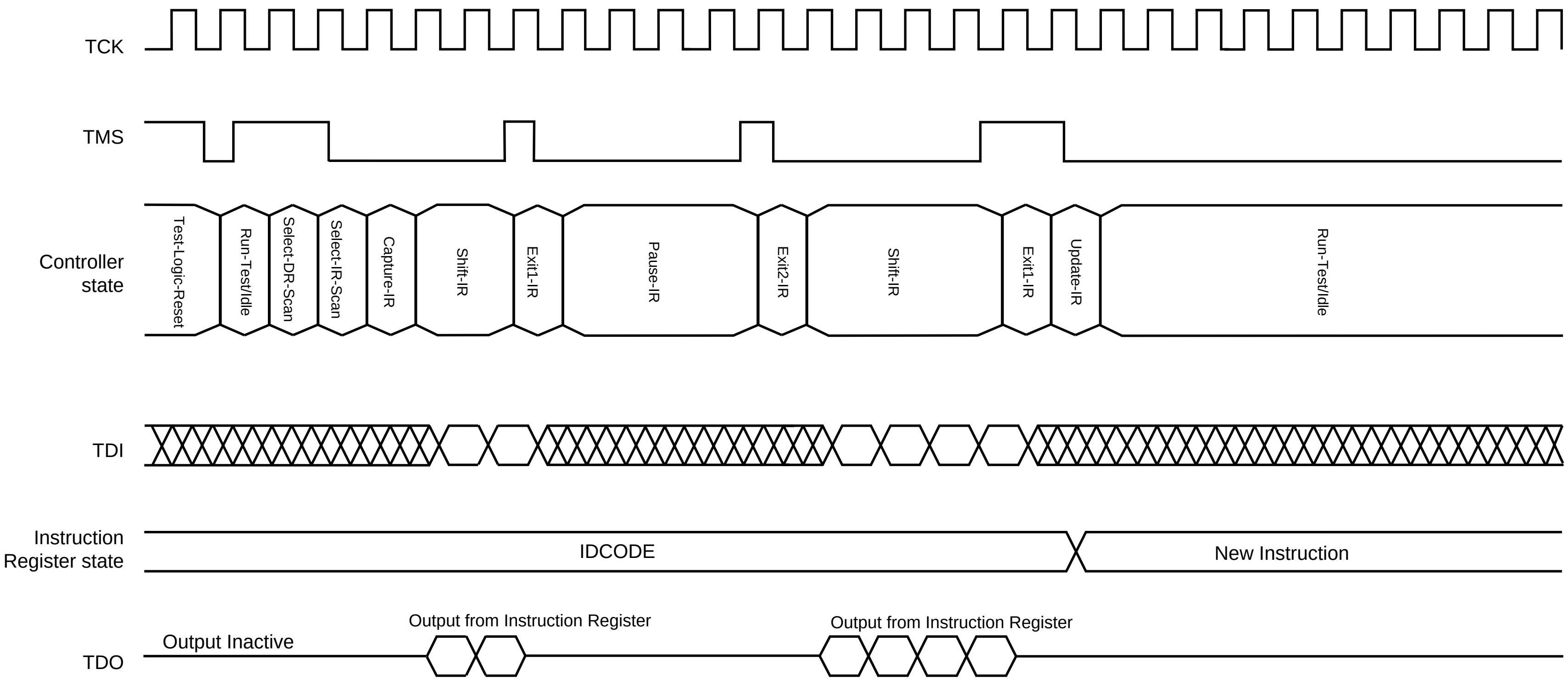
Disabling the Test Access Port

It is possible to use this device without utilizing the TAP. To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to VSS to preclude mid level inputs.

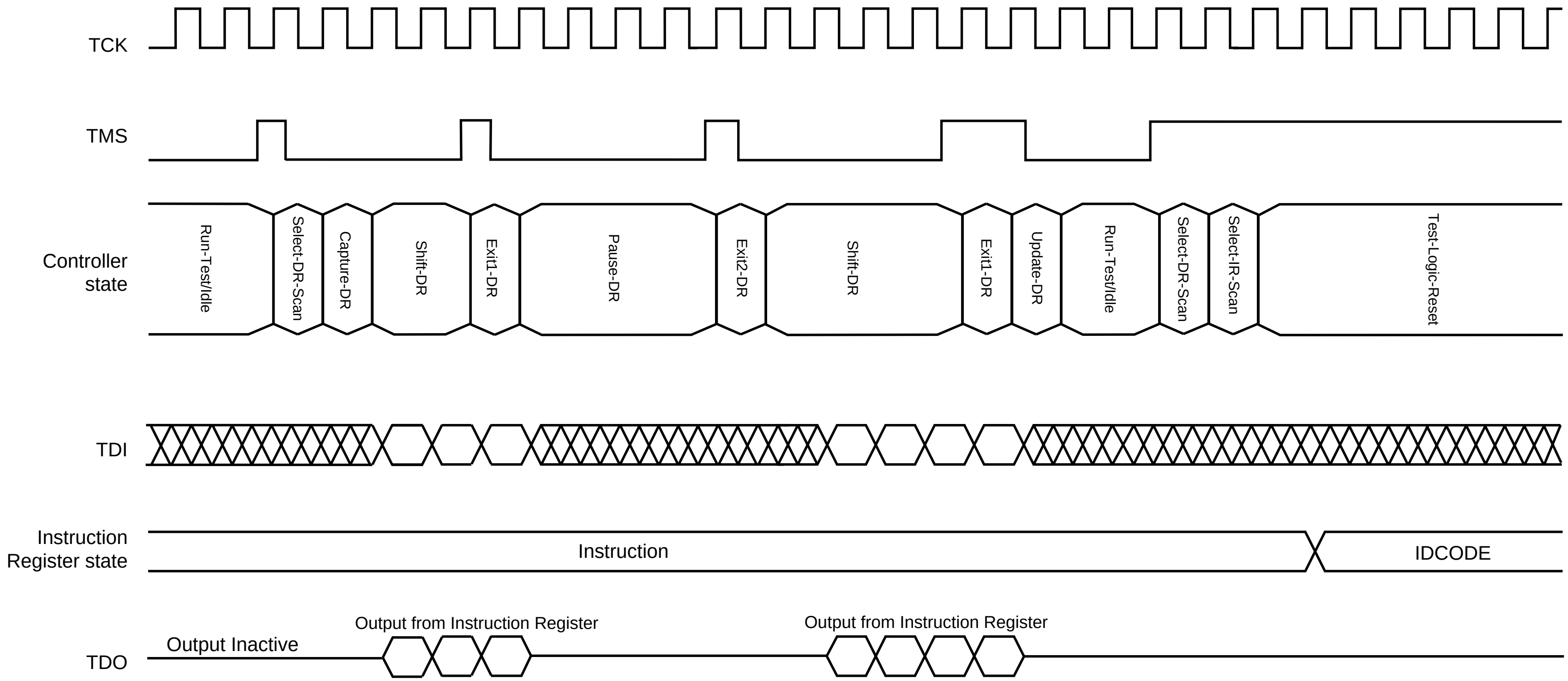
TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to VDD through a 1k resistor.

TDO should be left unconnected.

Test Logic Operation (Instruction Scan)



Test Logic Operation (Data Scan)



Package Drawing

TBD

Recommended Soldering Condition

Please consult with our sales offices for soldering conditions of these products.

Type of Surface Mount Devices

μPD44164085Fx : 165-pin PLASTIC FBGA (13 x 15)

μPD44164185Fx : 165-pin PLASTIC FBGA (13 x 15)

μPD44164365Fx : 165-pin PLASTIC FBGA (13 x 15)

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.