NEC

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC2726T

1.6 GHz SILICON MMIC DIFFERENTIAL WIDE BAND AMPLIFIER

DESCRIPTION

The μPC2726T is a silicon microwave monolithic integrated circuit designed for miniature differenctial amplifier. This IC operates up to 1.6 GHz and therefore is suitable for BS tuner, mobile communication and measurement equipment applications. This IC can also use as differential oscillator application.

This IC is manufactured using NEC's 20 GHz f_T NESAT™ III silicon bipolar process. This process uses silicon nitride passivation film and gold electrodes. These materials can protect the chip surface from external pollution and prevent corrosion/migration. Thus, this IC has excellent performance, uniformity and reliability.

★ FEATURES

- Supply voltage : V_{CC} = 4.5 to 5.5 V
- Circuit current : I_{CC} = 11.5 mA TYP. @V_{CC} = 5.0 V
- Power gain : G_P = 15.0 dB TYP. @f = 400 MHz
- Saturated output power gain : $P_{O(sat)}$ = –2.0 dBm @f = 400 MHz
- High isolation : ISL = 60 dB TYP. @f = 400 MHz
- Upper limit operating frequency : f_u = 1.6 GHz TYP. @3 dB down below from gain at f = 400 MHz

ORDERING INFORMATION

Part Number	Package	Supplying Form
μPC2726T-E3	6-pin minimold	• Embossed tape 8 mm wide • 1, 2, 3 pin face the perforation side of the tape • Qty 3 kpcs/reel

Remark To order evaluation samples, please contact your local NEC sales office.
Part number for sample order: μPC2726T

Caution Electro-static sensitive devices

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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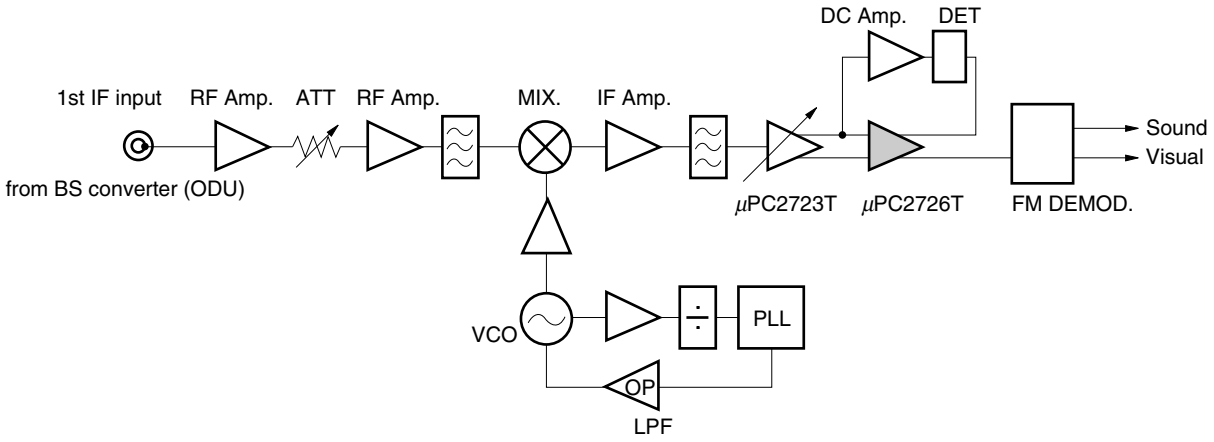
Printed in Japan

The mark ★ shows major revised points.

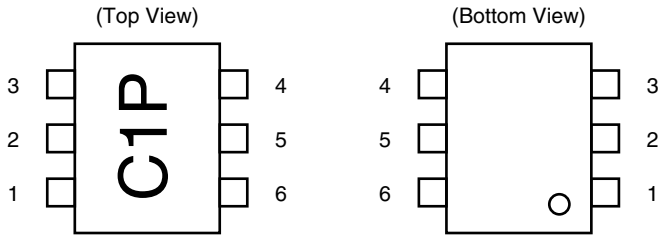
EXAMPLE FOR SYSTEM APPLICATION

DBS tuner



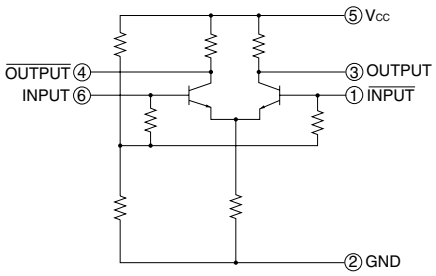
Caution The insertion point is different due to the specifications of conjunct devices.

PIN CONNECTIONS



Pin No.	Pin Name
1	$\overline{\text{INPUT}}$
2	GND
3	OUTPUT
4	$\overline{\text{OUTPUT}}$
5	V_{CC}
6	INPUT

★ PIN EXPLANATION

Pin No.	Pin Name	Applied Voltage (V)	Pin Voltage (V)[Note]	Function and Applications	Internal Equivalent Circuit
1 6	$\overline{\text{INPUT}}$ INPUT	–	3.45	Signal input pin.	
2	GND	0	–	Ground pin. This pin should be connected to system ground with minimum indactance. Ground pattern on the board should be formed as wide as possible. All the ground pins must be connected together with wide ground pattern to decrease impedance difference.	
3 4	OUTPUT $\overline{\text{OUTPUT}}$	–	3.76	Signal output pin.	
5	Vcc	4.5 to 5.5	–	Power supply pin. This pin should be externally equipped with bypass capacitor to minimize ground impedance.	

Note Pin voltage is measured at Vcc = 3.0 V

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V_{CC}	T_A = +25°C	6	V
Power Dissipation	P_D	T_A = +85°C **Note**	280	mW
Operating Ambient Temperature	T_A		−40 to +85	°C
Storage Temperature	T_{stg}		−55 to +150	°C
Input Power	P_{in}	T_A = +25°C	0	dBm

Note Mounted on double-sided copper clad 50 × 50 × 1.6 mm epoxy grass PWB

RECOMMENDED OPERATING RANGE

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating Ambient Temperature	T_A	−40	+25	+85	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, T_A = +25°C, V_{CC} = 5.0 V, Z_S = Z_L = 50 Ω, at single input)

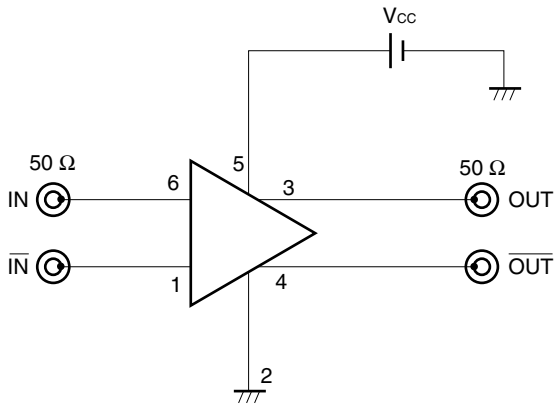
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Circuit Current	I_{CC}	No signal	8.0	11.5	15.0	mA
Power Gain	G_P	f = 400 MHz	11.0	15.0	17.0	dB
Noise Figure	NF	f = 400 MHz	–	4.5	6.0	dB
Upper Limit Operating Frequency	f_u	3 dB down below from gain at f = 0.4 GHz	1.0	1.6	–	GHz
Isolation	ISL	f = 400 MHz	–	60	–	dB
Input Return Loss	RL_{in}	f = 400 MHz	–	2.0	–	dB
Output Return Loss	RL_{out}	f = 400 MHz	–	4.0	–	dB
Saturated Output Power	$P_{O(sat)}$	f = 400 MHz, P_{in} = −10 dBm	−5.0	−2.0	–	dBm

STANDARD CHARACTERISTICS FOR REFERENCE (T_A = +25°C, Z_S = Z_L = 50 Ω, at single input)

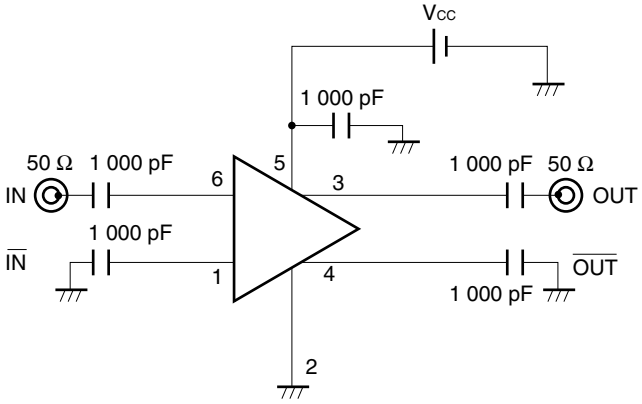
Parameters	Symbol	Test Conditions	Reference Value	Unit
Circuit Current	I_{CC}	V_{CC} = 2 V, No input signal	2.5	mA
Power Gain	G_P	V_{CC} = 2 V, f = 400 MHz	4.5	dB
Noise Figure	NF	V_{CC} = 2 V, f = 400 MHz	5.1	dB
Upper Limit Operating Frequency	f_u	3 dB down below flat gain at 0.4 GHz	2.4	GHz
Isolation	ISL	V_{CC} = 2 V, f = 400 MHz	58	dB
Input Return Loss	RL_{in}	V_{CC} = 2 V, f = 400 MHz	1.0	dB
Output Return Loss	RL_{out}	V_{CC} = 2 V, f = 400 MHz	4.0	dB
Maximum Output Power	$P_{O(sat)}$	V_{CC} = 2 V, f = 400 MHz, P_{in} = −10 dBm	−14	dBm
3rd Order Intermodulation Distortion 1	$IM_3$1	V_{CC} = 2 V, $P_{O(each)}$ = −25 dBm, f_1 = 400 MHz, f_2 = 402 MHz	−29	dBc
3rd Order Intermodulation Distortion 2	$IM_3$2	V_{CC} = 5 V, $P_{O(each)}$ = −25 dBm, f_1 = 400 MHz, f_2 = 402 MHz	−45	dBc

★ TEST CIRCUITS

DC Parameters



AC Parameters



CAPACITORS FOR THE Vcc, INPUT AND OUTPUT PINS

1 000 pF capacitors are recommendable as bypass capacitor for Vcc pin and coupling capacitors for input/output pins.

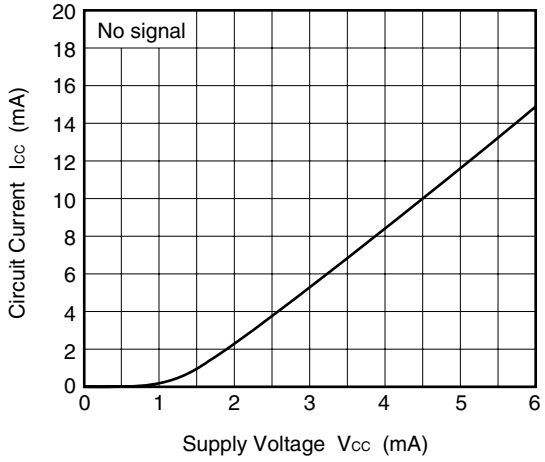
Bypass capacitor for Vcc pin is intended to minimize Vcc pin's ground impedance. Therefore, stable bias can be supplied against Vcc fluctuation.

Coupling capacitors for input/output pins are intended to minimize RF serial impedance and cut DC.

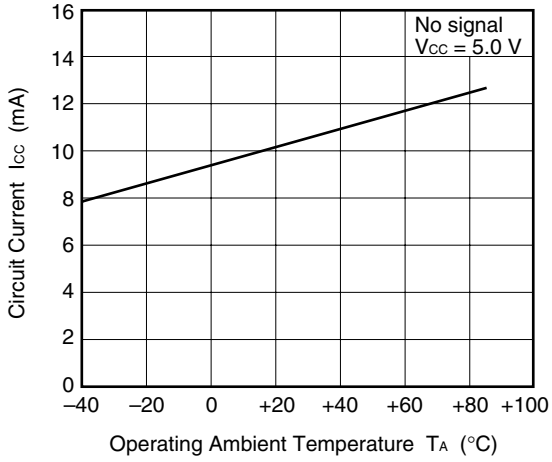
To get a flat gain from 100 MHz up, 1 000 pF capacitors are assembled on the test circuit. [Actually, 1 000 pF capacitors give flat gain at least 10 MHz. In the case of under 10 MHz operation, increase the value of coupling capacitor such as 2 200 pF. Because the coupling capacitors are determined by the equation of $C = 1/(2\pi fZs)$.]

TYPICAL CHARACTERISTICS (Unless otherwise specified, T_A = +25°C)

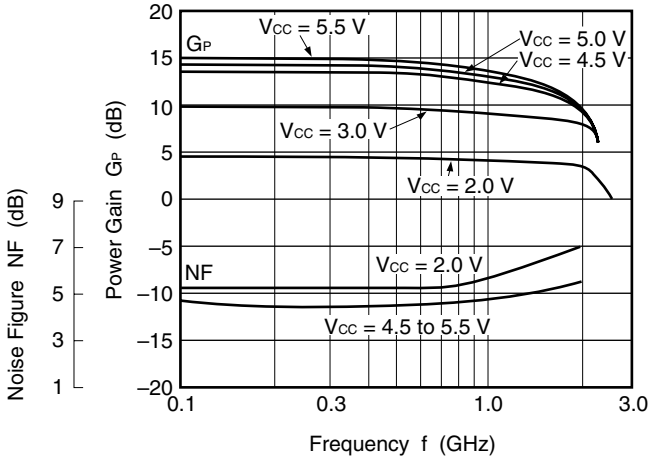
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



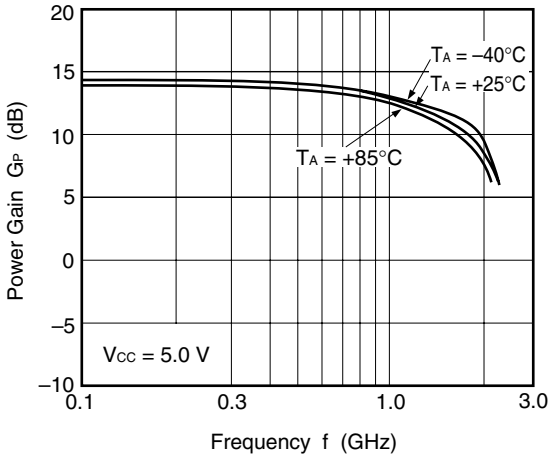
CIRCUIT CURRENT vs. OPERATING AMBIENT TEMPERATURE



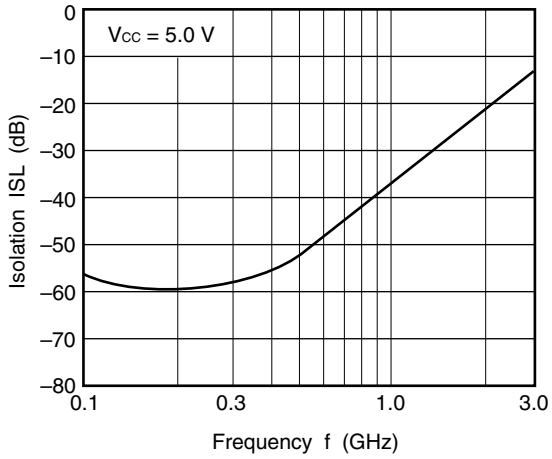
NOISE FIGURE, POWER GAIN vs. FREQUENCY



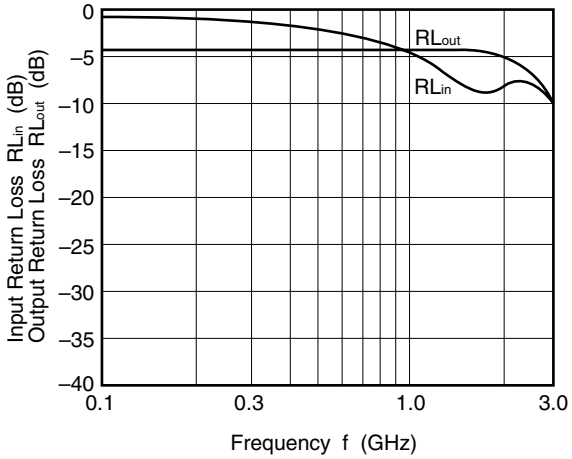
POWER GAIN vs. FREQUENCY



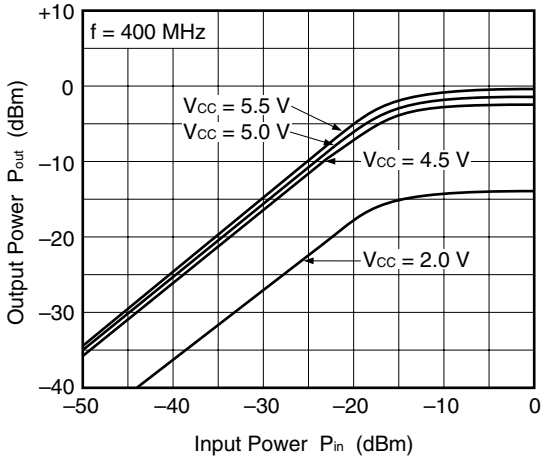
ISOLATION vs. FREQUENCY



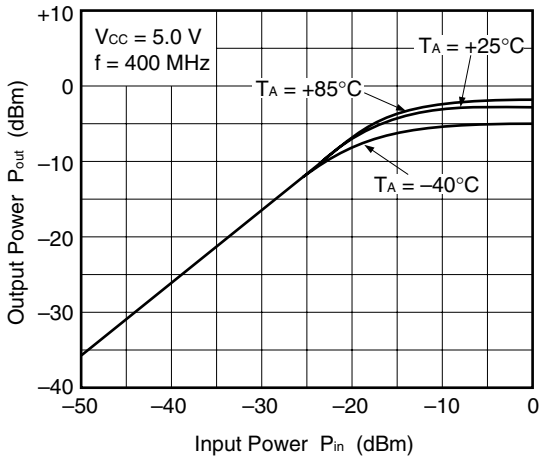
INPUT RETURN LOSS, OUTPUT RETURN LOSS vs. FREQUENCY



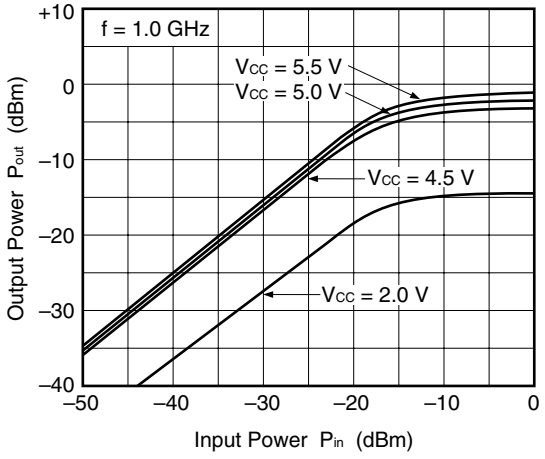
OUTPUT POWER vs. INPUT POWER



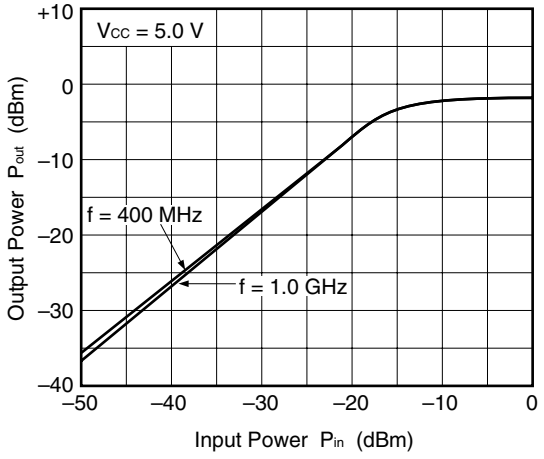
OUTPUT POWER vs. INPUT POWER



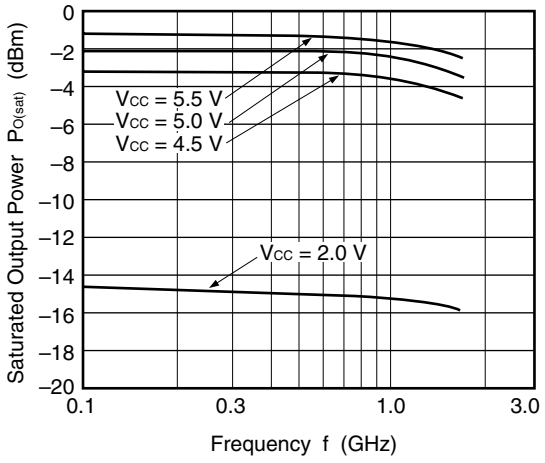
OUTPUT POWER vs. INPUT POWER



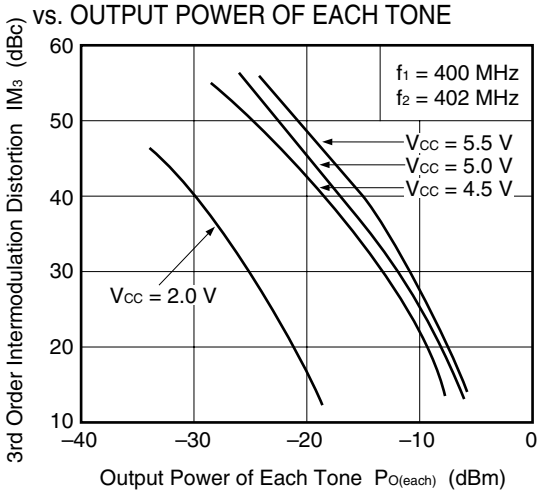
OUTPUT POWER vs. INPUT POWER



SATURATED OUTPUT POWER vs. FREQUENCY



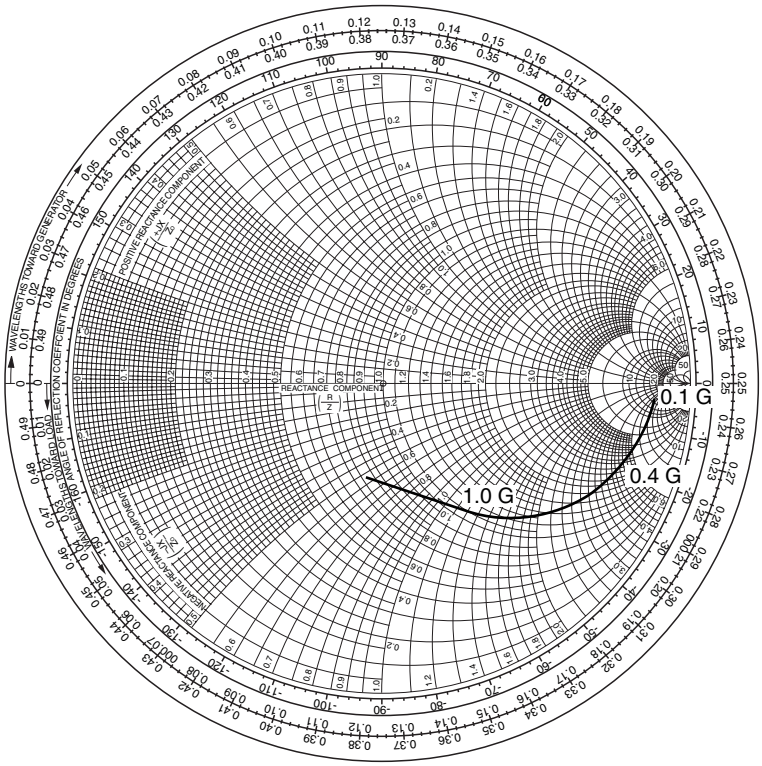
3RD ORDER INTERMODULATION DISTORTION vs. OUTPUT POWER OF EACH TONE



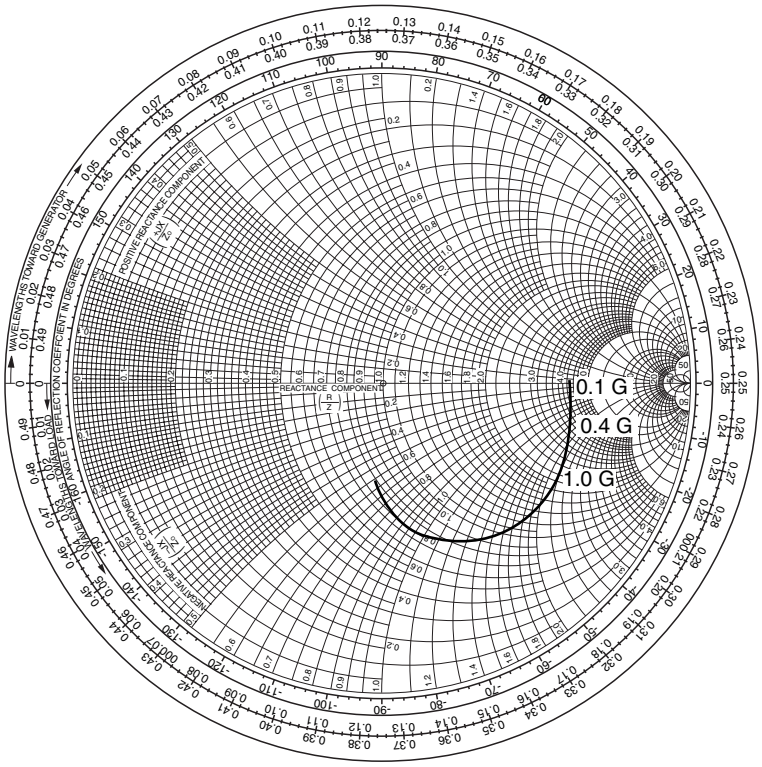
Remark The graphs indicate nominal characteristics.

S-PARAMETERS (Vcc = 5.0 V)

S_{11}-FREQUENCY

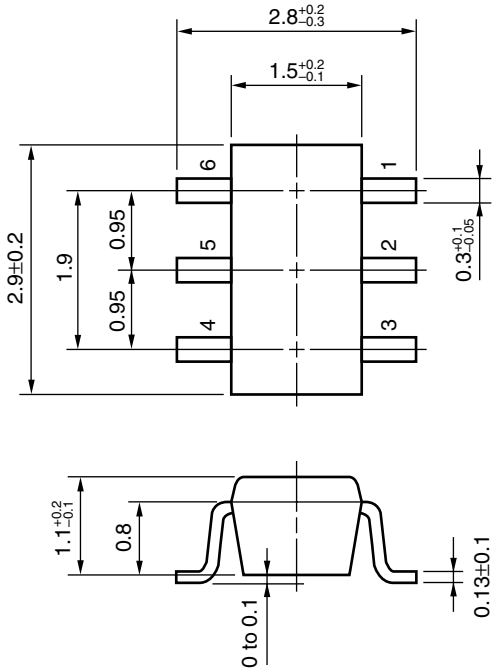


S_{22}-FREQUENCY



★ **PACKAGE DIMENSIONS**

6-PIN MINIMOLD (UNIT: mm)



★ NOTES ON CORRECT USE

(1) Observe precautions for handiling because of electro-static sensitive devices.

(2) Form a ground pattern as widely as possible to minimize ground impedance (to prevent undesired oscillation). All the ground pins must be connected together with wide ground pattern to decrease impedance difference.

(3) The bypass capacitor should be attached to V_{CC} line.

(4) The DC cut capacitor must be each attached to input pin and output pin.

★ RECOMMENDED SOLDERING CONDITIONS

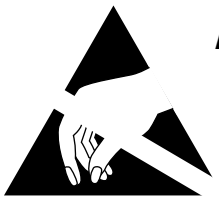
This product should be soldered under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235°C or below Time: 30 seconds or less (at 210°C) Count: 3, Exposure limit: None[Note]	IR35-00-3
VPS	Package peak temperature: 215°C or below Time: 40 seconds or less (at 200°C) Count: 3, Exposure limit: None[Note]	VP15-00-3
Wave Soldering	Soldering bath temperature: 260°C or below Time: 10 seconds or less Count: 1, Exposure limit: None[Note]	WS60-00-1
Partial Heating	Pin temperature: 300°C or below Time: 3 seconds or less (per side of device) Exposure limit: None[Note]	–

Note After opening the dry pack, keep it in a place below 25°C and 65% RH for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

For details of recommended soldering conditions for surface mounting, refer to information document **SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E)**.



ATTENTION

OBSERVE PRECAUTIONS
FOR HANDLING
ELECTROSTATIC
SENSITIVE
DEVICES

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