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μPD72873,72874

IEEE1394 OHCI 1.1 Compliant PHY/Link 1-chip Host Controller

Description

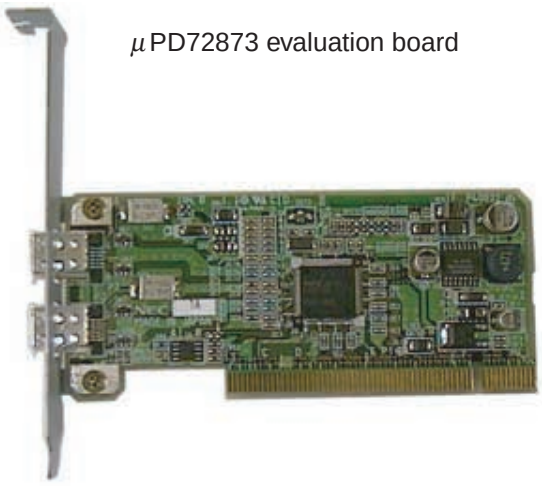
The μPD72873 and 72874 are NEC's single-chip solution for implementing an OHCI-Link layer and physical layer in compliance with the IEEE1394a-2000 specification. The μPD72873 has two and the μPD72874 three cable ports. The on-chip PCI/Cardbus interface, the OHCI 1.1 compliant architecture with OHCI 1.0 backward compatibility and the super low-power design makes the devices excellent choices for mobile PC applications, such as notebooks and PCMCIA cards. Package and pin configration are almost identical to NEC's OHCI 1.0 predecessor, the μPD72872, for easy substitution on application boards.

Features

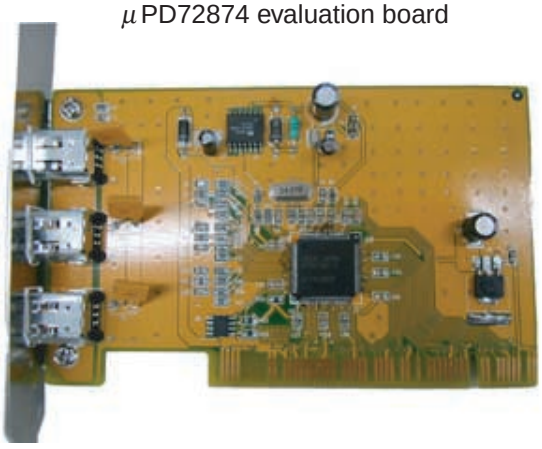
- Link layer complies with 1394 Open Host Controller Interface Specification release 1.1
- Physical layer complies with IEEE1394a-2000 (Data rate : 100/200/400 Mbps)
  - μPD72873 : two IEEE1394 DS ports
  - μPD72874 : three IEEE1394 DS ports
- Modular 32-bit host interface complies with PCI Specification release 2.2
- PCI Bus Power Management Interface Specification release 1.1
- Modular 32-bit host interface complies with CardBus Specification
- On-chip FIFOs :
  - Isochronous transmit : 2048 bytes
  - Asynchronous transmit : 2048 bytes
  - Common receive : 3072 bytes
- Power management : D0, D1, D2, D3 hot, wake-up from D3 cold supported
- 4 isochronous transmit DMAs and 4 isochronous receive DMAs supported
- 2-wire serial EEPROM™ interface supported
- Temperature range : 0 to 70°C
- Operation voltage : 3.3 V ±10%, single power supply
- Package : 120-pin plastic TQFP (Fine pitch) (14 × 14)

Evaluation Board

μPD72873 evaluation board



μPD72874 evaluation board



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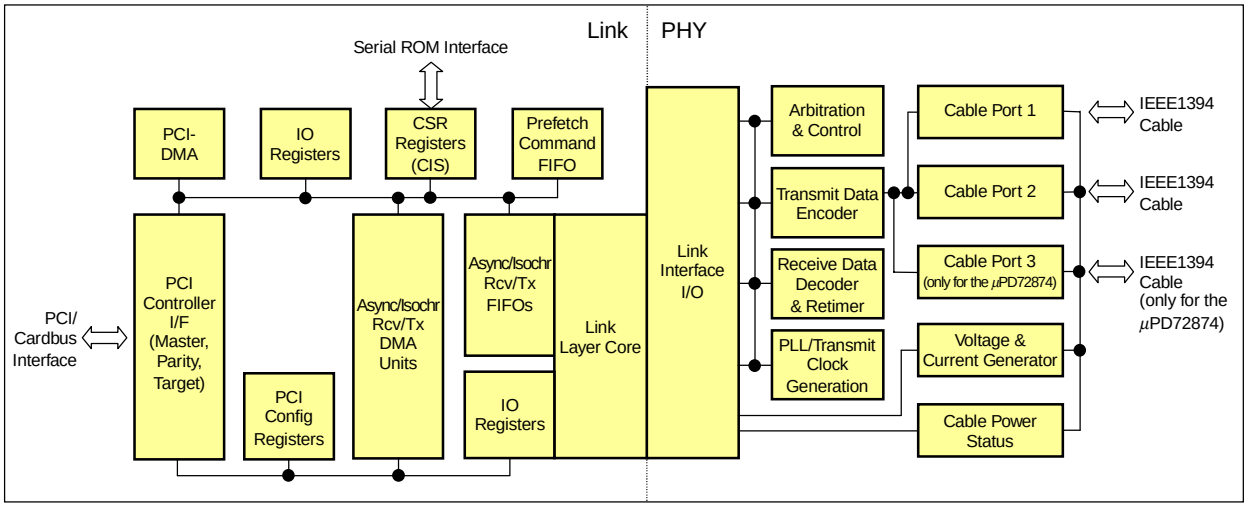
Block Diagram



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