Introduction

The Utopia (Universal Test & Operations PHY Interface for ATM) interface is defined by the ATM Forum to provide a standard interface between ATM devices and ATM PHY or SAR (segmentation and Re-assembly) devices.

The ATM forum has standardized the Utopia Level 2 (L2) which can handle aggregated throughputs of 622Mbps (OC-12 Rates). The Utopia L2 can be used in single or multi PHY applications.

The Slave interface responds to the polling of the Master device when it is able to receive or transmit a complete ATM cell. The Master device selects the Slave and initiates data transfers to / from the Slave device.

The Utopia Level 2 Slave Macrocell from MorethanIP is designed for ease of use performance and provides the required flexibility to be used in a wide range of applications.
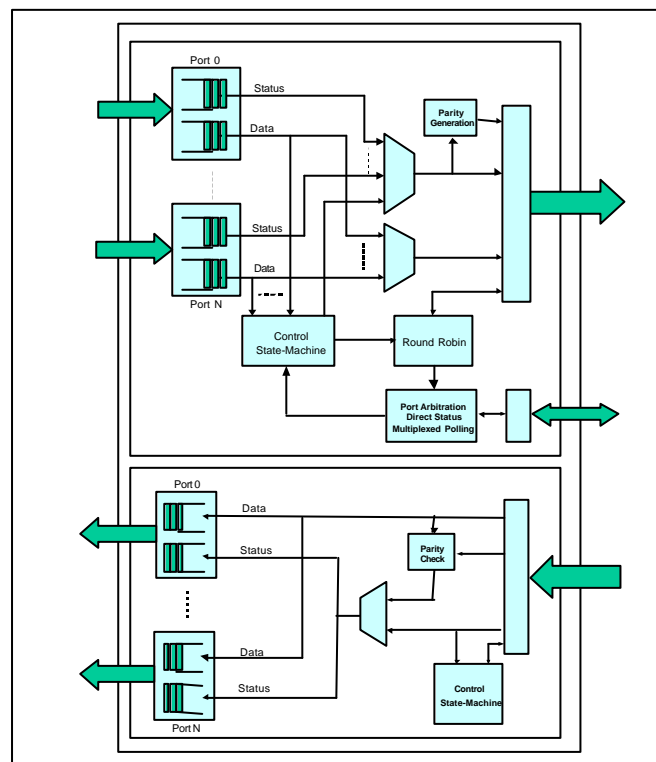
Features

- Compliant with ATM-Forum af-phy-0039.000

- Programmable Utopia Level-2 data width (8, 16-Bit)

- Meets 50MHz performance and 16-Bit interface operation supporting 800Mbps (Exceeding OC-12 requirements) packet rate transfers

- Selectable Octet Level or Cell Level transfers supported with Polled or Direct status indication and User programmable FIFO thresholds

- Packet rate decoupling with fully User programmable (Depth) FIFOs

- Optional odd Parity checking / generation on the Utopia Ingress / Egress interfaces

- Programmable Single PHY or Multi PHY (MPHY) operation with Out-Band addressing

- Programmable number of PHY ports from 1 (Single PHY operation) to 31

- Advanced management options with error handling, Utopia protocol violation check and non compliant cell discard

- Simple User application interface with a two signals handshake simplifying the user application design and integration

- Delivered with a complete and programmable simulation environment

- Scripts for Synplicity / Modelsim synthesis / simulation tools provided

- Delivered in VHDL source code for easy integration and with a platform independent JAVA configuration utility

- Optimized FIFO with Eclipse and QuickSD specific embedded memory blocks for high integration and speed

Application
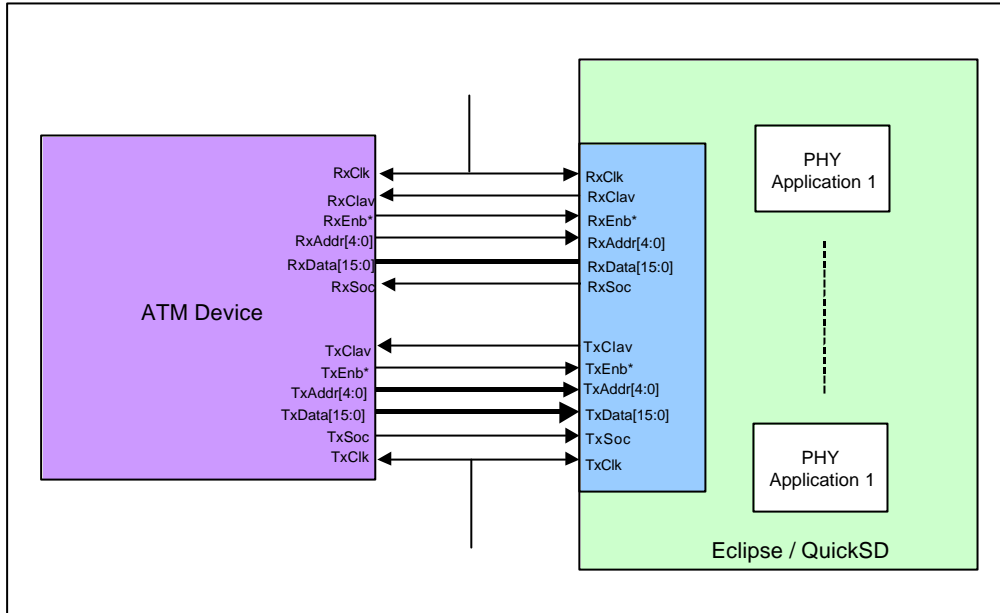
Application Example – L2 MPHY Polled Status Indication

Block Diagram

Block Diagram

Design Kit Overview

Design Files Language	Optimized VHDL
Simulation	Configurable VHDL Testbench with different simulation scenarios verifying the Macrocell features and simulating non Utopia compliance behavior
System Verification	The Testbench implements a configurable Utopia model to exercise the Macrocell.
Design Tools	
Simulation	Modelsim Version 5.4d Scripts (do files) provided
Synthesis	Synplicity Synplify v6.1.3
Implementation	Quickworks v9.0

References

- ATM Forum, af-phy-0039.000
- Quicklogic, Eclipse Family Datasheet (Preliminary, 8/24/2000)
- Quicklogic, QL82SD QuickSD Programmable Serdes (Preliminary, 8/25/2000)

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