

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μ PD78F0058 is a product of the μ PD780058 Subseries in the 78K/0 Series and equivalent to the μ PD780058 with a flash memory in place of internal ROM. This device is incorporated with a flash memory which can be programmed without being removed from the substrate.

Functions are described in detail in the following user's manuals, which should be read when carrying out design work.

μ PD780058, 780058Y Subseries User's Manual : U12013E
78K/0 Series User's Manual Instruction : IEU-1372

FEATURES

- Pin-compatible with mask ROM versions (except V_{PP} pin)
- Flash memory : 60 Kbytes^{Note 1}
- Internal high-speed RAM : 1024 bytes
- Internal expansion RAM : 1024 bytes^{Note 2}
- Buffer RAM : 32 bytes
- Operable with the same power supply voltage as that of mask ROM version ($V_{DD} = 1.8$ to 5.5 V)

Notes 1. The flash memory capacity can be changed with the memory size switching register (IMS).

2. The internal expansion RAM capacity can be changed with the internal expansion RAM size switching register (IXS).

Remark For the differences between the flash memory versions and the mask ROM versions, refer to
1. DIFFERENCES BETWEEN μ PD78F0058 AND MASK ROM VERSIONS.

ORDERING INFORMATION

Part Number	Package	Internal ROM
μ PD78F0058GC-3B9	80-pin plastic QFP (14 × 14 mm, resin thickness 2.7 mm)	Flash memory
μ PD78F0058GC-8BT ^{Note}	80-pin plastic QFP (14 × 14 mm, resin thickness 1.4 mm)	Flash memory
μ PD78F0058GK-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm)	Flash memory

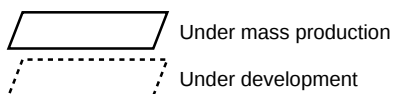
Note Under planning

Caution Two types of packages are available for μ PD78F0058GC (refer to 6. PACKAGE DRAWINGS).
For the suppliable package, consult an NEC sales representative.

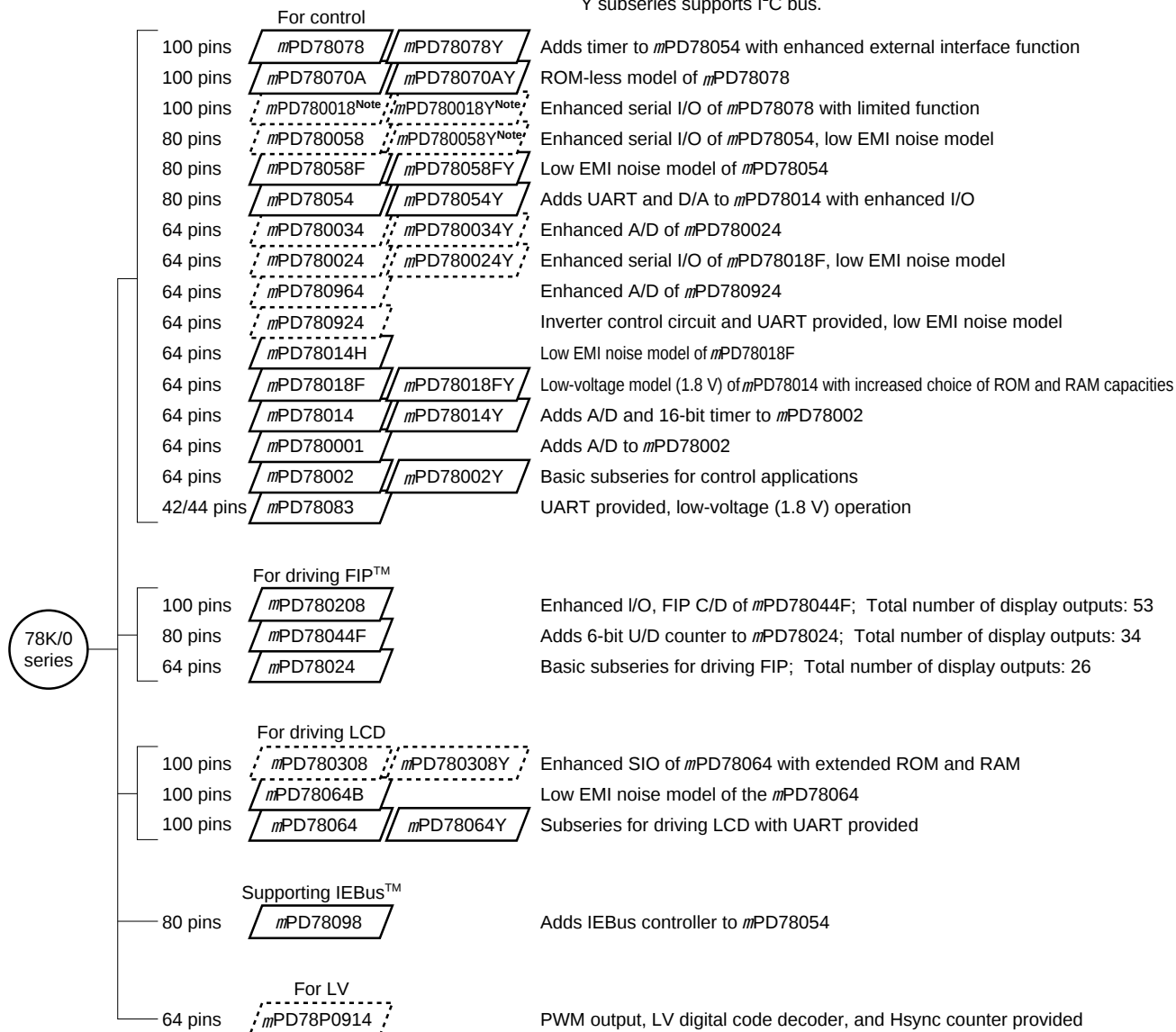
The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

78K/0 SERIES DEVELOPMENT

The products in the 78K/0 series are listed below. The names enclosed in boxes are subseries names.



Y subseries supports I²C bus.



Note Under planning

The following lists the main functional differences.

Subseries	Function	ROM Capacity	Timer				8-bit	10-bit	8-bit	Serial Interface	I/O	V _{DD} MIN. Value	External Expansion
			8-bit	16-bit	Watch	WDT	A/D	A/D	D/A				
For control	μPD78078	32 K-60 K	4 ch	1 ch	1 ch	1 ch	8 ch	—	2 ch	3 ch (UART: 1 ch)	88	1.8 V	○
	μPD78070A	—									61	2.7 V	
	μPD780018	48 K-60 K							—	2 ch (Time division 3-wire: 1 ch)	88		
	μPD780058	24 K-60 K	2 ch						2 ch	3 ch (Time division UART: 1 ch)	68	1.8 V	
	μPD78058F	48 K-60 K								3 ch (UART: 1 ch)	69	2.7 V	
	μPD78054	16 K-60 K										2.0 V	
	μPD780034	8 K-32 K					—	8 ch	—	3 ch (UART: 1 ch, Time division 3-wire: 1 ch)	51	1.8 V	
	μPD780024						8 ch	—					
	μPD780964		3 ch	Note	—		—	8 ch		2 ch (UART: 2 ch)	47	2.7 V	
	μPD780924						8 ch	—					
	μPD78014H		2 ch	1 ch	1 ch					2ch	53	1.8 V	
	μPD78018F	8 K-60 K										2.7 V	
	μPD78014	8 K-32 K											
	μPD780001	8 K		—	—					1 ch	39		—
	μPD780002	8 K-16 K			1 ch		—				53		○
	μPD78083				—		8 ch			1 ch (UART: 1 ch)	33	1.8 V	—
For FIP driving	μPD780208	32 K-60 K	2 ch	1 ch	1 ch	1 ch	8 ch	—	—	2 ch	74	2.7 V	—
	μPD78044F	16 K-40 K									68		
	μPD78024	24 K-32 K									54		
For LCD driving	μPD780308	48 K-60 K	2 ch	1 ch	1 ch	1 ch	8 ch	—	—	3 ch (Time division UART: 1 ch)	57	2.0 V	—
	μPD78064B	32 K								2 ch (UART: 1 ch)			
	μPD78064	16 K-32 K											
For IEBus	μPD78098	32 K-60 K	2 ch	1 ch	1 ch	1 ch	8 ch	—	2 ch	3 ch (UART: 1 ch)	69	2.7V	○
For LV	μPD78P0914	32 K	6 ch	—	—	1 ch	8 ch	—	—	2 ch	54	4.5 V	○

Note 10-bit timer: 1 channel

OVERVIEW OF FUNCTION

Item		Function								
Internal memory	Flash memory	60 Kbytes ^{Note 1}								
	High-speed RAM	1024 bytes								
	Expansion RAM	1024 bytes ^{Note 2}								
	Buffer RAM	32 bytes								
Memory space		64 Kbytes								
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)								
Instruction cycle		On-chip instruction execution time cycle modification function								
	When main system clock selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs 12.8 μs (at 5.0-MHz operation)								
	When subsystem clock selected	122 μs (at 32.768-kHz operation)								
Instruction set		• 16-bit operation • Multiplication/division (8 bits × 8 bits,16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD correction, etc.								
I/O ports		<table><tr><td>Total</td><td>: 68</td></tr><tr><td>• CMOS input</td><td>: 2</td></tr><tr><td>• CMOS I/O</td><td>: 62</td></tr><tr><td>• N-ch open drain I/O</td><td>: 4</td></tr></table>	Total	: 68	• CMOS input	: 2	• CMOS I/O	: 62	• N-ch open drain I/O	: 4
Total	: 68									
• CMOS input	: 2									
• CMOS I/O	: 62									
• N-ch open drain I/O	: 4									
A/D converter		• 8-bit resolution × 8 channels								
D/A converter		• 8-bit resolution × 2 channels								
Serial interface		<table><tr><td>• 3-wired serial I/O/SBI/2-wire serial I/O mode selectable</td><td>: 1 channel</td></tr><tr><td>• 3-wired serial I/O mode (MAX. 32-byte on-chip automatic transmission/reception function)</td><td>: 1 channel</td></tr><tr><td>• 3-wired serial I/O/UART mode (on-chip time division transfer function) selectable</td><td>: 1 channel</td></tr></table>	• 3-wired serial I/O/SBI/2-wire serial I/O mode selectable	: 1 channel	• 3-wired serial I/O mode (MAX. 32-byte on-chip automatic transmission/reception function)	: 1 channel	• 3-wired serial I/O/UART mode (on-chip time division transfer function) selectable	: 1 channel		
• 3-wired serial I/O/SBI/2-wire serial I/O mode selectable	: 1 channel									
• 3-wired serial I/O mode (MAX. 32-byte on-chip automatic transmission/reception function)	: 1 channel									
• 3-wired serial I/O/UART mode (on-chip time division transfer function) selectable	: 1 channel									
Timer		<table><tr><td>• 16-bit timer/event counter</td><td>: 1 channel</td></tr><tr><td>• 8-bit timer/event counter</td><td>: 2 channels</td></tr><tr><td>• Watch timer</td><td>: 1 channel</td></tr><tr><td>• Watchdog timer</td><td>: 1 channel</td></tr></table>	• 16-bit timer/event counter	: 1 channel	• 8-bit timer/event counter	: 2 channels	• Watch timer	: 1 channel	• Watchdog timer	: 1 channel
• 16-bit timer/event counter	: 1 channel									
• 8-bit timer/event counter	: 2 channels									
• Watch timer	: 1 channel									
• Watchdog timer	: 1 channel									
Timer output		3 (14-bit PWM output capable: 1)								
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, 5.0 MHz (main system clock: at 5.0-MHz operation) 32.768 kHz (subsystem clock: at 32.768-kHz operation)								
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz, 9.8 kHz (main system clock: at 5.0-MHz operation)								
Vectored-interrupt source	Maskable	Internal : 13, External : 7								
	Non-maskable	Internal : 1								
	Software	1								
Test input		Internal : 1, External : 1								
Power supply voltage		V _{DD} = 1.8 to 5.5 V								
Operating ambient temperature		T _A = −40 to +85°C								
Package		• 80-pin plastic QFP (14 × 14 mm, resin thickness 2.7 mm) • 80-pin plastic QFP (14 × 14 mm, resin thickness 1.4 mm)^{Note 3} • 80-pin plastic TOFP (fine pitch) (12 × 12 mm)								

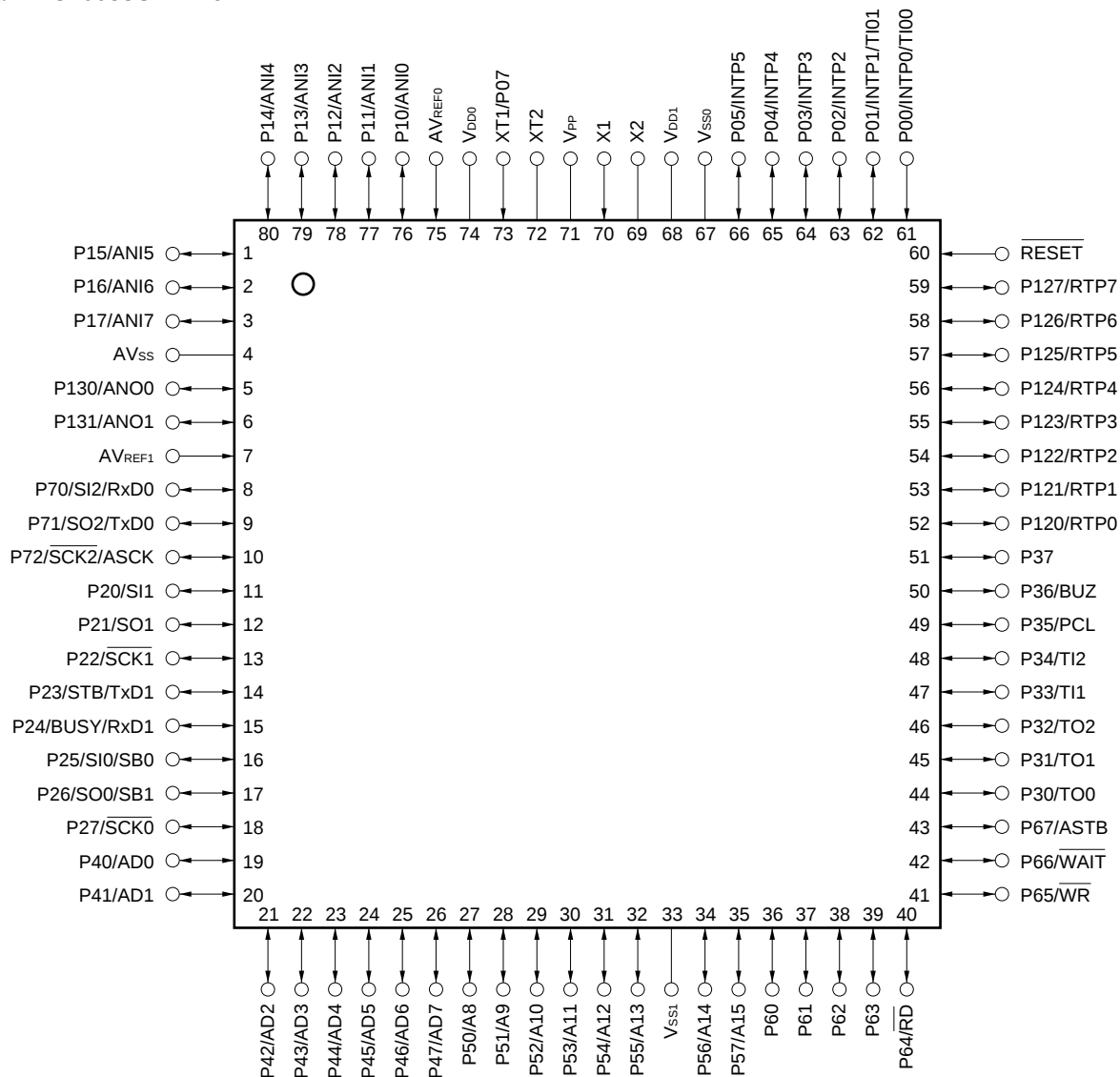
Notes 1. The flash memory capacity can be changed with the memory size switching register (IMS).

2. The internal expansion RAM capacity can be changed with the internal expansion RAM size switching register (IXS).

3. Under planning

PIN CONFIGURATION (Top View)

- 80-pin plastic QFP (14 × 14 mm, resin thickness 2.7 mm)
μPD78F0058GC-3B9
- 80-pin plastic QFP (14 × 14 mm, resin thickness 1.4 mm)
μPD78F0058GC-8BT^{Note}
- 80-pin plastic TQFP (fine pitch) (12 × 12 mm)
μPD78F0058GK-BE9



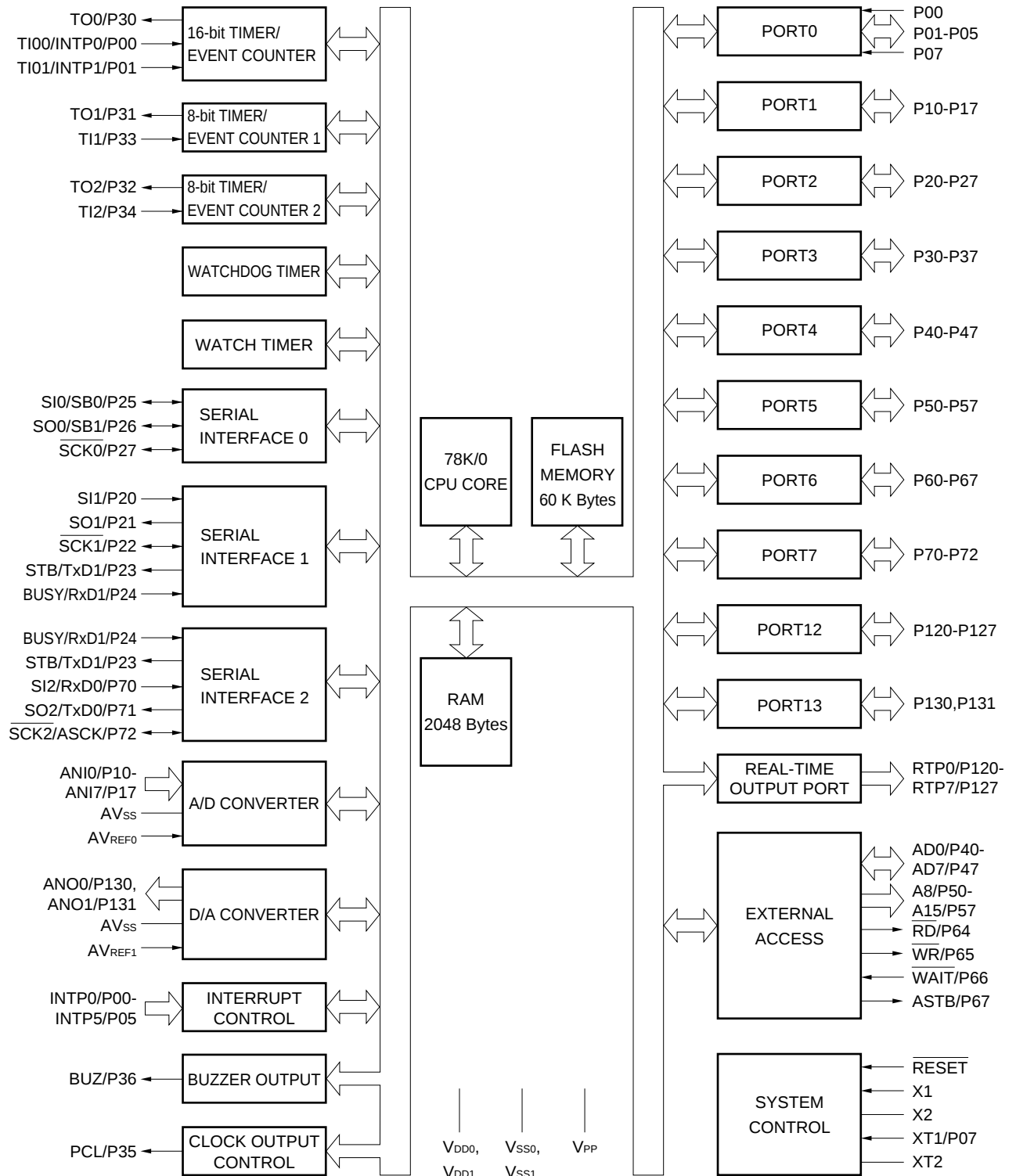
Note Under planning

- Cautions**
1. Connect the V_{PP} pin directly to V_{SS} in normal operation mode
 2. Connect the AV_{SS} pin to V_{SS0}.

Remark When the μPD78F0058 is used in application fields that require reduction of the noise generated from inside the microcontroller, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

A8-A15	: Address Bus	PCL	: Programmable Clock
AD0-AD7	: Address/Data Bus	$\overline{RD}$	: Read Strobe
ANI0-ANI7	: Analog Input	$\overline{RESET}$	: Reset
ANO0, ANO1	: Analog Output	RTP0-RTP7	: Real-Time Output Port
ASCK	: Asynchronous Serial Clock	RxD0, RxD1	: Receive Data
ASTB	: Address Strobe	SB0, SB1	: Serial Bus
AV _{REF0, 1}	: Analog Reference Voltage	$\overline{SCK0-SCK2}$	: Serial Clock
AV _{SS}	: Analog Ground	SI0-SI2	: Serial Input
BUSY	: Busy	SO0-SO2	: Serial Output
BUZ	: Buzzer Clock	STB	: Strobe
INTP0-INTP6	: Interrupt from Peripherals	TI00, TI01	: Timer Input
P00-P05, P07	: Port0	TI1, TI2	: Timer Input
P10-P17	: Port1	TO0-TO2	: Timer Output
P20-P27	: Port2	TxD0, TxD1	: Transmit Data
P30-P37	: Port3	V _{DD0} , V _{DD1}	: Power Supply
P40-P47	: Port4	V _{PP}	: Programming Power Supply
P50-P57	: Port5	V _{SS0} , V _{SS1}	: Ground
P60-P67	: Port6	$\overline{WAIT}$	: Wait
P70-P72	: Port7	$\overline{WR}$	: Write Strobe
P120-P127	: Port12	X1, X2	: Crystal (Main system Clock)
P130, P131	: Port13	XT1, XT2	: Crystal (Subsystem Clock)

BLOCK DIAGRAM



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1. DIFFERENCES BETWEEN μPD78F0058 AND MASK ROM VERSIONS

The μPD78F0058 is a product provided with a flash memory which enables on-board reading, erasing, and rewriting of programs with device mounted on target system. The functions of the μPD78F0058 (except the functions specified for flash memory and mask option of P60 to P63 pins) can be made the same as those of the mask ROM versions by setting the memory size switching register (IMS) and internal expansion RAM size switching register (IXS).

Table 1-1 shows the differences between the flash memory version (μPD78F0058) and the mask ROM versions (μPD780053, 780054, 780055, 780056, and 780058).

Table 1-1. Differences between μPD78F0058 and Mask ROM Versions

Item	μPD78F0058	Mask ROM Versions
Internal ROM structure	Flash memory	Mask ROM
Internal ROM capacity	60 Kbytes	μPD780053 : 24 Kbytes μPD780054 : 32 Kbytes μPD780055 : 40 Kbytes μPD780056 : 48 Kbytes μPD780058 : 60 Kbytes
Internal expansion RAM capacity	1024 bytes	μPD780053 : None μPD780054 : None μPD780055 : None μPD780056 : None μPD780058 : 1024 bytes
Internal ROM capacity changeable/not changeable with memory size switching register (IMS)	Changeable ^{Note 1}	Not changeable
Internal expansion RAM capacity changeable/not changeable with internal expansion RAM size switching register (IXS)	Changeable ^{Note 2}	Not changeable
IC pin	Not provided	Provided
V _{PP} pin	Provided	Not provided
P60 to P63 pin mask option with internal pull-up resistors	Not provided	Provided

- Notes** 1. Flash memory is set to 60 Kbytes by $\overline{\text{RESET}}$ input
2. Internal expansion RAM is set to 1024 bytes by $\overline{\text{RESET}}$ input.

Caution The noise resistance and noise radiation differ between flash memory versions and mask ROM versions. When considering the replacement of flash memory versions with mask ROM versions in the process from trial manufacturing to mass production, adequate evaluation should be carried out using CS products (not ES products) of mask ROM versions.

Remark Only the μPD780058 and 78F0058 are provided with IXS.

2. PIN FUNCTIONS

2.1 Port Pins (1/2)

Pin Name	I/O	Funciton		After Reset	Alternate Function
P00	Input	Port 0	Input only	Input	INTP0/TI00
P01	I/O	7-bit input/output port.	Input/output can be specified bit-wise. When used as an input port, an internal pull-up resistor can be connected by software.	Input	INTP1/TI01
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P07 ^{Note 1}	Input		Input only	Input	XT1
P10-P17	I/O	Port 1 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an internal pull-up resistor can be connected by software. ^{Note 2}		Input	ANI0-ANI7
P20	I/O	Port 2 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an internal pull-up resistor can be connected by software.		Input	SI1
P21					SO1
P22					SCK1
P23					STB/TxD1
P24					BUSY/RxD1
P25					SI0/SB0
P26					SO0/SB1
P27					SCK0
P30	I/O	Port 3 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an internal pull-up resistor can be connected by software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—

- Notes**
1. When using P07/XT1 pin as an input port, set 1 to the bit 6 (FRC) of the processor clock control register. Do not use the feedback resistor of the subsystem clock oscillator.
 2. When using P10/ANI0 to P17/ANI7 pins as analog inputs of A/D converter, the internal pull-up resistor is automatically set unused.

2.1 Port Pins (2/2)

Pin Name	I/O	Funciton		After Reset	Alternate Function
P40-P47	I/O	Port 4 8-bit input/output port. Input/output can be specified in 8-bit units. When used as an input port, an internal pull-up resistor can be connected by software. Test input flag (KRIF) is set to 1 by the falling edge detection.		Input	AD0-AD7
P50-P57	I/O	Port 5 8-bit input/output port. LED can be driven directly. Input/output can be specified bit-wise. When used as an input port, an internal pull-up resistor can be connected by software.		Input	A8-A15
P60	I/O	Port 6 8-bit input/output port. Input/output can be specified bit-wise.	N-ch open drain input/output port. LED can be driven directly.	Input	—
P61					
P62					
P63					
P64		When used as an input port, an internal pull-up resistor can be connected by software.	Input	$\overline{RD}$	
P65				$\overline{WR}$	
P66				$\overline{WAIT}$	
P67				ASTB	
P70	I/O	Port 7 3-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an internal pull-up resistor can be connected by software.		Input	SI2/RxD0
P71					SO2/TxD0
P72					$\overline{SCK2}/ASCK$
P120-P127	I/O	Port 12 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an internal pull-up resistor can be connected by software.		Input	RTP0-RTP7
P130, P131	I/O	Port 13 2-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an internal pull-up resistor can be connected by software.		Input	ANO0, ANO1

2.2 Non-Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt request input by which the effective edge (rising edge, falling edge, or both rising edge and falling edge) can be specified.	Input	P00/TI00
INTP1				P01/TI01
INTP2				P02
INTP3				P03
INTP4				P04
INTP5				P05
SI0	Input	Serial interface serial data input.	Input	P25/SB0
SI1				P20
SI2				P70/RxD
SO0	Output	Serial interface serial data output.	Input	P26/SB1
SO1				P21
SO2				P71/TxD
SB0	I/O	Serial interface serial data input/output.	Input	P25/SI0
SB1				P26/SO0
$\overline{\text{SCK0}}$	I/O	Serial interface serial clock input/output.	Input	P27
$\overline{\text{SCK1}}$				P22
$\overline{\text{SCK2}}$				P72/ASCK
STB	Output	Strobe output for serial interface automatic transmission/reception.	Input	P23/TxD1
BUSY	Input	Busy input for serial interface automatic transmission/reception.	Input	P24/RxD1
RxD0	Input	Serial data input for asynchronous serial interface.	Input	P70/SI2
RxD1				P24/BUSY
TxD0	Output	Serial data output for asynchronous serial interface.	Input	P71/SO2
TxD1				P23/STB
ASCK	Input	Serial clock input for asynchronous serial interface.	Input	P72/ $\overline{\text{SCK2}}$
TI00	Input	External count clock input to 16-bit timer (TM0).	Input	P00/INTP0
TI01		Capture trigger signal input to capture register (CR00).		P01/INTP1
TI1		External count clock input to 8-bit timer (TM1).		P33
TI2		External count clock input to 8-bit timer (TM2).		P34
TO0	Output	16-bit timer output (shared with 14-bit PWM output).	Input	P30
TO1		8-bit timer output.		P31
TO2				P32
PCL	Output	Clock output (for trimming of main system clock and subsystem clock).	Input	P35
BUZ	Output	Buzzer output.	Input	P36
RTP0-RTP7	Output	Real-time output port to output data in synchronization with triggers.	Input	P120-P127
AD0-AD7	I/O	Lower address/data bus for extending memory externally.	Input	P40-P47
A8-A15	Output	Higher address bus for extending memory externally.	Input	P50-P57
$\overline{\text{RD}}$	Output	Strobe signal output for read operation of external memory.	Input	P64
$\overline{\text{WR}}$		Strobe signal output for write operation of external memory.	Input	P65

2.2 Non-Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
WAIT	Input	Inserting wait for accessing external memory.	Input	P66
ASTB	Output	Strobe output which externally latches address information output to port 4 and port 5 to access external memory.	Input	P67
ANI0-ANI7	Input	A/D converter analog input.	Input	P10-P17
ANO0, ANO1	Output	D/A converter analog output.	Input	P130, P131
AV _{REF0}	Input	A/D converter reference voltage input (shared with analog power supply).	—	—
AV _{REF1}	Input	D/A converter reference voltage input.	—	—
AV _{SS}	—	A/D converter ground potential. Voltage equal to V _{SS0} .	—	—
RESET	Input	System reset input.	—	—
X1	Input	Connecting crystal resonator for main system clock oscillation.	—	—
X2	—		—	—
XT1	Input	Connecting crystal resonator for subsystem clock oscillation.	Input	P07
XT2	—		—	—
V _{DD0}	—	Positive power supply voltage for ports.	—	—
V _{SS0}	—	Ground potential of ports.	—	—
V _{DD1}	—	Positive power supply (except ports and analog parts).	—	—
V _{SS1}	—	Ground potential (except ports and analog parts).	—	—
V _{PP}	—	Applying high-voltage for program write/verify. Connected directly to V _{SS0} in normal operation mode.	—	—

2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

Table 2-1 shows the I/O circuit type of each pin and the recommended connection of unused pins.
For the configuration of each I/O circuit type, refer to Figure 2-1.

Table 2-1. I/O Circuit Type of Each Pin (1/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connection when Not Used	
P00/INTP0/TI00	2	Input	Connected to V _{SS0} .	
P01/INTP1/TI01	8-C	I/O	Independently connected to V _{SS0} through a resistor.	
P02/INTP2				
P03/INTP3				
P04/INTP4				
P05/INTP5				
P07/XT1	16	Input	Connected to V _{DD0} .	
P10/ANI0-P17/ANI7	11-D	I/O	Independently connected to V _{DD0} or V _{SS0} through a resistor.	
P20/SI1	8-C			
P21/SO1	5-H			
P22/ $\overline{\text{SCK1}}$	8-C			
P23/STB/TxD1	5-H			
P24/BUSY/RxD1	8-C			
P25/SI0/SB0	10-B			
P26/SO0/SB1				
P27/ $\overline{\text{SCK0}}$				
P30/TO0	5-H			
P31/TO1				
P32/TO2				
P33/TI1	8-C			
P34/TI2				
P35/PCL	5-H			
P36/BUZ				
P37				
P40/AD0-P47/AD7	5-N			Independently connected to V _{DD0} through a resistor.
P50/A8-P57/A15	5-H			Independently connected to V _{DD0} or V _{SS0} through a resistor.
P60-P63	13-K			Independently connected to V _{DD0} through a resistor.
P64/ $\overline{\text{RD}}$	5-H			Independently connected to V _{DD0} or V _{SS0} through a resistor.
P65/ $\overline{\text{WR}}$				
P66/ $\overline{\text{WAIT}}$				
P67/ASTB				
P70/SI2/RxD0	8-C			
P71/SO2/TxD0	5-H			
P72/ $\overline{\text{SCK2}}$ /ASCK	8-C			
P120/RTP0-P127/RTP7	5-H			
P130/ANO0, P131/ANO1	12-C			Independently connected to V _{SS0} through a resistor.

Table 2-1. I/O Circuit Type of Each Pin (2/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connection when Not Used
RESET	2	Input	–
XT2	16	–	Open
AVREF0	–		Connected to VSS0.
AVREF1			Connected to VDD0.
AVSS			Connected to VSS0.
VPP			Connected directly to VSS0.

Figure 2-1. List of Pin I/O Circuits (1/2)

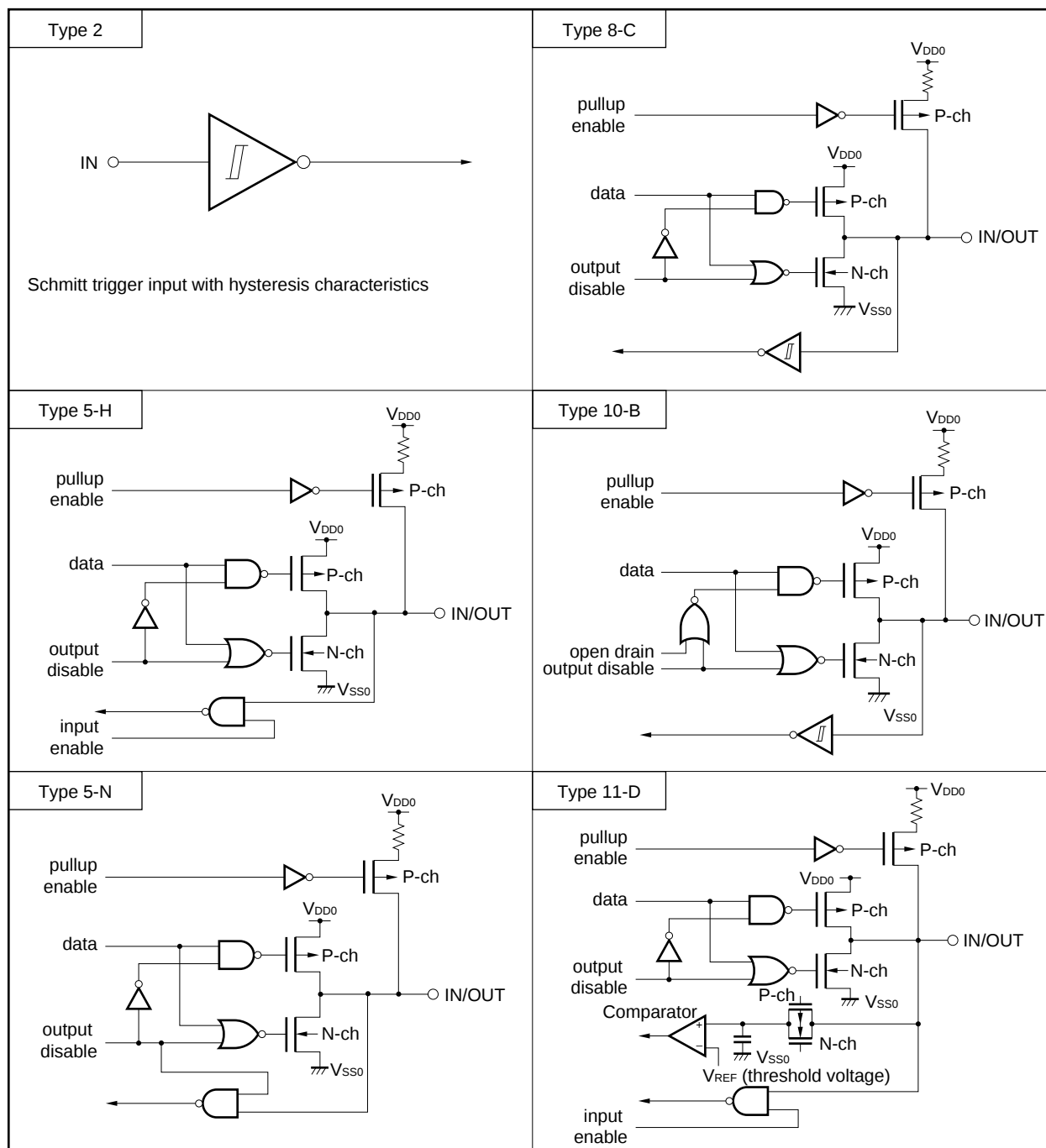
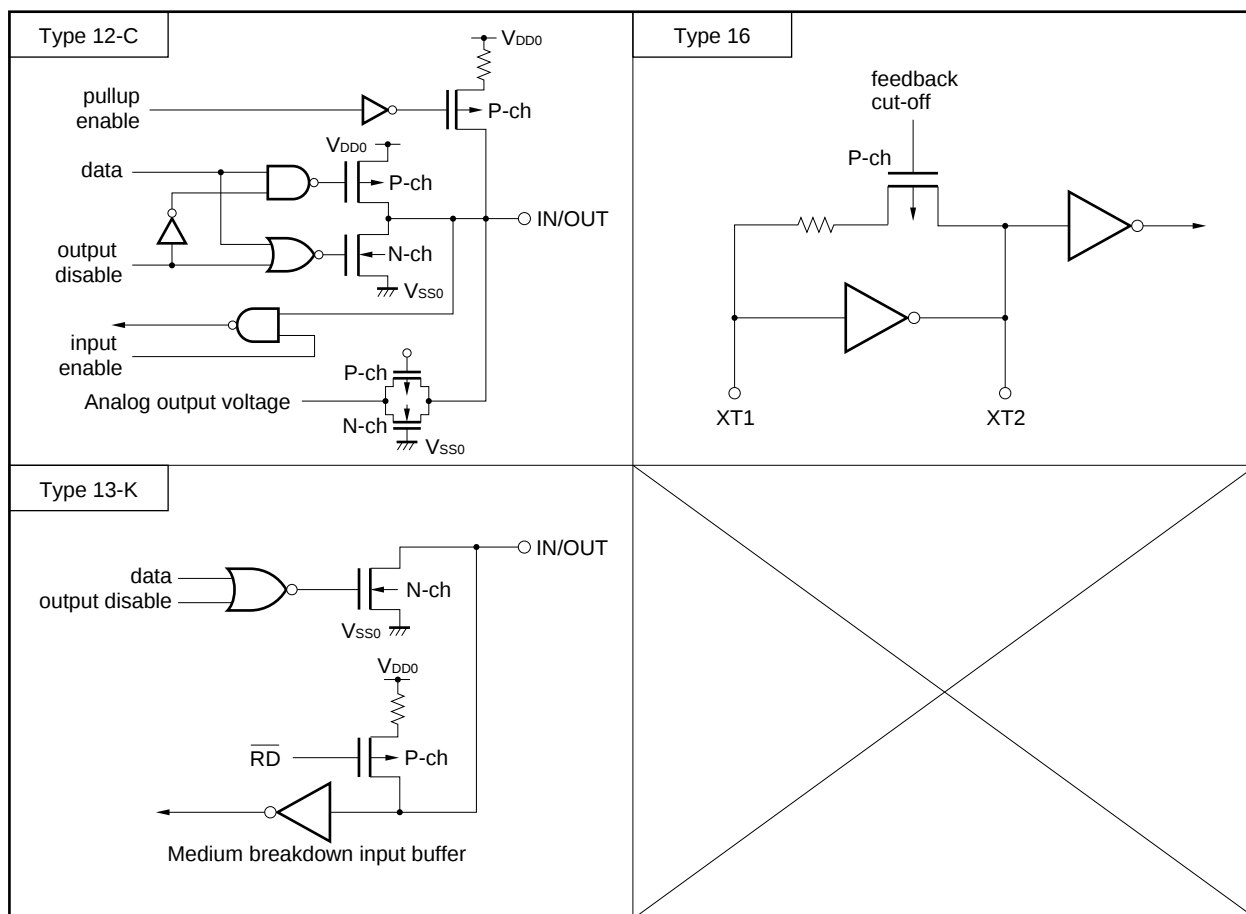


Figure 2-1. List of Pin I/O Circuits (2/2)



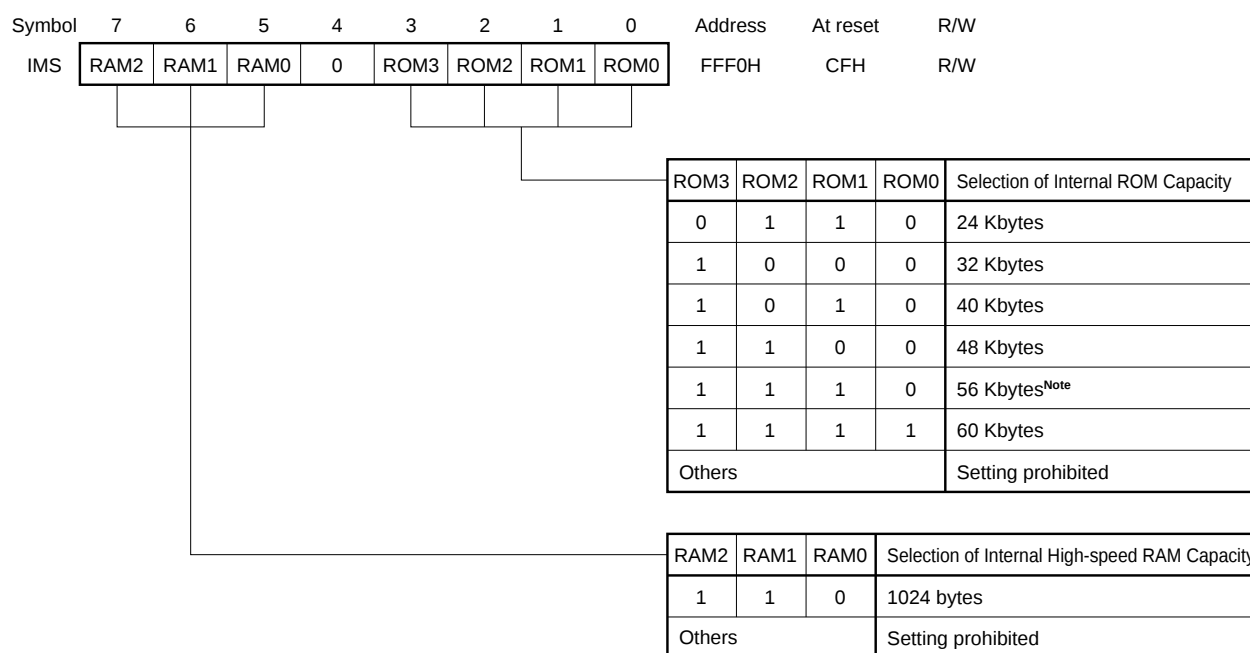
3. MEMORY SIZE SWITCHING REGISTER (IMS)

This register sets a part of internal memory unused by software. The memory mapping can be made the same as that of mask ROM versions with different types of internal memory (ROM and RAM) by setting the memory size switching register (IMS).

The IMS is set with an 8-bit memory manipulation instruction.

RESET input sets the IMS to CFH.

Figure 3-1. Format of Memory Size Switching Register



Note When using external device expansion function, set the internal ROM capacity to less than 56 Kbytes.

Table 3-1 shows the IMS set value to make the memory mapping the same as those of mask ROM versions.

Table 3-1. Set Value of Memory Size Switching Register

Target Mask ROM Versions	IMS Set Value
μPD780053	C6H
μPD780054	C8H
μPD780055	CAH
μPD780056	CCH
μPD780058	CFH

4. INTERNAL EXPANSION RAM SIZE SWITCHING REGISTER (IXS)

This register sets the internal expansion RAM capacity by software. The memory mapping can be made the same as that of mask ROM versions with different types of internal expansion RAM by setting the internal expansion RAM size switching register (IXS).

The IXS is set with an 8-bit memory manipulation instruction.

RESET input sets the IXS to 0AH.

Figure 4-1. Format of Internal Expansion RAM Size Switching Register

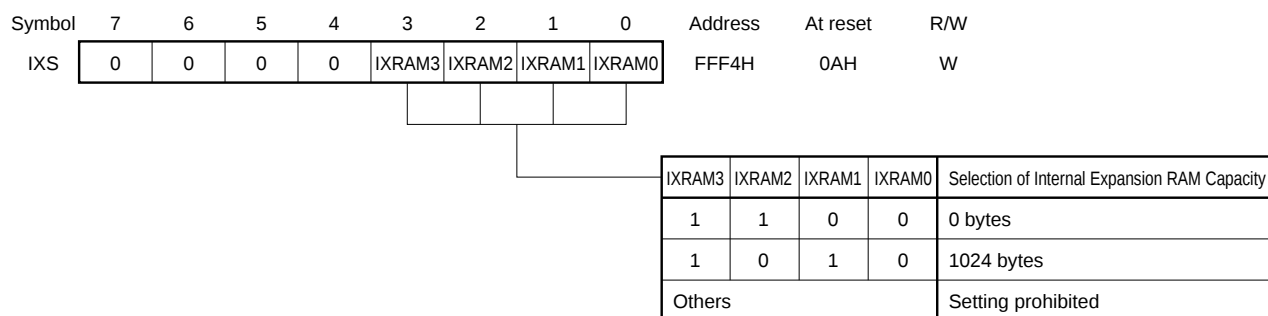


Table 4-1 shows the IXS set value to make the memory mapping the same as those of mask ROM versions.

Table 4-1. Set Value of Internal Expansion RAM Size Switching Register

Target Mask ROM Versions	IMS Set Value
μPD780053	0CH
μPD780054	
μPD780055	
μPD780056	
μPD780058	0AH

Remark Even if a μPD78F0058 program in which MOV IXS, #0CH is written is executed on the μPD780055 and 780056, the operation will not be affected.

5. FLASH MEMORY PROGRAMMING

Writing to a flash memory can be performed without removing the memory from the target system (on-board). Writing is performed connecting the dedicated flash programmer (Flashpro) to the host machine and the target system.

Remark Flashpro is a product of Naitou Densai Machidaseisakusho Co., Ltd.

5.1 Selection of Transmission Method

Writing to a flash memory is performed using the Flashpro with a serial transmission mode. One of the transmission method is selected from those in Table 5-1. The selection of the transmission method is made by using the format shown in Figure 5-1. Each transmission method is selected by the number of V_{PP} pulses shown in Table 5-1.

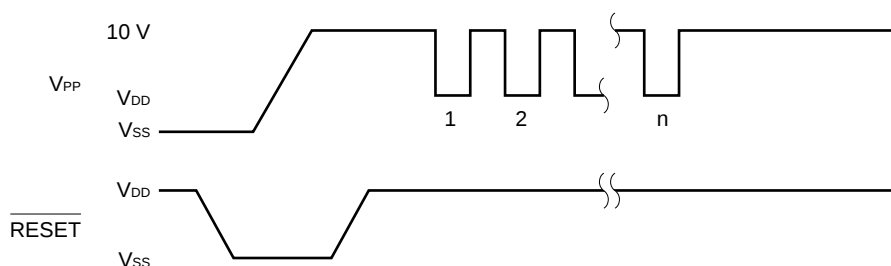
Table 5-1. List of Transmission Method

Transmission Method	Channels	Pin	V_{PP} Pulses
3-wired serial I/O	3	P27/ $\overline{SCK0}$ P26/SO0/SB1 P25/SI0/SB0	0
		P22/ $\overline{SCK1}$ P21/SO1 P20/SI1	1
		P72/ $\overline{SCK2}/\overline{ASCK}$ P71/SO2/TxD0 P70/SI1/RxD0	2
UART	2	P71/SO2/TxD0 P70/SI2/RxD0	8
		P23/TxD1 P24/RxD1	9
Pseudo 3-wired serial I/O ^{Note}	1	P32/TO2 (serial clock input/output) P31/TO1 (serial data output) P30/TO0 (serial data input)	12

Note Serial transmission is performed by controlling the port using software.

Caution Select a communication system always using the number of V_{PP} pulses shown in Table 5-1.

Figure 5-1. Format of Transmission Method Selection



5.2 Function of Flash Memory Programming

Operations such as writing to a flash memory are performed by various command/data transmission and reception operations according to the selected transmission method. Table 5-2 shows major functions of flash memory programming.

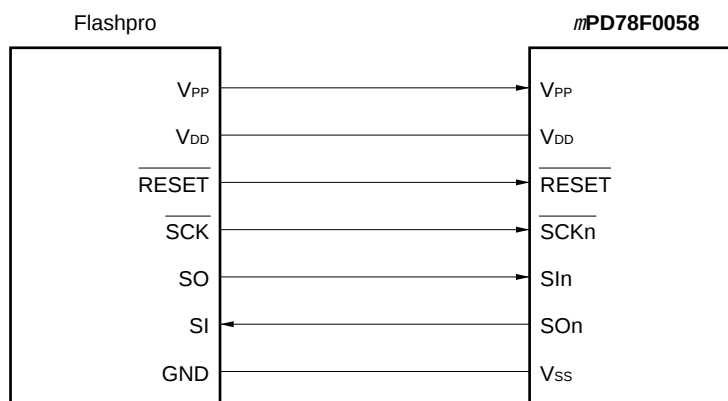
Table 5-2. Major Functions of Flash Memory Programming

Functions	Descriptions
Reset	Used to stop write operation and detect transmission cycle.
Batch verify	Compares the entire memory contents with the input data.
Block verify	Compares the contents of the specified memory blocks with the input data.
Batch delete	Deletes the entire memory contents.
Block delete	Deletes the contents of the specified memory block, setting 16 Kbytes as one memory block.
Convergence	Prevents over-deletion.
Batch blank check	Checks the deletion status of the entire memory.
Block blank check	Checks the deletion status of the specified block.
High-speed write	Performs write to the flash memory based on the write start address and the number of data to be written (number of bytes).
Continuous write	Performs continuous write based on the information input with high-speed write operation.
Status	Used to confirm the current operating mode and operation end.
Oscillation frequency setting	Sets the frequency of the resonator.
Delete time setting	Sets the memory delete time.
Baud rate setting	Sets the transmission rate in transmission using UART system.
Convergence time setting	Sets the correction time in convergence.
Silicon signature read	Outputs the device name and memory capacity, and device block information.

5.3 Connection of Flashpro

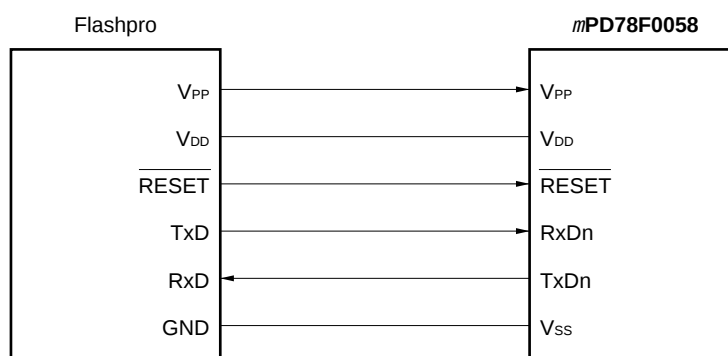
The connection of the Flashpro and the μ PD78F0058 differs according to the transmission method. The connection for each transmission method is shown in Figures 5-2 to 5-4.

Figure 5-2. Connection of Flashpro for 3-wired Serial I/O System



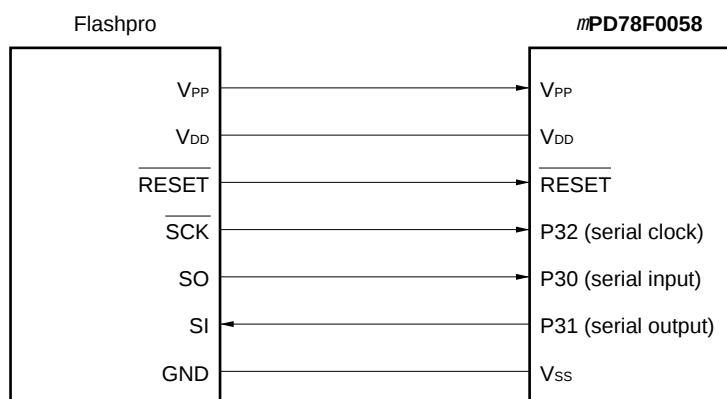
n = 0-2

Figure 5-3. Connection of Flashpro for UART System



n = 0, 1

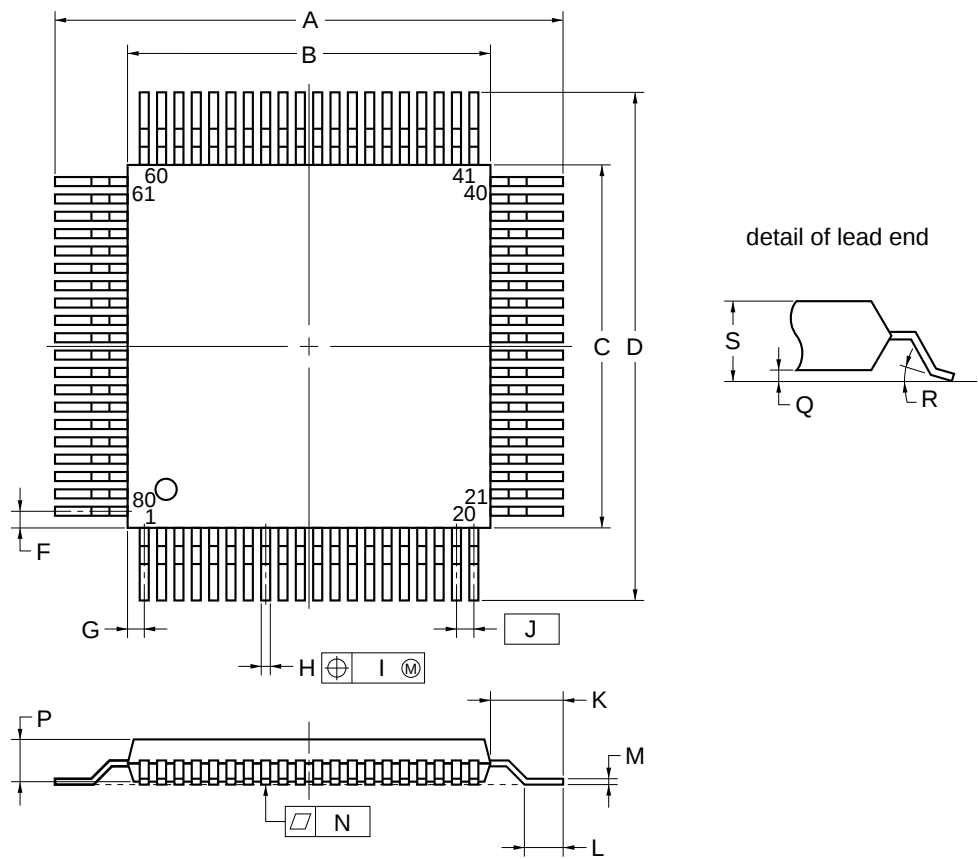
Figure 5-4. Connection of Flashpro for Pseudo 3-wired Serial I/O System



6. PACKAGE DRAWINGS

80-pin plastic QFP (14 × 14) (Unit: mm)

80 PIN PLASTIC QFP (14 · 14)



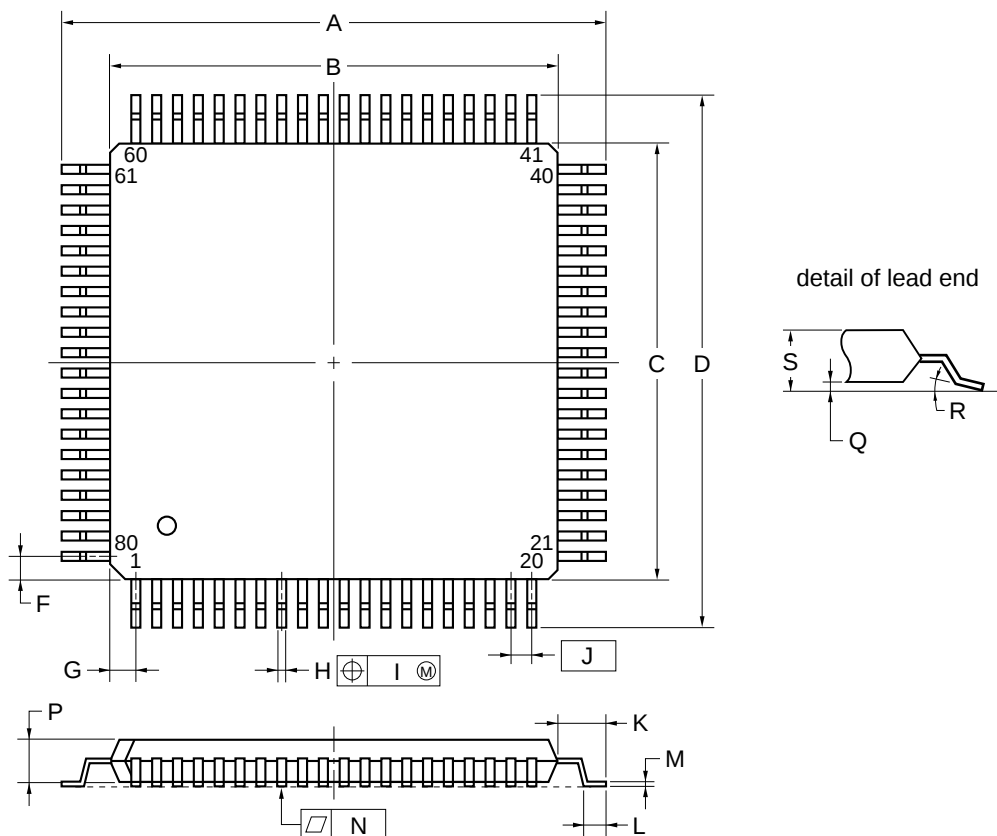
NOTE
Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	0.551 ^{+0.009} _{-0.008}
C	14.0±0.2	0.551 ^{+0.009} _{-0.008}
D	17.2±0.4	0.677±0.016
F	0.825	0.032
G	0.825	0.032
H	0.30±0.10	0.012 ^{+0.004} _{-0.005}
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	0.031 ^{+0.009} _{-0.008}
M	0.15 ^{+0.10} _{-0.05}	0.006 ^{+0.004} _{-0.003}
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5° ±5°	5° ±5°
S	3.0 MAX.	0.119 MAX.

S80GC-65-3B9-4

80-pin plastic QFP (14 × 14) (Unit: mm)

80 PIN PLASTIC QFP (14 · 14)



NOTE

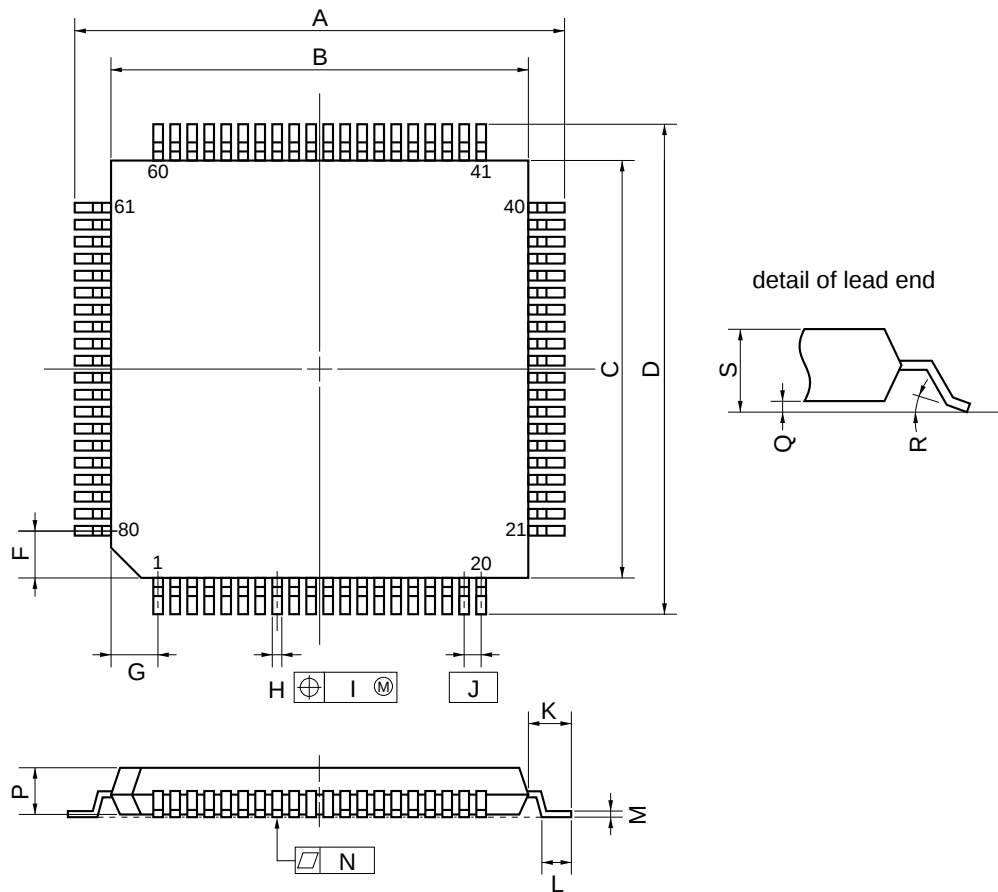
Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.20±0.20	0.677±0.008
B	14.00±0.20	0.551 ^{+0.009} _{-0.008}
C	14.00±0.20	0.551 ^{+0.009} _{-0.008}
D	17.20±0.20	0.677±0.008
F	0.825	0.032
G	0.825	0.032
H	0.32±0.06	0.013 ^{+0.002} _{-0.003}
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.60±0.20	0.063±0.008
L	0.80±0.20	0.031 ^{+0.009} _{-0.008}
M	0.17 ^{+0.03} _{-0.07}	0.007 ^{+0.001} _{-0.003}
N	0.10	0.004
P	1.40±0.10	0.055±0.004
Q	0.125±0.075	0.005±0.003
R	3° ^{+7°} _{-3°}	3° ^{+7°} _{-3°}
S	1.70 MAX.	0.067 MAX.

P80GC-65-8BT

80-pin plastic TQFP (fine pitch) (12 × 12) (Unit: mm)

80 PIN PLASTIC TQFP (FINE PITCH) (□12)



NOTE
Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.0±0.2	0.551 ^{+0.009} _{-0.008}
B	12.0±0.2	0.472 ^{+0.009} _{-0.008}
C	12.0±0.2	0.472 ^{+0.009} _{-0.008}
D	14.0±0.2	0.551 ^{+0.009} _{-0.008}
F	1.25	0.049
G	1.25	0.049
H	0.22 ^{+0.05} _{-0.04}	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	0.039 ^{+0.009} _{-0.008}
L	0.5±0.2	0.020 ^{+0.008} _{-0.009}
M	0.145 ^{+0.055} _{-0.045}	0.006±0.002
N	0.10	0.004
P	1.05	0.041
Q	0.05±0.05	0.002±0.002
R	5°±5°	5°±5°
S	1.27 MAX.	0.050 MAX.

P80GK-50-BE9-4

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78F0058.

Language Processing Software

RA78K/0 ^{Notes 1, 2, 3, 4}	78K/0 Series common assembler package
CC78K/0 ^{Notes 1, 2, 3, 4}	78K/0 Series common C compiler package
DF780058 ^{Notes 1, 2, 3, 4, 8}	Device file for μPD780058 Subseries
CC78K/0-L ^{Notes 1, 2, 3, 4}	78K/0 Series common C compiler library source file

Flash Memory Writing Tools

Flashpro II (FL-PR2)	Dedicated flash writer Product of Naitou Densai Machidaseisakusho Co., Ltd.
FA-80GC ^{Note 8}	Adapter for flash memory writing
FA-80GK ^{Note 8}	Product of Naitou Densai Machidaseisakusho Co., Ltd.

Debugging Tool

IE-78000-R	78K/0 Series common in-circuit emulator
IE-78000-R-A	78K/0 Series common in-circuit emulator (for integrated debugger)
IE-78000-R-BK	78K/0 Series common brake board
IE-780308-R-EM	μPD780308 Subseries common emulation board
EP-780058GC-R ^{Note 8}	Emulation probe for μPD780058 Subseries
EV-9200GC-80	Socket to be mounted on a target system board made for the 80-pin plastic QFP (GC-3B9, GC-8BT type)
EP-780058GK-R ^{Note 8}	Emulation probe for μPD780058 Subseries
TGK-080SDW	Adapter to be mounted on a target system board made for the 80-pin plastic QFP (GK-BE9 type) Product of TOKYO ELETECH Corporation Consult NEC sole agent for purchase.
SM78K/0 ^{Notes 5, 6, 7}	78K/0 Series common system simulator
ID78K/0 ^{Notes 4, 5, 6, 7}	Integrated debugger for IE-78000-R-A
SD78K/0 ^{Notes 1, 2}	Screen debugger for IE-78000-R
DF780058 ^{Notes 1, 2, 3, 4, 5, 6, 7, 8}	Device file for μPD780058 Subseries

- Notes**
1. PC-9800 Series (MS-DOS™) based
 2. IBM PC/AT™ and compatibles (PC DOS™/IBM DOS™/MS-DOS) based
 3. HP9000 Series 300™ (HP-UX™) based
 4. HP9000 Series 700™ (HP-UX) based, SPARCstation™ (SunOS™) based, EWS4800 Series (EWS-UX/V) based
 5. PC-9800 Series (MS-DOS + Windows™) based
 6. IBM PC/AT and compatibles (PC-DOS/IBM DOS/MS-DOS + Windows) based
 7. NEWS™ (NEWS-OS™) based
 8. Under development

Real-time OS

RX78K/0 ^{Notes 1, 2, 3, 4}	78K/0 Series real-time OS
MX78K0 ^{Notes 1, 2, 3, 4}	78K/0 Series OS

Fuzzy Inference Development Support System

FE9000 ^{Note 1} /FE9200 ^{Note 5}	Fuzzy knowledge data creation tool
FT9080 ^{Note 1} /FT9085 ^{Note 2}	Translator
FI78K ^{Notes 1, 2}	Fuzzy inference module
FD78K0 ^{Notes 1, 2}	Fuzzy inference debugger

Notes 1. PC-9800 Series (MS-DOS) based

2. IBM PC/AT and compatibles (PC DOS/IBM DOS/MS-DOS) based

3. HP9000 Series 300 (HP-UX) based

4. HP9000 Series 700 (HP-UX) based, SPARCstation (SunOS) based, EWS4800 Series (EWS-UX/V) based

5. IBM PC/AT and compatibles (PC DOS/IBM DOS/MS-DOS + Windows) based

Remarks 1. For third party development tools, refer to the 78K/0 Series Selection Guide (U11126E)

2. The RA78K/0, CC78K/0, SM78K0, ID78K0, SD78K/0, and RX78K/0 are used in combination with the DF780058.

APPENDIX B. RELATED DOCUMENTS

Device Related Documents

Document Name	Document No.	
	Japanese	English
μPD780058, 780058Y Subseries User's Manual	U12013J	Planned
μPD780053, 780054, 780055, 780056, 780058 Preliminary Product Information	U12182J	Planned
μPD78F0058 Preliminary Product Information	U12092J	This manual
78K/0 Series User's Manual Instruction	IEU-849	IEU-1372
78K/0 Series Instruction Table	U10903J	–
78K/0 Series Instruction Set	U10904J	–

Development Tools Documents (User's Manual)

Document Name		Document No.	
		Japanese	English
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
CC78K0 C Compiler	Operation	U11517J	U11517E
	Language	U11518J	U11518E
CC78K/0 C Compiler Application Note	Programming Know-how	EEA-618	EEA-1208
CC78K Series Library Source File		EEU-777	–
IE-78000-R		EEU-810	U11376E
IE-78000-R-A		U10057J	U10057E
IE-78000-R-BK		EEU-867	EEU-1427
IE-78308-R-EM		U11362J	U11362E
EP-780058GC-R		Planned	Planned
EP-780058GK-R		Planned	Planned
SM78K0 System Simulator Windows based	Reference	U10181J	U10181E
SM78K Series System Simulator	External Parts User Open Interface Specification	U10092J	U10092E
ID78K0 Integrated Debugger EWS based	Reference	U11151J	–
ID78K0 Integrated Debugger PC based	Reference	U11539J	U11539E
ID78K0 Integrated Debugger Windows based	Guide	U11649J	U11649E
SD78K0 Screen Debugger	Introduction	EEU-852	–
PC-9800 Series (MS-DOS) based	Reference	U10952J	–
SD78K/0 Screen Debugger	Guide	EEU-5024	EEU-1414
IBM PC/AT (PC DOS) based	Reference	U11279J	U11279E

Caution The contents of the above related documents are subject to change without notice. The latest documents should be used for design, etc.

Embedded Software Documents (User's Manual)

Document Name		Document No.	
		Japanese	English
78K/0 Series Real-time OS	Basic	U11537J	—
	Installation	U11536J	—
	Technical	U11538J	—
OS for 78K/0 Series MX78K0	Basic	EEU-5010	—
Fuzzy Knowledge Data Creation Tool		EEU-829	EEU-1438
78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System Translator		EEU-862	EEU-1444
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Module		EEU-858	EEU-1441
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Debugger		EEU-921	EEU-1458

Other Documents

Document Name		Document No.	
		Japanese	English
IC PACKAGE MANUAL		C10943X	
Semiconductor Device Mounting Technology Manual		C10535J	C10535E
Quality Grade on NEC Semiconductor Devices		C11531J	C11531E
Reliable Quality Maintenance on NEC Semiconductor Devices		C10983J	C10983E
Electrostatic Discharge (ESD) Test		MEM-539	—
Semiconductor Devices Quality Guarantee Guide		C11893J	MEI-1202
Microcomputer Product Series Guide		U11416J	—

Caution The contents of the above related documents are subject to change without notice. The latest documents should be used for design, etc.

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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Santa Clara, California
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Fax: 800-729-9288

NEC Electronics (Germany) GmbH

Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

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Milton Keynes, UK
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Fax: 01908-670-290

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NEC devices are classified into the following three quality grades:

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Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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Anti-radioactive design is not implemented in this product.