NEC

MOS INTEGRATED CIRCUIT

μPD78P9014

8-bit Single-Chip Microcontroller

μPD78P9014 is a product in the μPD789014 Subseries of compact, general-purpose microcontrollers in the 78K/0S Series.

In addition to an 8-bit CPU, this product has substantial hardware such as on-chip I/O ports, timers, serial interface, and interrupt controls.

This PROM product incorporates one-time PROM that can be written only once.

Since user can write programs, this microcontroller is best suited for evaluation during development, multi-product small-volume production, and rapid start up.

These user's manuals contain detailed descriptions of the functions. Be sure to read them before designing.

μPD78P9014 Subseries User's Manual: U11187E
78K/0S Series User's Manual - Instruction: U11047E

FEATURES

- Pin compatible with mask ROM products (except for the V_{PP} pin)
- On-chip one-time PROM: 8K bytes
- On-chip high-speed RAM: 256 bytes
- Can change the minimum instruction execution time to the fast speed (0.4 μs) and the low speed (1.6 μs)
- I/O ports: 22
- Serial interface: 1 channel
  Can select the three-wire serial I/O mode or the UART mode
- Timers: 3 channels
  - 8-bit timer/event counter: 2 channels
  - Watchdog timer: 1 channel
- Operation possible at the same power supply voltage as in mask ROM products (V_{DD} = 1.8 to 5.5 V)
- Compatible with the QTOP™ microcontroller

Remarks QTOP microcontroller is the name of the on-chip one-time PROM microcontroller fully supported by the NEC write service (sealing from the write, screening, inspection).

APPLICATION FIELDS

Compact household appliances, remote controls, games, etc.

ORDERING INFORMATION

Part Number	Package
μPD78P9014CT	28-pin plastic shrink DIP (400 mils)
μPD78P9014GT	28-pin plastic SOP (375 mils)

The information in this document is subject to change without notice.

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Printed in Japan

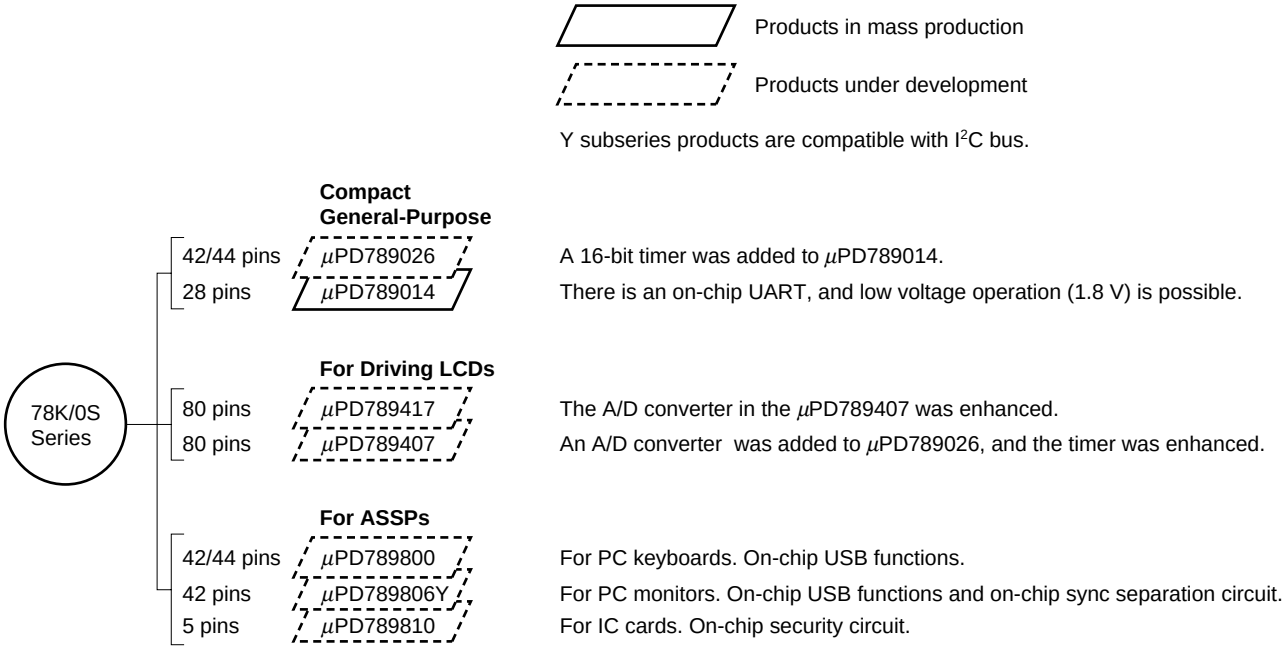
The mark ★ shows major revised points.

OVERVIEW OF THE FEATURES

Item		Function
On-chip memory	One-time PROM	8K bytes
	High-speed RAM	256 bytes
General-purpose registers		8 bits × 8 registers
Minimum instruction execution time		0.4 μs or 1.6 μs (main system clock: 5.0 MHz operation)
Instruction set		• 16-bit calculations • Bit manipulation (set, reset, test)
I/O ports		CMOS I/O: 22
Serial interface		Can select the three-wire serial I/O mode or the UART mode: 1 channel
Timers		• 8-bit timer/event counter: 2 channels • Watchdog timer: 1 channel
Timer output		2
Vector interrupt source	Maskable	Internal: 6, External: 3
	Nonmaskable	Internal: 1
Power supply voltage		V_{DD} = 1.8 to 5.5 V
Ambient operating temperature		T_A = -40 to +85°C
Package		• 28-pin plastic shrink DIP (400 mils) • 28-pin plastic SOP (375 mils)

78K/0S Series Expansion

The following shows the 78K/0S Series products development. Subseries names are shown inside frames.



The following lists the main functional differences between subseries products.

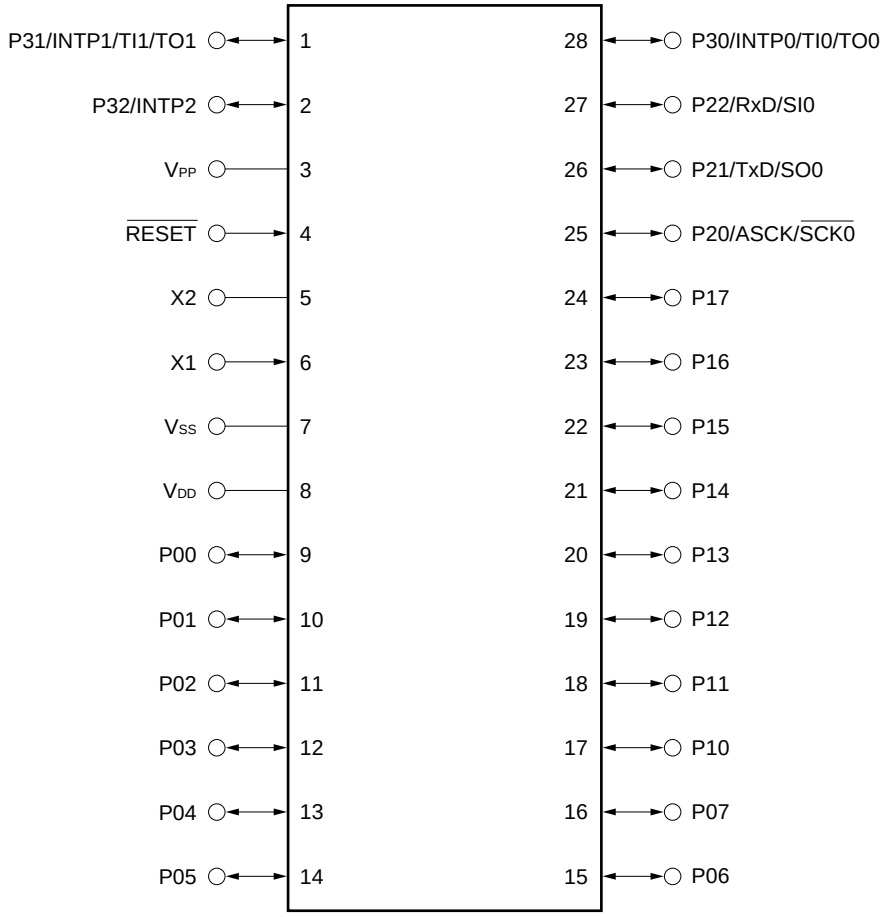
Subseries Name / Function		ROM Capacity	Timers				8-bit A/D	10-bit A/D	8-bit D/A	Serial Interface	I/O	Minimum V_{DD}
			8-bit	16-bit	Watch	WDT						
Compact, general-purpose	μPD789026	4K-16K	1ch	1ch	–	1ch	–	–	–	1ch (UART :1 ch)	34	1.8 V
	μPD789014	2K-4K	2ch	–							22	
For LCD driving	μPD789417	12K-24K	3ch	1ch	1ch	1ch	–	7ch	–	1ch (UART : 1ch)	43	1.8 V
	μPD789407	12K-24K					7ch	–				
For ASSP	μPD789800	8K	2ch	–	–	1ch	–	–	–	2ch (USB : 1ch)	31	4.0 V
	μPD789806Y	16K	2ch	–	–	1ch	–	–	–	2ch (USB : 1ch, I²C : 1ch)	20	4.5 V
	μPD789810	6K	–	–	–	1ch	–	–	–	–	1	1.8 V

CONTENTS

1. PIN CONNECTION DIAGRAM (Top View)

(1) Normal operating modes

- **28-pin plastic shrink DIP (400 mils)**
  μPD78P9014CT
- **28-pin plastic SOP (375 mils)**
  μPD78P9014GT

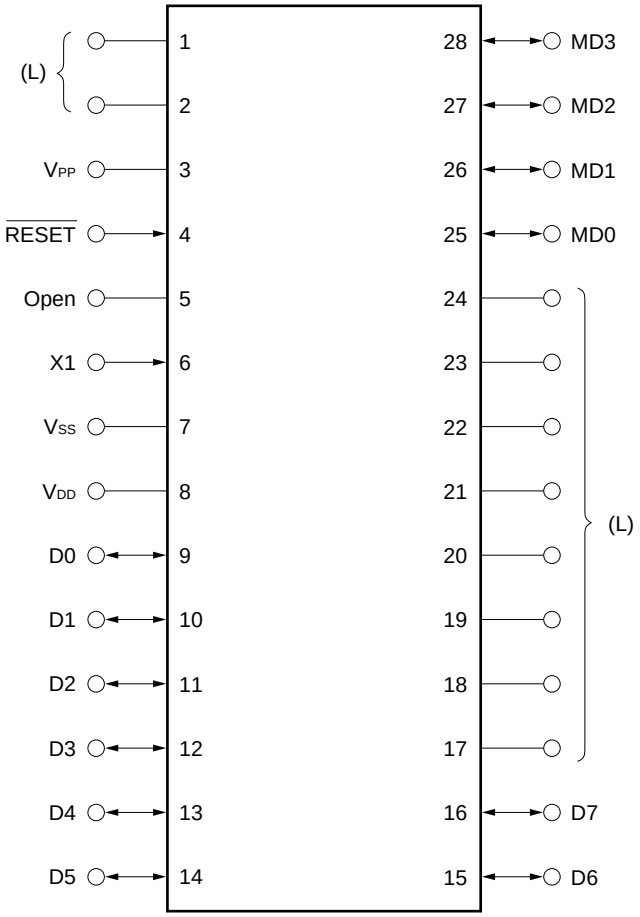


Caution Directly connect V_{PP} to V_{SS}.

ASCK	:	Asynchronous Serial Clock	SI0	:	Serial Input
INTP0-INTP2	:	Interrupt from Peripherals	SO0	:	Serial Output
P00-P07	:	Port0	TI0, TI1	:	Timer Input
P10-P17	:	Port1	TO0, TO1	:	Timer Output
P20-P22	:	Port2	TxD	:	Transmit Data
P30-P32	:	Port3	V_{DD}	:	Power Supply
$\overline{\text{RESET}}$	:	Reset	V_{PP}	:	Programming Power Supply
RxD	:	Receive Data	V_{SS}	:	Ground
$\overline{\text{SCK0}}$	:	Serial Clock	X1, X2	:	Crystal

(2) PROM programming mode

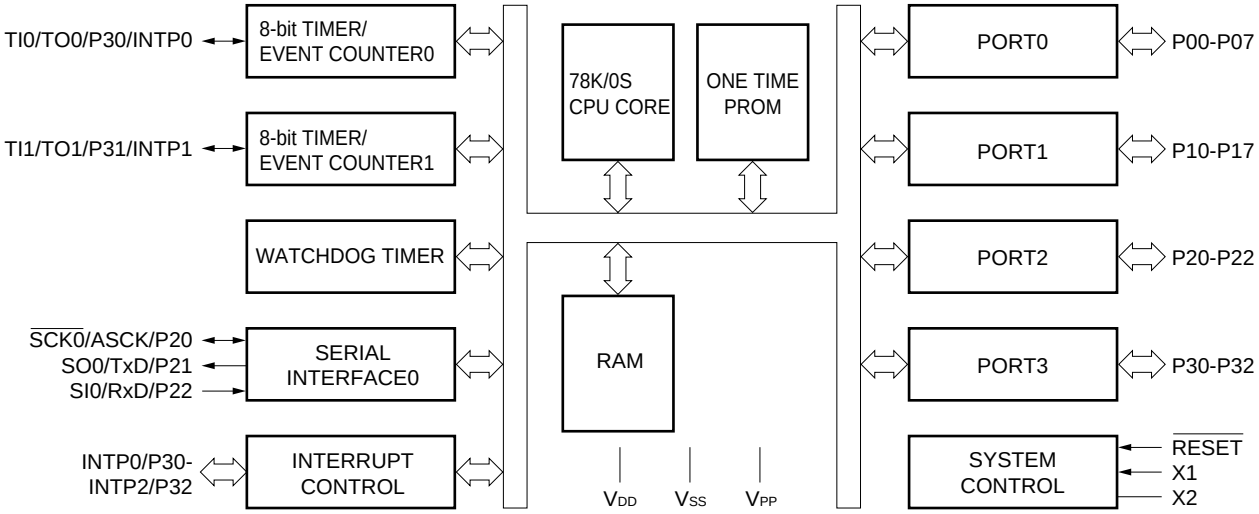
- **28-pin plastic shrink DIP (400 mils)**
  μPD78P9014CT
- **28-pin plastic SOP (375 mils)**
  μPD78P9014GT



Cautions 1. (L) : Individually connect to V_{SS} via a pull-down resistor.
2. V_{SS} : Connect to ground.
3. $\overline{RESET}$: Set to the low level.
4. Open : Leave open.

D0-D7	: Data Bus	V_{DD}	: Power Supply
MD0-MD3	: Programming Mode Select	V_{PP}	: Programming Power Supply
$\overline{RESET}$	: Reset	V_{SS}	: Ground
		X1	: Programming Clock Input

2. BLOCK DIAGRAM



3. DIFFERENCES BETWEEN THE μPD78P9014 AND MASK ROM PRODUCTS

μPD78P9014 is a product with an on-chip one-time PROM that can only be written once.
Table 3-1 lists the differences between the μPD78P9014 and mask ROM products.

Table 3-1. Differences Between the μPD78P9014 and Mask ROM Products

Item		One-Time PROM Product	Mask ROM Products	
		μPD78P9014	μPD789011	μPD789012
On-chip memory	ROM	8K bytes	2K bytes	4K bytes
	High-speed RAM	256 bytes	128 bytes	

4. PIN FUNCTION LIST

4.1 Pins in the Normal Operating Mode

(1) Port pins

Pin Name	I/O	Function	On Reset	Alternate Function Pin
P00-P07	I/O	Port 0 8-bit I/O port Input/output specifiable bit-wise When used as an input port, on-chip pull-up resistor can be used by software. LEDs can be directly driven.	Input	–
P10-P17	I/O	Port 1 8-bit I/O port Input/output specifiable bit-wise When used as an input port, on-chip pull-up resistor can be used by software. LEDs can be directly driven.	Input	–
P20	I/O	Port 2 3-bit I/O port Input/output specifiable bit-wise When used as an input port, on-chip pull-up resistor can be used by software. LEDs can be directly driven.	Input	ASCK/$\overline{\text{SCK0}}$
P21				TxD/SO0
P22				RxD/SI0
P30	I/O	Port 3 3-bit I/O port Input/output specifiable bit-wise When used as an input port, on-chip pull-up resistor can be used by software. LEDs can be directly driven.	Input	INTP0/TI0/TO0
P31				INTP1/TI1/TO1
P32				INTP2

(2) Pins not in the ports

Pin Name	I/O	Function	On Reset	Alternate Function Pin
INTP0[Note]	Input	External interrupt input whose valid edge can be specified (rising edge, falling edge, or both the rising and falling edges)	Input	P30/TI0/TO0
INTP1[Note]				P31/TI1/TO1
INTP2[Note]				P32
SI0[Note]	Input	Serial data input in the serial interface	Input	P22/RxD
SO0	Output	Serial data output in the serial interface	Input	P21/TxD
$\overline{\text{SCK0}}$[Note]	I/O	Serial clock I/O for the serial interface	Input	P20/ASCK
RxD[Note]	Input	Serial data input for the asynchronous serial interface	Input	P22/SI0
TxD	Output	Serial data output for the asynchronous serial interface	Input	P21/SO0
ASCK[Note]	Input	Serial clock input for the asynchronous serial interface	Input	P20/SCK0
TI0[Note]	Input	External count clock input to the 8-bit timer (TM0)	Input	P30/INTP0/TO0
TI1[Note]		External count clock input to the 8-bit timer (TM1)		P31/INTP1/TO1
TO0	Output	8-bit timer output	Input	P30/INTP0/TI0
TO1				P31/INTP1/TI1
$\overline{\text{RESET}}$	Input	System reset input	Input	–
X1	Input	Crystal connection for the main system clock oscillation	–	–
X2	–		–	–
V_{DD}	–	Positive power supply	–	–
V_{PP}	–	High voltage applied when writing or verifying programs. In the normal operating mode, this is directly connected to V_{SS}.	–	–
V_{SS}	–	Ground potential	–	–

★ **Note** These pins are input through Schmitt triggers. (See **Type 5-D in Figure 4-1, "Pin I/O Circuit Types**.")

4.2 Pins in the PROM Programming Mode

Pin Name	I/O	Function
$\overline{\text{RESET}}$	Input	Connect to V_{SS}.
V_{PP}	Input	High voltage applied when setting the PROM programming mode and when writing a program or verifying. ★ If +5.5 V is applied to the V_{DD} pin and +12.5 V is applied to the V_{PP} pin, the PROM programming mode is entered.
MD0-MD3	I/O	Select the operating mode when in the PROM programming mode.
D0-D7	I/O	Data bus
X1	Input	Clock input for address updating in the PROM programming mode
V_{DD}	–	PROM programming mode setting and the positive power supply
V_{SS}	–	Ground potential

4.3 Pin I/O Circuit and Unused Pin Connections

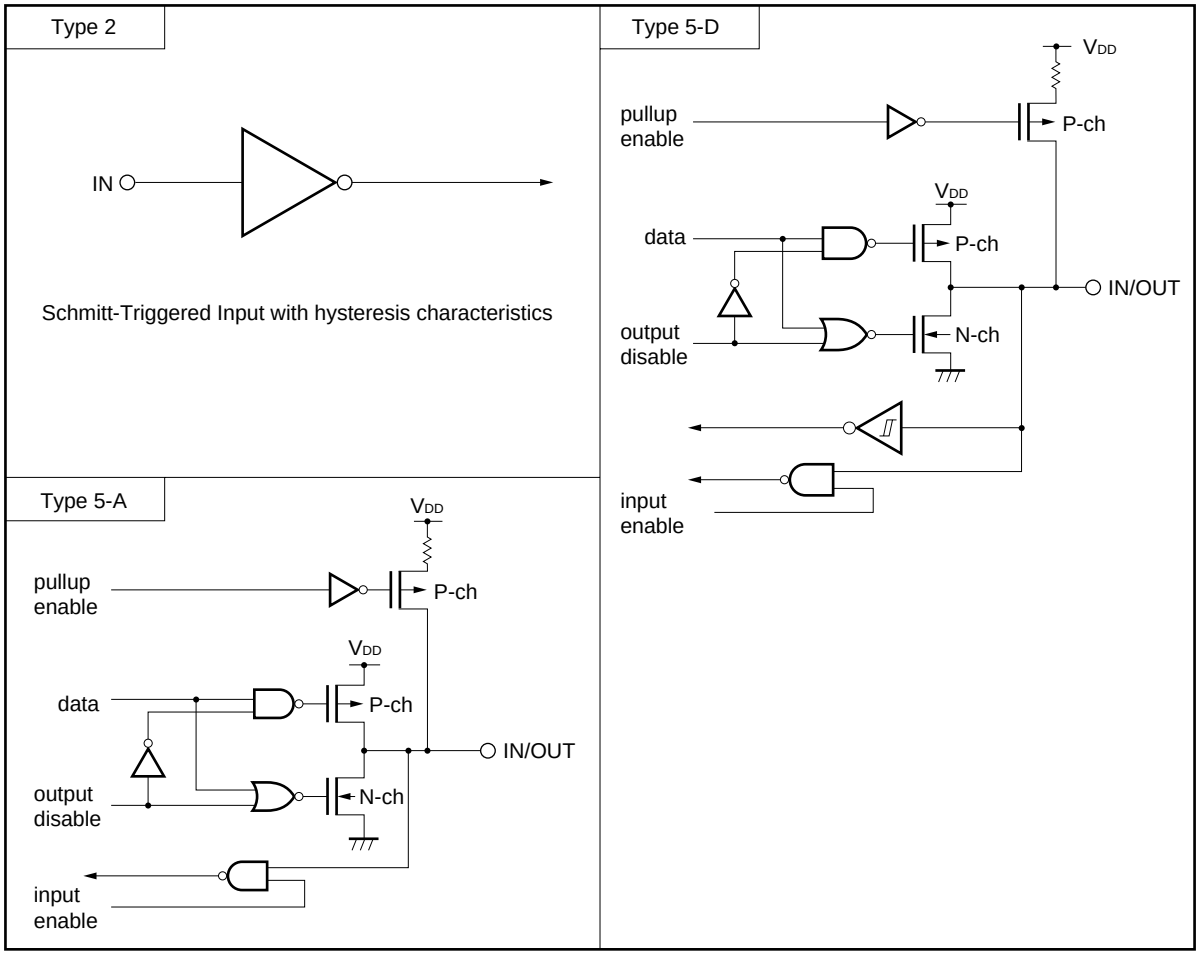
Table 4-1 shows the types of the I/O circuits of each pin and the connections for unused pins.

See Figure 4-1 for the structure of each type of I/O circuit.

Table 4-1. Types of Pin I/O Circuits

Pin Name	I/O Circuit Type	I/O	Recommended Connection for Unused Pin
P00-P07	5-A	I/O	Connect to V_{DD} or V_{SS} through a separate resistor.
P10-P17			
P20/ASCK/$\overline{SCK0}$	5-D		
P21/TxD/SO0	5-A		
P22/RxD/SI0	5-D		
P30/INTP0/TI0/TO0			Connect to V_{SS} through a separate resistor.
P31/INTP1/TI1/TO1			
P32/INTP2			
$\overline{RESET}$	2	–	–
V_{PP}	–	–	Connect directly to V_{SS}.

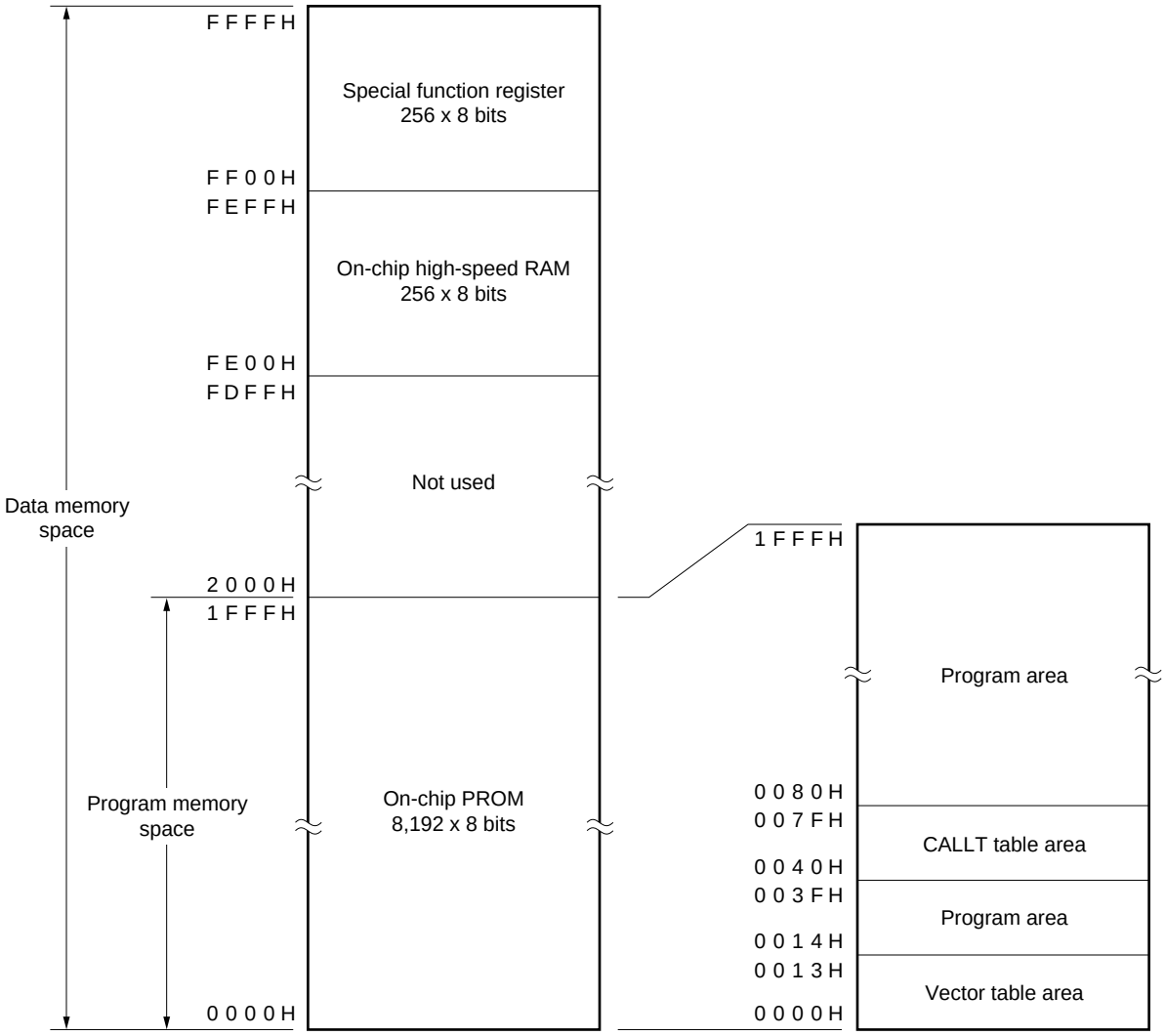
Figure 4-1. Summary of the Pin I/O Circuits



5. MEMORY SPACE

Figure 5-1 shows the μPD78P9014 memory map.

Figure 5-1. Memory Map



6. OVERVIEW OF THE INSTRUCTION SET

The μPD78P9014 instruction set is shown in the table below.

6.1 Legend

6.1.1 Operand identifiers and methods of use

Operands are described in “Operand” column of each instruction in accordance with the description method of the instruction operand identifier (refer to the assembler specifications for detail). When there are two or more description methods, select one of them. Alphabetic letters in capitals and symbols, #, !, $, and [ ] are keywords and must be described as they are. Each symbol has the following meaning.

- # : Immediate data specification
- ! : Absolute address specification
- $: Relative address specification
- [ ] : Indirect address specification

In the case of immediate data, describe an appropriate numeric value or a label. When using a label, Be sure to describe the #, !, $, and [ ] symbols.

For operand register identifiers, r and rp, either function names (X, A, C, etc.) or absolute names (names in parentheses in the table below, R0, R1, R2, etc.) can be used for description.

Table 6-1. Operand Identifiers and Description Methods

Identifier	Description Method
r	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7)
rp	AX (RP0), BC (RP1), DE (RP2), HL (RP3)
sfr	Special-function register symbol
saddr	FE20H-FF1FH Immediate data or labels
saddrp	FE20H-FF1FH Immediate data or labels (even addresses only)
addr16	0000H-FFFFH Immediate data or labels
	(Only even addresses in a 16-bit data transfer instructions)
addr5	0040H-007FH Immediate data or labels (even addresses only)
word	16-bit immediate data or label
byte	8-bit immediate data or label
bit	3-bit immediate data or label

6.1.2 Description of “Operation” column

A	:	A register ; 8-bit accumulator
X	:	X register
B	:	B register
C	:	C register
D	:	D register
E	:	E register
H	:	H register
L	:	L register
AX	:	AX register pair; 16-bit accumulator
BC	:	BC register pair
DE	:	DE register pair
HL	:	HL register pair
PC	:	Program counter
SP	:	Stack pointer
PSW	:	Program status word
CY	:	Carry flag
AC	:	Auxiliary carry flag
Z	:	Zero flag
IE	:	Interrupt request enable flag
NMIS	:	Non-maskable interrupt servicing flag
( )	:	Memory contents indicated by the address or register contents in parentheses
X_H, X_L	:	High 8 bits and low 8 bits of a 16-bit register
∧	:	Logical product (AND)
∨	:	Logical sum (OR)
∀	:	Exclusive logical sum (exclusive OR)
———	:	Inverted data
addr16	:	16-bit immediate data or label
jdisp8	:	signed 8-bit data (displacement value)

6.1.3 Description of “Flag Operation” column

(Blank)	:	Unchanged
0	:	Clear to 0.
1	:	Set to 1.
×	:	Set/cleared according to the result
R	:	Previously saved value is restored.

★ 6.2 Operation List

Mnemonic	Operand	Bytes	Clock	Operation	Flags Z	Flags AC	Flags CY
MOV	r, #byte	3	6	r ← byte			
	saddr, #byte	3	6	(saddr) ← byte			
	sfr, #byte	3	6	sfr ← byte			
	A, r Note 1	2	4	A ← r			
	r, A Note 1	2	4	r ← A			
	A, saddr	2	4	A ← (saddr)			
	saddr, A	2	4	(saddr) ← A			
	A, sfr	2	4	A ← sfr			
	sfr, A	2	4	sfr ← A			
	A, !addr16	3	8	A ← (addr16)			
	!addr16, A	3	8	(addr16) ← A			
	PSW, #byte	3	6	PSW ← byte	×	×	×
	A, PSW	2	4	A ← PSW			
	PSW, A	2	4	PSW ← A	×	×	×
	A, [DE]	1	6	A ← (DE)			
	[DE], A	1	6	(DE) ← A			
	A, [HL]	1	6	A ← (HL)			
	[HL], A	1	6	(HL) ← A			
	A, [HL + byte]	2	6	A ← (HL + byte)			
	[HL + byte], A	2	6	(HL + byte) ← A			
XCH	A, X	1	4	A ↔ X			
	A, r Note 2	2	6	A ↔ r			
	A, saddr	2	6	A ↔ (saddr)			
	A, sfr	2	6	A ↔ (sfr)			
	A, [DE]	1	8	A ↔ (DE)			
	A, [HL]	1	8	A ↔ (HL)			
	A, [HL + byte]	2	8	A ↔ (HL + byte)			
MOVW	rp, #word	3	6	rp ← word			
	AX, saddrp	2	6	AX ← (saddrp)			
	saddrp, AX	2	8	(saddrp) ← AX			
	AX, rp Note 3	1	4	AX ← rp			
	rp, AX Note 3	1	4	rp ← AX			
XCHW	AX, rp Note 3	1	8	AX ↔ rp			

Notes 1. Except r = A

2. Except r = A or X

3. Only when rp = BC, DE, or HL

Remark One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags		
					Z	AC	CY
ADD	A, #byte	2	4	A, CY ← A + byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte	×	×	×
	A, r	2	4	A, CY ← A + r	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte)	×	×	×
ADDC	A, #byte	2	4	A, CY ← A + byte + CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte + CY	×	×	×
	A, r	2	4	A, CY ← A + r + CY	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr) + CY	×	×	×
	A, !addr16	3	8	A, CY ← A + (add16) + CY	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL) + CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte) + CY	×	×	×
SUB	A, #byte	2	4	A, CY ← A – byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte	×	×	×
	A, r	2	4	A, CY ← A – r	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte)	×	×	×
SUBC	A, #byte	2	4	A, CY ← A – byte – CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte – CY	×	×	×
	A, r	2	4	A, CY ← A – r – CY	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr) – CY	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16) – CY	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL) – CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte) – CY	×	×	×
AND	A, #byte	2	4	A ← A ∧ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∧ byte	×		
	A, r	2	4	A ← A ∧ r	×		
	A, saddr	2	4	A ← A ∧ (saddr)	×		
	A, !addr16	3	8	A ← A ∧ (addr16)	×		
	A, [HL]	1	6	A ← A ∧ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∧ (HL + byte)	×		

Remark One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags		
					Z	AC	CY
OR	A, #byte	2	4	A ← A ∨ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∨ byte	×		
	A, r	2	4	A ← A ∨ r	×		
	A, saddr	2	4	A ← A ∨ (saddr)	×		
	A, !addr16	3	8	A ← A ∨ (addr16)	×		
	A, [HL]	1	6	A ← A ∨ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∨ (HL + byte)	×		
XOR	A, #byte	2	4	A ← A ∀ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∀ byte	×		
	A, r	2	4	A ← A ∀ r	×		
	A, saddr	2	4	A ← A ∀ (saddr)	×		
	A, !addr16	3	8	A ← A ∀ (addr16)	×		
	A, [HL]	1	6	A ← A ∀ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∀ (HL + byte)	×		
CMP	A, #byte	2	4	A – byte	×	×	×
	saddr, #byte	3	6	(saddr) – byte	×	×	×
	A, r	2	4	A – r	×	×	×
	A, saddr	2	4	A – (saddr)	×	×	×
	A, !addr16	3	8	A – (addr16)	×	×	×
	A, [HL]	1	6	A – (HL)	×	×	×
	A, [HL + byte]	2	6	A – (HL + byte)	×	×	×
ADDW	AX, #word	3	6	AX, CY ← AX + word	×	×	×
SUBW	AX, #word	3	6	AX, CY ← AX – word	×	×	×
CMPW	AX, #word	3	6	AX – word	×	×	×
INC	r	2	4	r ← r + 1	×	×	
	saddr	2	4	(saddr) ← (saddr) + 1	×	×	
DEC	r	2	4	r ← r + 1	×	×	
	saddr	2	4	(saddr) ← (saddr) – 1	×	×	
INCW	rp	1	4	rp ← rp + 1			
DECW	rp	1	4	rp ← rp – 1			
ROR	A, 1	1	2	(CY, $A_7 \leftarrow A_0$, $A_{m-1} \leftarrow A_m$) × 1			×
ROL	A, 1	1	2	(CY, $A_0 \leftarrow A_7$, $A_{m+1} \leftarrow A_m$) × 1			×
RORC	A, 1	1	2	(CY ← A_0, $A_7 \leftarrow$ CY, $A_{m-1} \leftarrow A_m$) × 1			×
ROLC	A, 1	1	2	(CY ← A_7, $A_0 \leftarrow$ CY, $A_{m+1} \leftarrow A_m$) × 1			×

Remark One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags		
					Z	AC	CY
SET1	saddr. bit	3	6	(saddr. bit) ← 1			
	sfr. bit	3	6	sfr. bit ← 1			
	A. bit	2	4	A. bit ← 1			
	PSW. bit	3	6	PSW. bit ← 1	×	×	×
	[HL]. bit	2	10	(HL). bit ← 1			
CLR1	saddr. bit	3	6	(saddr. bit) ← 0			
	sfr. bit	3	6	sfr. bit ← 0			
	A. bit	2	4	A. bit ← 0			
	PSW. bit	3	6	PSW. bit ← 0	×	×	×
	[HL]. bit	2	10	(HL). bit ← 0			
SET1	CY	1	2	CY ← 1			1
CLR1	CY	1	2	CY ← 0			0
NOT1	CY	1	2	CY ← $\overline{CY}$			×
CALL	!addr16	3	6	(SP–1) ← (PC + 3)$_H$, (SP – 2) ← (PC + 3)$_L$, PC ← addr16, SP ← SP – 2			
CALLT	[addr5]	1	8	(SP–1) ← (PC + 1)$_H$, (SP – 2) ← (PC + 1)$_L$, PC$_H$ ← (00000000, addr5 + 1), PC$_L$ ← (00000000, addr5), SP ← SP – 2			
RET		1	6	PC$_H$ ← (SP + 1), PC$_L$ ← (SP), SP ← SP + 2			
RETI		1	8	PC$_H$ ← (SP + 1), PC$_L$ ← (SP), PSW ← (SP + 2), SP ← SP + 3, NMIS ← 0	R	R	R
PUSH	PSW	1	2	(SP – 1) ← PSW, SP ← SP – 1			
	rp	1	4	(SP – 1) ← rp$_H$, (SP – 2) ← rp$_L$, SP ← SP – 2			
POP	PSW	1	4	PSW ← (SP), SP ← SP + 1	R	R	R
	rp	1	6	rp$_H$ ← (SP + 1), rp$_L$ ← (SP), SP ← SP + 2			
MOVW	SP, AX	2	8	SP ← AX			
	AX, SP	2	6	AX ← SP			
BR	!addr16	3	6	PC ← addr16			
	$addr16	2	6	PC ← PC + 2 + jdisp8			
	AX	1	6	PC$_H$ ← A, PC$_L$ ← X			

Remark One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags Z AC CY
BC	$saddr16	2	6	PC ← PC + 2 + jdisp8 if CY = 1	
BNC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 0	
BZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 1	
BNZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 0	
BT	saddr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 1	
	sfr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 1	
	A. bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 1	
	PSW. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 1	
BF	saddr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 0	
	sfr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 0	
	A. bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 0	
	PSW. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 0	
DBNZ	B, $addr16	2	6	B ← B – 1, then PC ← PC + 2 + jdisp8 if B ≠ 0	
	C, $addr16	2	6	C ← C – 1, then PC ← PC + 2 + jdisp8 if C ≠ 0	
	saddr, $addr16	3	8	(saddr) ← (saddr) – 1, then PC ← PC + 3 + jdisp8 if (saddr) ≠ 0	
NOP		1	2	No Operation	
EI		3	6	IE ← 1 (Enable Interrupt)	
DI		3	6	IE ← 0 (Disable Interrupt)	
HALT		1	2	Set HALT Mode	
STOP		1	2	Set STOP Mode	

Remark One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

7. PROM PROGRAMMING

The program memory in μPD78P9014 is an 8K-byte one-time PROM that can be written electrically. The pins listed in Table 7-1 are used to write or verify this one-time PROM. For the connections for unused pins, see to "(2) PROM programming mode" in section 1, "Pin Connection Diagram (Top View)." The method updates the address by the clock input from the X1 pin and not the address input.

Table 7-1. Pins in the PROM Programming Mode

Pin Name	Function
V_{PP}	High voltage pin for setting the PROM programming mode and writing or verifying a program (usually, the V_{DD} potential)
MD0-MD3	Operating mode selection pin when writing or verifying a program
D0-D7	Data bus
X1	Address update clock input when writing or verifying a program
★ V_{DD}	Pin for setting the PROM programming mode and applying the power supply voltage. In the normal operating mode, 1.8 to 5.5 V are applied. In the PROM programming mode, +5.5 V are applied.

7.1 Operating Modes

If +5.5 V is applied to the V_{DD} pin and +12.5 V is applied to V_{PP} pin, the PROM programming mode is entered. This mode becomes an operating mode in Table 7-2 based on the settings of the MD0 to MD3 pins.

Table 7-2. Operating Modes in PROM Programming

Operating Mode \ Pins	V_{PP}	V_{DD}	MD0	MD1	MD2	MD3
★ Zero clear of the program memory address	+12.5	+5.5	H	L	H	L
Write mode			L	H	H	H
Verify mode			L	L	H	H
Program inhibit mode			H	×	H	H

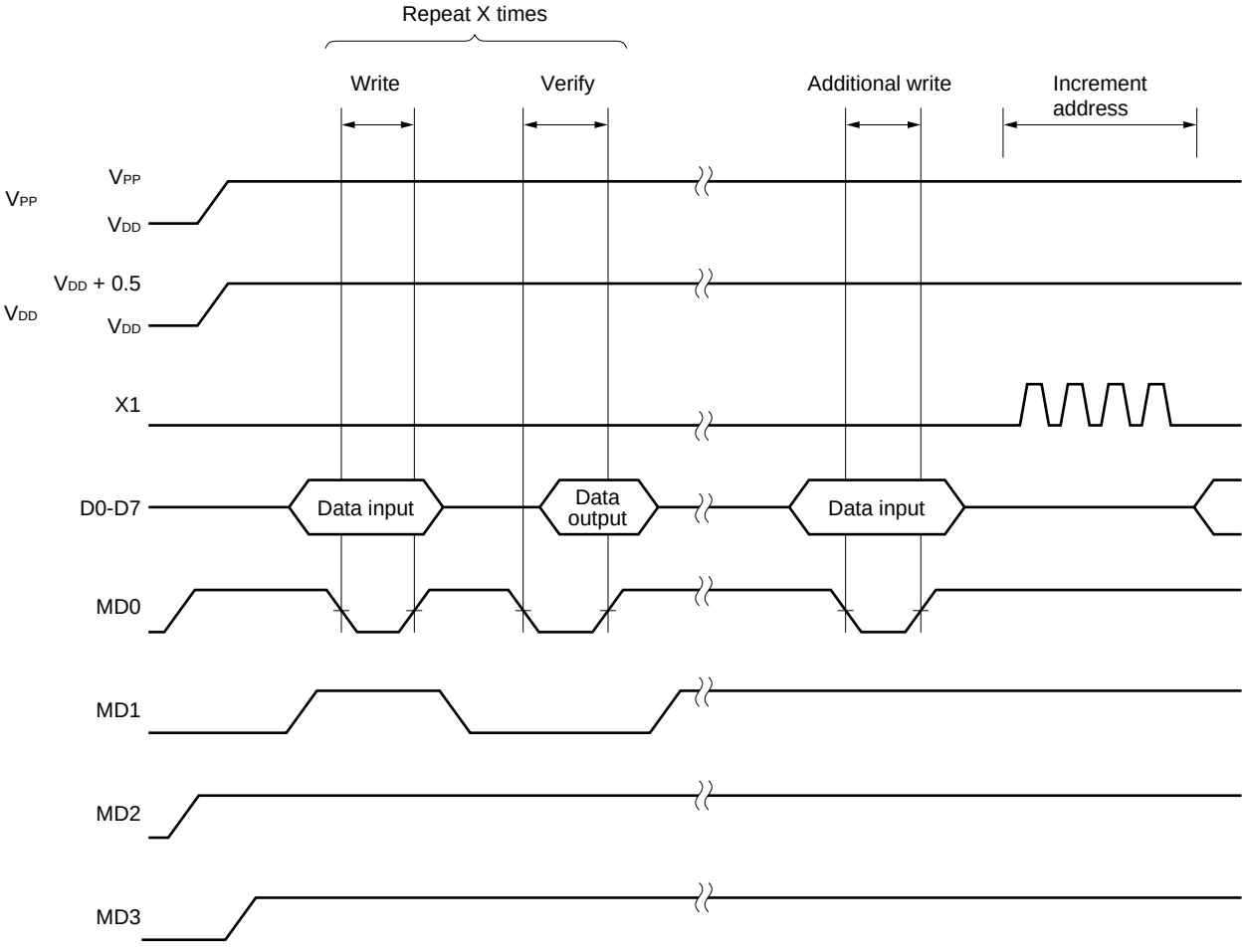
X : L or H

★ 7.2 PROM writing procedure

The following is the PROM writing procedure. High-speed writing is enabled.

(1) Pull down each unused pin through a resistor to V_{SS}. The X1 pin has the low level.
(2) Supply +5 V to the V_{DD} and V_{PP} pins.
(3) Wait 10 μs.
(4) 0 clear mode in the program memory address
(5) Supply 5.5 V to the V_{DD} pin and 12.5 V to the V_{PP} pin.
(6) Write data in the 1-ms write mode.
(7) Verify mode. If written, go to (8). If not written, repeat (6) and (7).
(8) Additional write for (Counts written in (6) and (7): X) × 1 ms
(9) Update (+1) the program memory address by the input of four pulses at the X1 pin.
(10) Repeat (6) to (9) until the last address.
(11) 0 clear mode of the program memory address
(12) Change the voltages at the V_{DD} and V_{PP} pins to 5 V.
(13) Power off

Steps (2) to (9) are illustrated in the following diagram.

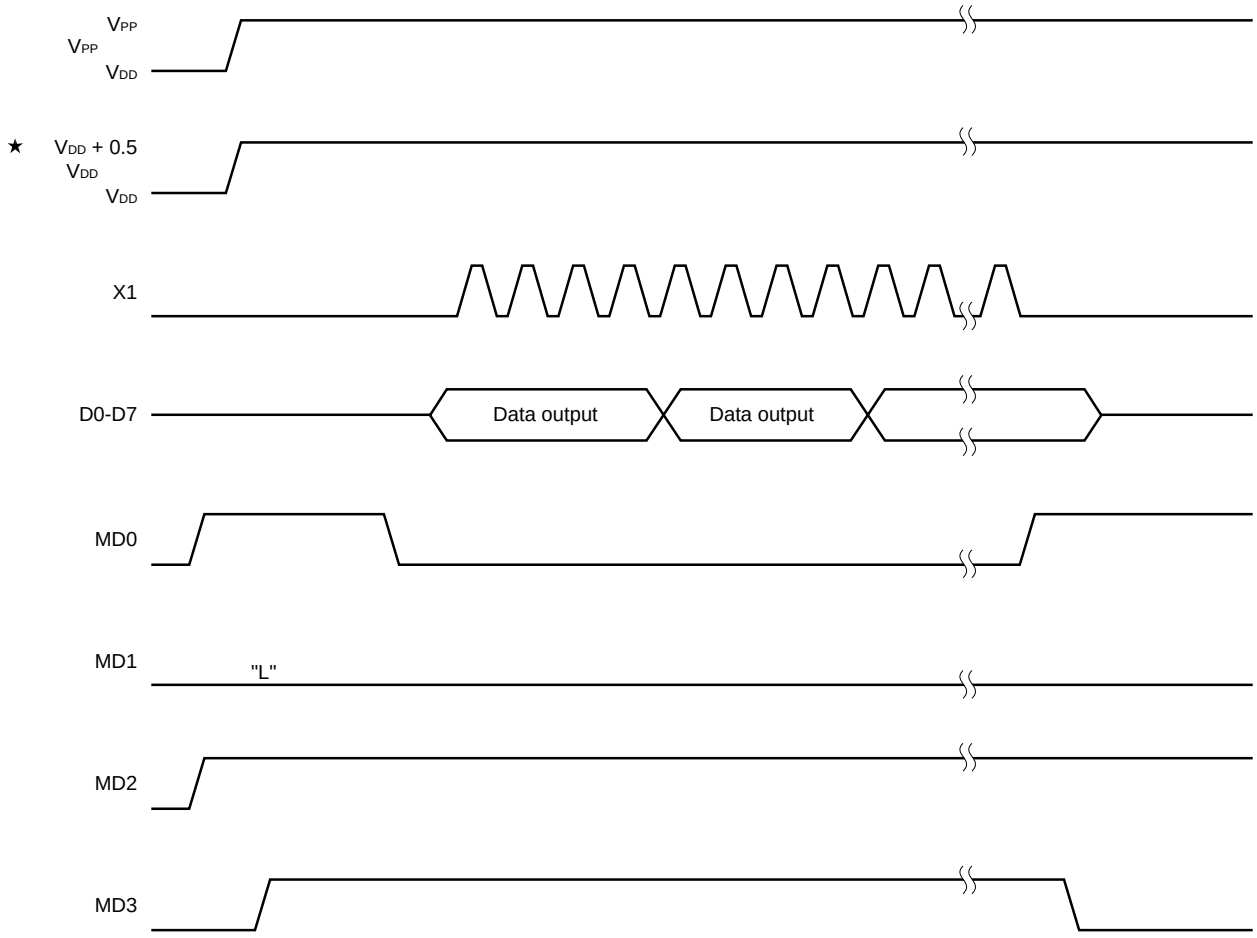


7.3 PROM reading procedure

The following is the PROM reading procedure.

(1) Pull down each unused pin through the resistor to V_{SS}. The X1 pin has the low level.
(2) Supply +5 V to the V_{DD} and V_{PP} pins.
(3) Wait 10 μs.
(4) 0 clear mode in the program memory address
★ (5) Supply +5.5V to V_{DD} and +12.5 V to V_{PP}.
(6) Verify mode. When clock pulses are input to the X1 pin, the data are sequentially output for each address for a period of four clock pulses.
(7) 0 clear mode in the program memory address
(8) Supply +5 V to the V_{DD} and V_{PP} pins.
(9) Power off

Steps (2) to (7) are shown in the figure below.



7.4 One-Time PROM Product Screening

The one-time PROM product cannot be tested completely by NEC before it is shipped, because of its structure. It is recommended to perform screening to verify PROM after writing necessary data and performing high-temperature storage under the following conditions.

Storage Temperature	Storage Time
125 °C	24 hours

★ NEC provides a fee-based, one-time microprocessor PROM writing, marking, screening, and verifying service called QTOP. For details, contact your NEC distributor.

★ 8. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Test Conditions		Rating	Unit
Supply voltages	V_{DD}			–0.3 to + 7.0	V
	V_{PP}			–0.3 to + 13.5	V
Input voltage	V_I			–0.3 to V_{DD} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH} **Note**	1 pin	Peak value	–10	mA
			r.m.s.	–5	mA
		Total of all pins	Peak value	–30	mA
			r.m.s.	–15	mA
Output current, low	I_{OL} **Note**	1 pin	Peak value	30	mA
			r.m.s.	15	mA
		Total of all pins	Peak value	160	mA
			r.m.s.	80	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note r.m.s. should be calculated as follows [r.m.s.] = [peak value] $\times \sqrt{\text{duty}}$

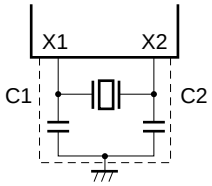
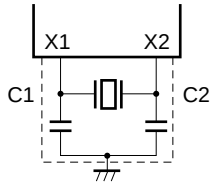
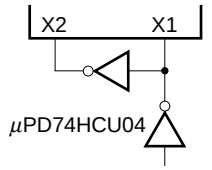
Caution Product quality may suffer if the absolute maximum rating is exceeded for even an single parameter or even momentarily. That is, the absolute maximum ratings are the rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

Remark The characteristics of an alternate function pin and a port pin are the same unless specified otherwise.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz, Unmeasured pins returned to 0 V			15	pF
Output capacitance	C_{OUT}				15	pF
I/O capacitance	C_{IO}				15	pF

Main System Clock Oscillation Circuit Characteristics(T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Condition	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillator frequency (fx)**Note 1**	V_{DD} = Oscillating voltage range	1.0		5.0	MHz
		Oscillation stabilization time**Note 2**	After V_{DD} reaches oscillator voltage range MIN.			4	ms
Crystal resonator		Oscillating frequency (fx)**Note 1**		1.0		5.0	MHz
		Oscillation stabilization time**Note 2**	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (fx)**Note 1**		1.0		5.0	MHz
		X1 input high/low level width (t_{XH}, t_{XL})		100		500	ns

Notes 1. Indicates only oscillation circuit characteristics. Refer to AC characteristics for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release.

Caution When using the main system clock oscillator, wiring the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

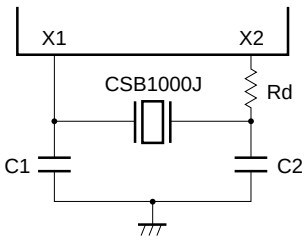
- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying higher current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS}.**
- **Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

★ **Recommended Oscillating Circuit Constants**

Ceramic Resonator (T_A = –40 to +85°C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Oscillation Circuit Constant (pF)		Oscillation Voltage Range (V_{DD})		Remarks
			C1	C2	MIN.	MAX.	
Murata Mfg. Co., Ltd.	CSB1000J[Note]	1.00	100	100	1.8	5.5	Rd = 1.0 kΩ
	CSA2.00MG040	2.00	100	100	2.0	5.5	
	CST2.00MG040		–	–			Product containing capacitor
	CSA4.19MG	4.19	30	30	1.8	5.5	
	CST4.19MGW		–	–			Product containing capacitor
	CSA5.00MG	5.00	30	30	2.2	5.5	
	CST5.00MGW		–	–			Product containing capacitor
	CSA5.00MGU		30	30	1.8	5.5	
	CST5.00MGWU		–	–			Product containing capacitor
TDK	CCR1000K2	1.0	100	100	1.8	5.5	
	CCR4.19MC3	4.19	–	–	1.8	5.5	Product containing capacitor
	FCR4.19MC5		–	–	2.0		Product containing capacitor
	CCR5.0MC3	5.0	–	–	2.2	5.5	Product containing capacitor
	FCR5.0MC5		–	–	2.0		Product containing capacitor
Kyocera Corp.	KBR-1000F/Y	1.0	100	100	1.8	5.5	T_A = –20 to +85 °C
	KBR-2.0MS	2.0	68	68	2.1	5.5	
	PBRC4.19A	4.19	33	33	1.8	5.5	
	PBRC4.19B		–	–			Product containing capacitor, T_A = –20 to +85°C
	KBR-4.19MSB		33	33			T_A = –20 to +85°C
	KBR-4.19MKC		–	–			Product containing capacitor, T_A = –20 to +85°C
	PBRC5.00A	5.0	33	33	1.8	5.5	T_A = –20 to +85°C
	PBRC5.00B		–	–			Product containing capacitor, T_A = –20 to +85°C
	KBR-5.0MSB		33	33			T_A = –20 to +85°C
	KBR-5.0MKC		–	–			Product containing capacitor, T_A = –20 to +85°C

Note If the ceramic resonator is the CSB1000J (1.0 MHz) by Murata Mfg. Co., Ltd., the limiting resistor (Rd = 1.0 kΩ) is needed (see the following figure). If another recommended oscillator is used, the limiting resistor is not needed.



Caution The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation but do not guarantee the accuracy of the oscillation frequency. If the application circuit requires accuracy of the oscillation frequency, it is necessary to set the oscillation frequency of the resonator in the application circuit. For this, it is necessary to directly contact manufacturer of the resonator being used.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Output current, low	I_{OL}	1 pin				15	mA
		Total of all of the pins				80	mA
Input voltage, high	V_{IH1}	P00 to P07, P10 to P17,	V_{DD} = 2.7 to 5.5 V	0.7 V_{DD}		V_{DD}	V
		P20 to P22, P30 to P32		0.9 V_{DD}		V_{DD}	V
	V_{IH2}	INTP0 to INTP2, SI0, RxD,	V_{DD} = 2.7 to 5.5 V	0.8 V_{DD}		V_{DD}	V
		ASCK, $\overline{SCK0}$, TI0, TI1, $\overline{RESET}$		0.9 V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2		V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P07, P10 to P17,	V_{DD} = 2.7 to 5.5 V	0		0.3 V_{DD}	V
		P20 to P22, P30 to P32		0		0.1 V_{DD}	V
	V_{IL2}	INTP0 to INTP2, SI0, RXD,	V_{DD} = 2.7 to 5.5 V	0		0.2 V_{DD}	V
		ASCK, $\overline{SCK0}$, TI0, TI1, $\overline{RESET}$		0		0.1 V_{DD}	V
	V_{IL3}	X1, X2		0		0.1	V
Output voltage, high	V_{OH}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA		V_{DD} – 1.0			V
		I_{OH} = –100 μA		V_{DD} – 0.5			V
Output voltage, low	V_{OL}	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA				1.0	V
		I_{OL} = 400 μA				0.5	V
Input leakage current, high	I_{LIH1}	V_{IN} = V_{DD}	Pins other than X1 and X2			3	μA
	I_{LIH2}		X1, X2			20	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	Pins other than X1 and X2			–3	μA
	I_{LIL2}		X1, X2			–20	μA
Output leakage current, high	I_{LOH}	V_{OUT} = V_{DD}				3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA

Remark The characteristics of an alternate function pin and a port pin are the same unless specified otherwise.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Software pull-up resistor	R	V_{IN} = 0 V		50	100	200	kΩ
Supply current[Note 1]	I_{DD1}	5.0 MHz	V_{DD} = 5.0 V ± 10 %[Note 2]		4.2	12.0	mA
		Crystal oscillation operation	V_{DD} = 3.0 V ± 10 %[Note 3]		0.95	2.8	mA
	I_{DD2}	5.0 MHz	V_{DD} = 5.0 V ± 10 %[Note 2]		0.7	2.0	mA
		Crystal oscillation HALT mode	V_{DD} = 3.0 V ± 10 %[Note 3]		0.3	0.9	mA
	I_{DD3}	STOP mode	V_{DD} = 5.0 V ± 10 %		0.1	20	μA
			V_{DD} = 3.0 V ± 10 %		0.05	8	μA
			V_{DD} = 2.0 V ± 10 %		0.05	10	μA

Notes 1. This does not include the port current (containing the current flowing through the on-chip pull-up resistor).

2. When operating at high-speed mode (when the processor clock control register (PCC) is set to 00H)

3. When operating at low-speed mode (when PCC is set to 02H)

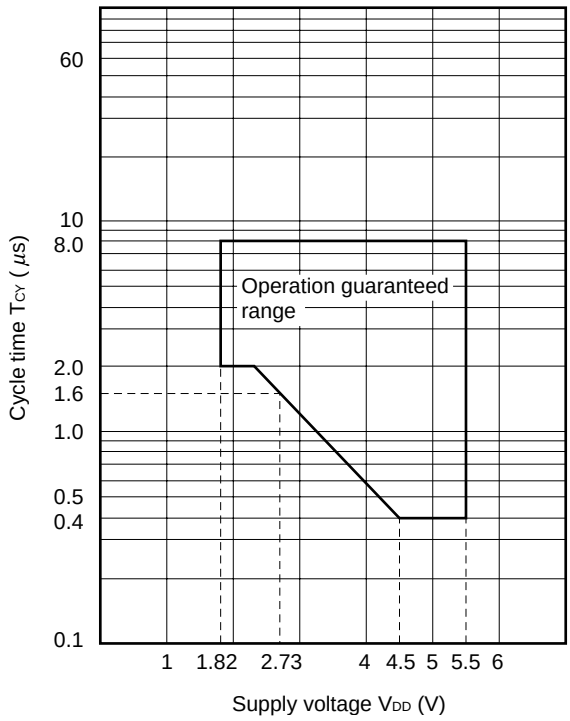
Remark The characteristics of an alternate function pin and a port pin are the same unless specified otherwise.

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T_{CY}	4.5 V ≤ V_{DD} ≤ 5.5 V		0.4		8	μs
		2.7 V ≤ V_{DD} ≤ 5.5 V		1.6		8	μs
				2.0		8	μs
TI0, TI1 inputs High/low level widths	t_{TIH}, t_{TIL}	V_{DD} = 2.7 to 5.5 V		0.1			μs
				1.8			μs
TI0, TI1 input frequency	f_{TI}	V_{DD} = 2.7 to 5.5 V		0		4	MHz
				0		275	kHz
Interrupt request input High/low level widths	t_{INTH}, t_{INTL}	INTP0 to INTP2	V_{DD} = 2.7 to 5.5 V	10			μs
				20			μs
$\overline{\text{RESET}}$ Low level width	t_{RSL}	V_{DD} = 2.7 to 5.5 V		10			μs
				20			μs

T_{CY} vs V_{DD} (Main System Clock)



(2) Serial interface channel 0 (T_A = –40 to +85°, V_{DD} = 1.8 to 5.5 V)

(i) 3-wire serial I/O mode ($\overline{SCK0}$ - on-chip clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		800			ns
				3200			ns
$\overline{SCK0}$ high/low level widths	t_{KH1}, t_{KL1}	V_{DD} = 2.7 to 5.5 V		t_{KCY1}/2-50			ns
				t_{KCY1}/2-150			ns
SI0 setup time (on $\overline{SCK0}$ ↑)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
				500			ns
SI0 hold time (on $\overline{SCK0}$ ↑)	t_{KSI1}	V_{DD} = 2.7 to 5.5 V		400			ns
				600			ns
$\overline{SCK0}$ ↓ → SO0 Output delay time	t_{KSO1}	R = 1k Ω, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		250	ns
				0		1000	ns

Note R and C are the load resistance and load capacitance of the SO0 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$ - external clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		800			ns
				3200			ns
$\overline{SCK0}$ high/low level widths	t_{KH2}, t_{KL2}	V_{DD} = 2.7 to 5.5 V		400			ns
				1600			ns
SI0 setup time (on $\overline{SCK0}$ ↑)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
				150			ns
SI0 hold time (on $\overline{SCK0}$ ↑)	t_{KSI2}	V_{DD} = 2.7 to 5.5 V		400			ns
				600			ns
$\overline{SCK0}$ ↓ → SO0 Output delay time	t_{KSO2}	R = 1k Ω, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		300	ns
				0		1000	ns

Note R and C are the load resistance and load capacitance of the SO0 output line.

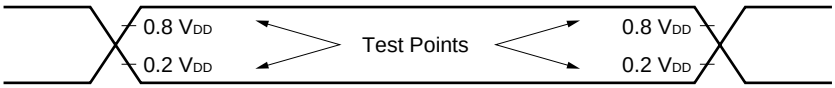
(iii) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V_{DD} = 2.7 to 5.5 V			78125	bps
					19531	bps

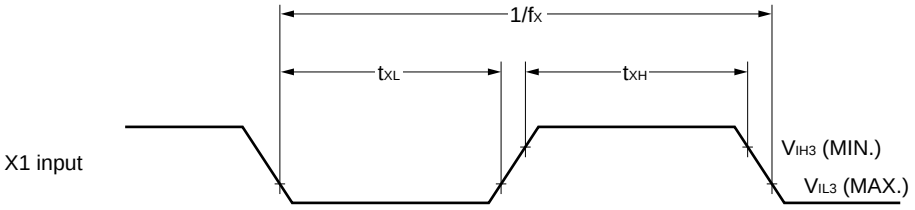
(iv) UART mode (external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY3}	V_{DD} = 2.7 to 5.5 V	800			ns
			3200			ns
ASCK high and low level widths	t_{KH3}, t_{KL3}	V_{DD} = 2.7 to 5.5 V	400			ns
			1600			ns
Transfer rate		V_{DD} = 2.7 to 5.5 V			39063	bps
					9766	bps
ASCK rise and fall times	t_R, t_F				1	μs

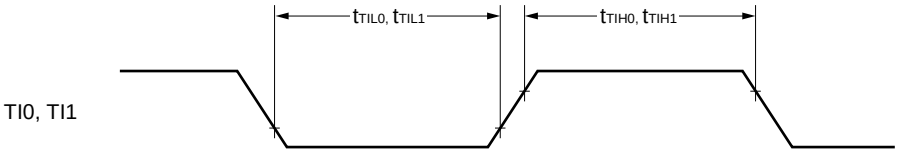
AC Timing Test Points (Except for X1 input)



Clock Timing

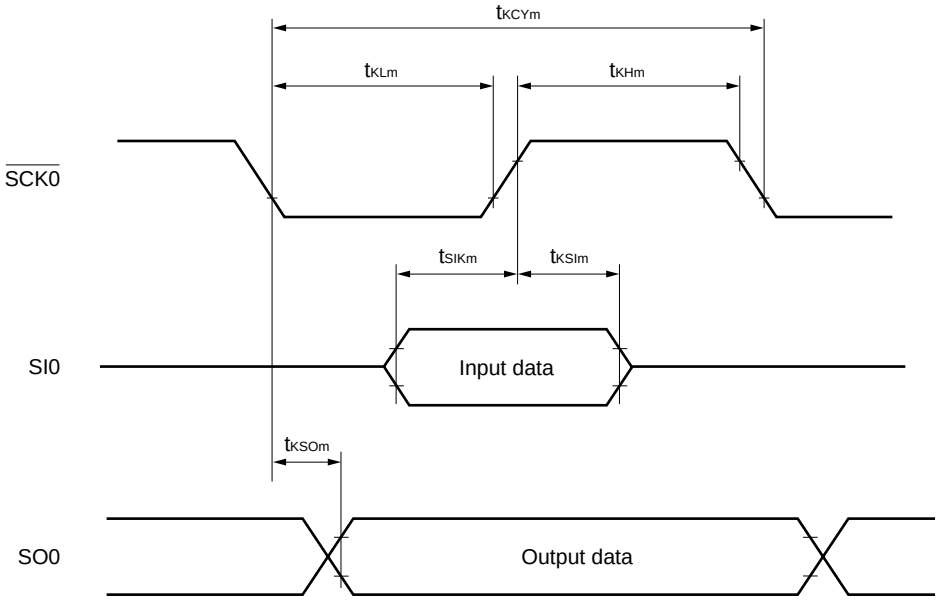


TI Timing

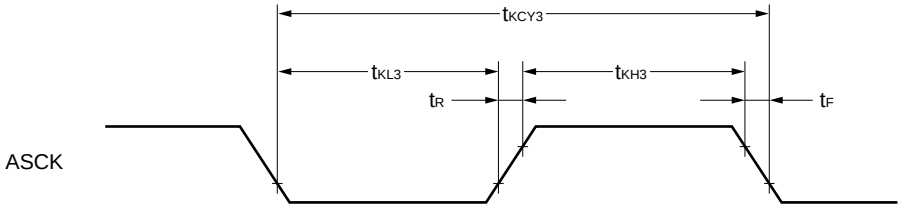


Serial Transfer Timing

3-Wire serial I/O mode:



UART mode (external clock input):



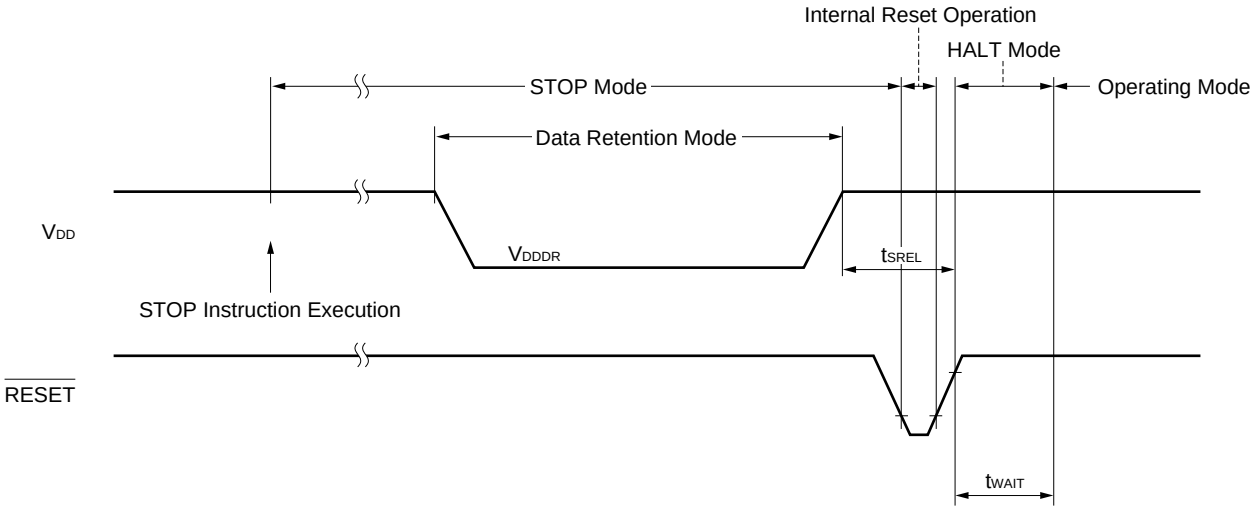
Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		5.5	v
Release signal set time	t_{SREL}		0		0	μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^{15}/f_X$		ms
		Release by interrupt request		**Note**		ms

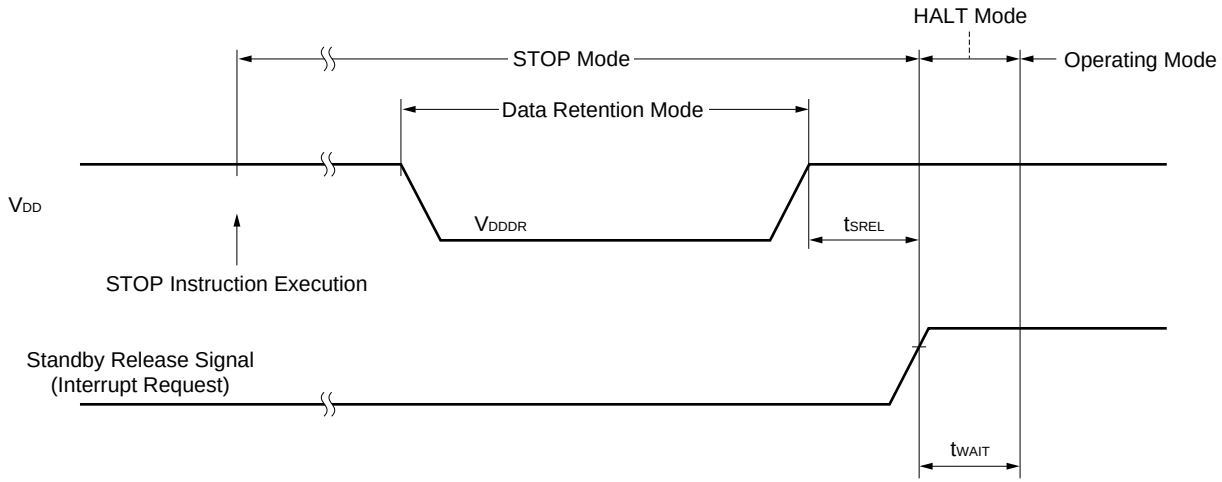
Note In combination with bits 0 to 2 (OSTS0 to OSTS2) of oscillation stabilization time select register (OSTS), selection of $2^{12}/f_X$, $2^{15}/f_X$, or $2^{17}/f_X$ is possible.

Remark f_X: Main system clock oscillation frequency

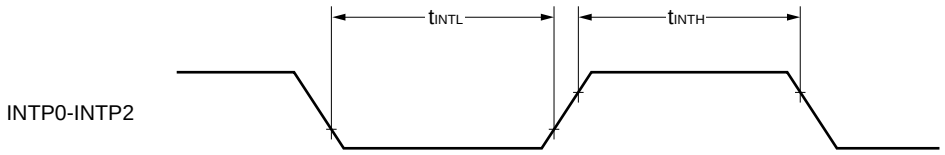
Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



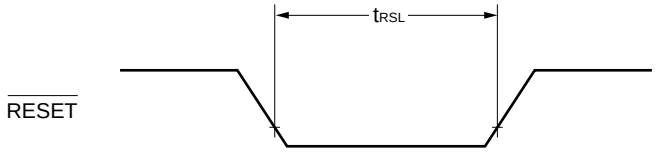
Data Retention Timing (Standby Release Signal: STOP Release by Interrupt Request Signal)



Interrupt Request Input Timing



$\overline{\text{RESET}}$ Input Timing



DC Programming Characteristics (T_A = 25°C, V_{DD} = 5.5 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	Neither X1 nor X2	0.7 V_{DD}		V_{DD}	V
	V_{IH2}	X1, X2	V_{DD}–0.5		V_{DD}	V
Input voltage, low	V_{IL1}	Neither X1 nor X2	0		0.3 V_{DD}	V
	V_{IL2}	X1, X2	0		0.4	V
Input leakage current	I_{L1}	V_{IN} = V_{IL} or V_{IH}			10	μA
Output voltage, high	V_{OH}	I_{OH} = –1 mA	V_{DD}–1.0			V
Output voltage, low	V_{OL}	I_{OL} = 1.6 mA			0.4	V
V_{DD} supply current	I_{DD}				30	mA
V_{PP} supply current	I_{PP}	MD0 = V_{IL}, MD1 = V_{IH}			30	mA

Cautions 1. Keep V_{PP} within +13.5 V, including overshoot.

2. Apply V_{DD} before V_{PP} and turn it off after V_{PP}.

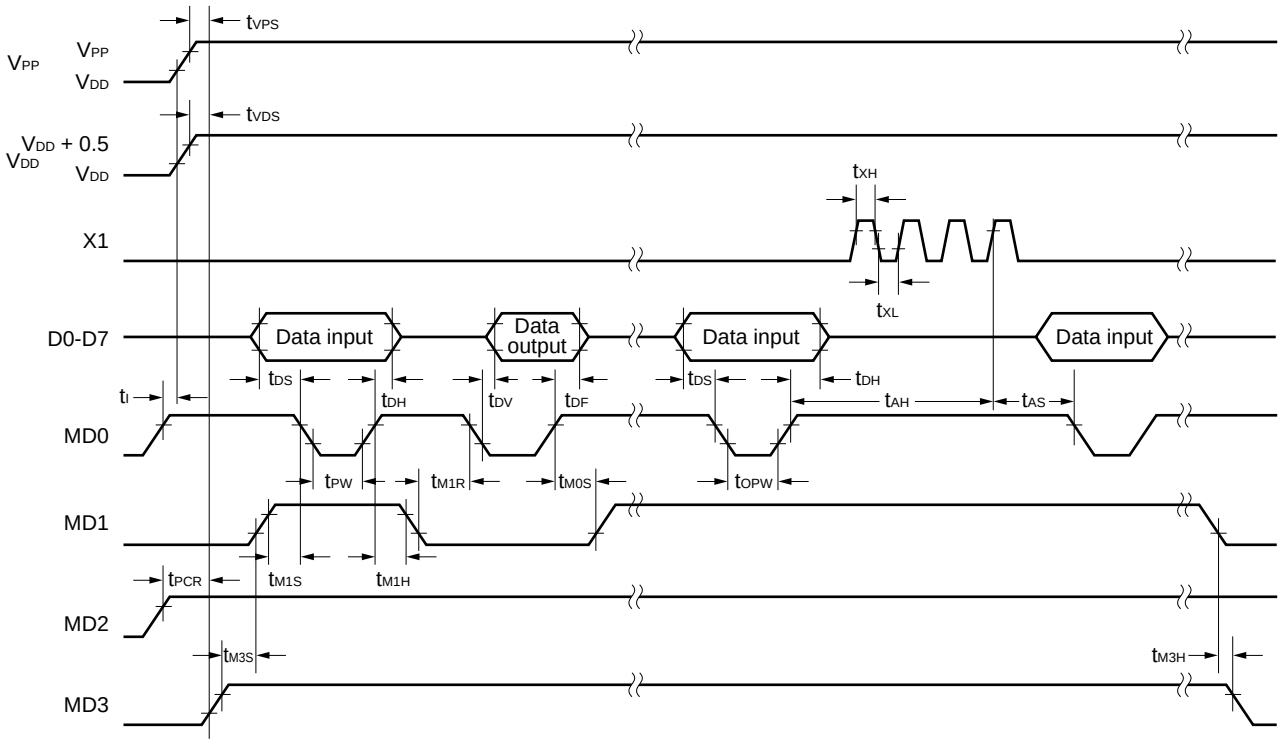
AC Programming Characteristics (T_A = 25°C, V_{DD} = 5.5 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	Note 1	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time[Note 2] (vs. MD0 ↓)	t_{AS}	t_{AS}		2			μs
MD1 setup time (vs. MD0 ↓)	t_{M1S}	t_{OES}		2			μs
Data setup time (vs. MD0 ↓)	t_{DS}	t_{DS}		2			μs
Address hold time[Note 2] (vs. MD0 ↓)	t_{AH}	t_{AH}		2			μs
Data hold time (vs. MD0 ↑)	t_{DH}	t_{DH}		2			μs
MD0 ↑ → data output float delay time	t_{DF}	t_{DF}		0		130	μs
V_{PP} setup time (vs. MD3 ↑)	t_{VPS}	t_{VPS}		2			μs
V_{DD} setup time (vs. MD3 ↑)	t_{VDS}	t_{VCS}		2			μs
Initial program pulse width	t_{PW}	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{OPW}	t_{OPW}		0.95		21.0	ms
MD0 setup time (vs. MD1 ↑)	t_{MOS}	t_{CES}		2			μs
MD0 ↑ → data output delay time	t_{DV}	t_{DV}	MD0 = MD1 = V_{IL}			1	μs
MD1 hold time (vs. MD0 ↑)	t_{M1H}	t_{OEH}	$t_{M1H} + t_{M1R} \geq 50$ μs	2			μs
MD1 recovery time (on MD0 ↓)	t_{M1R}	t_{OR}		2			μs
Program counter reset time	t_{PCR}	–		10			μs
X1 input high/low level widths	t_{XH}, t_{KL}	–		0.125			μs
X1 input frequency	f_X	–				4.19	MHz
Initial mode set time	t_I	–		2			μs
MD3 setup time (vs. MD1 ↑)	t_{M3S}	–		2			μs
MD3 hold time (vs. MD1 ↓)	t_{M3H}	–		2			μs
MD3 setup time (vs. MD0 ↓)	t_{M3SR}	–	During program memory read	2			μs
Address[Note 2] → data output delay time	t_{DAD}	t_{ACC}	During program memory read			2	μs
Address[Note 2] → data output hold time	t_{HAD}	t_{OH}	During program memory read	0		130	ns
MD3 hold time (vs. MD0 ↑)	t_{M3HR}	–	During program memory read	2			μs
MD3 ↓ → data output float delay time	t_{DFR}	–	During program memory read			2	μs

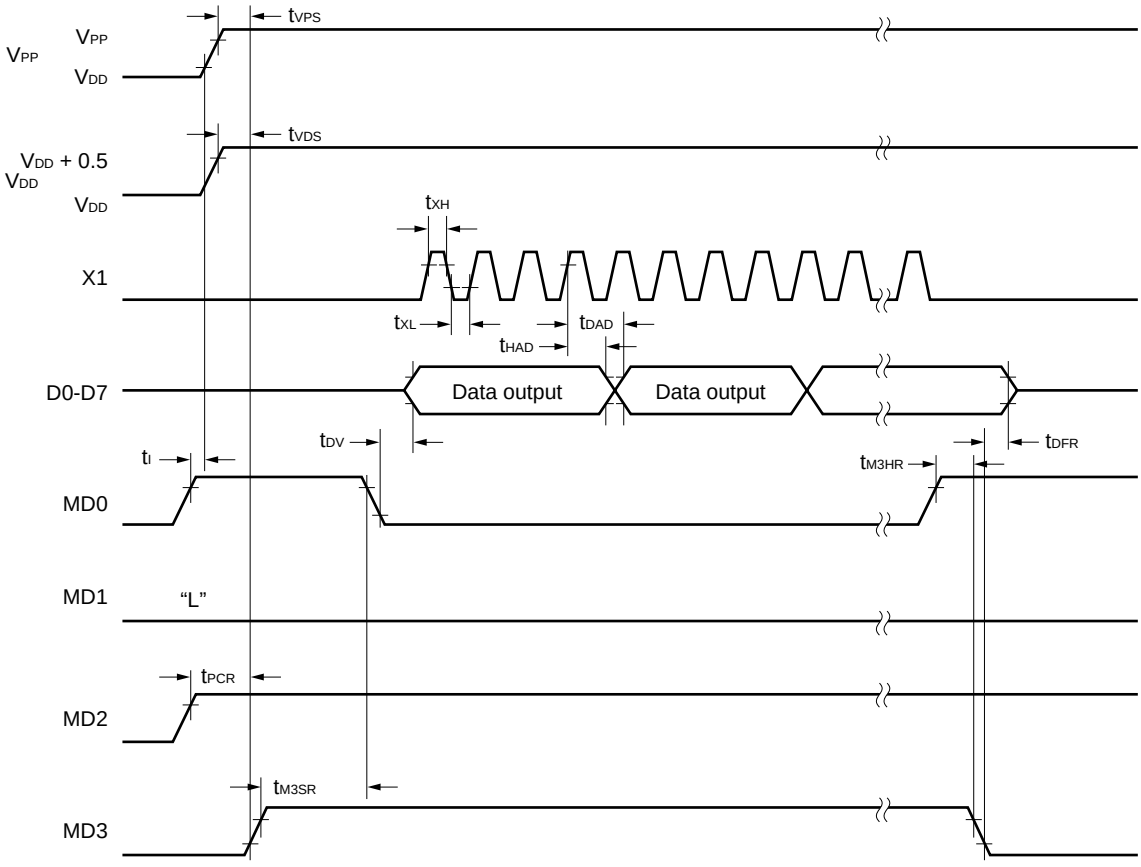
Notes 1. Symbol corresponding to those of μPD27C256A.

2. The internal address signal is incremented by one at the rising edge of the fourth X1 input and is not connected to a pin.

Program Memory Write Timing

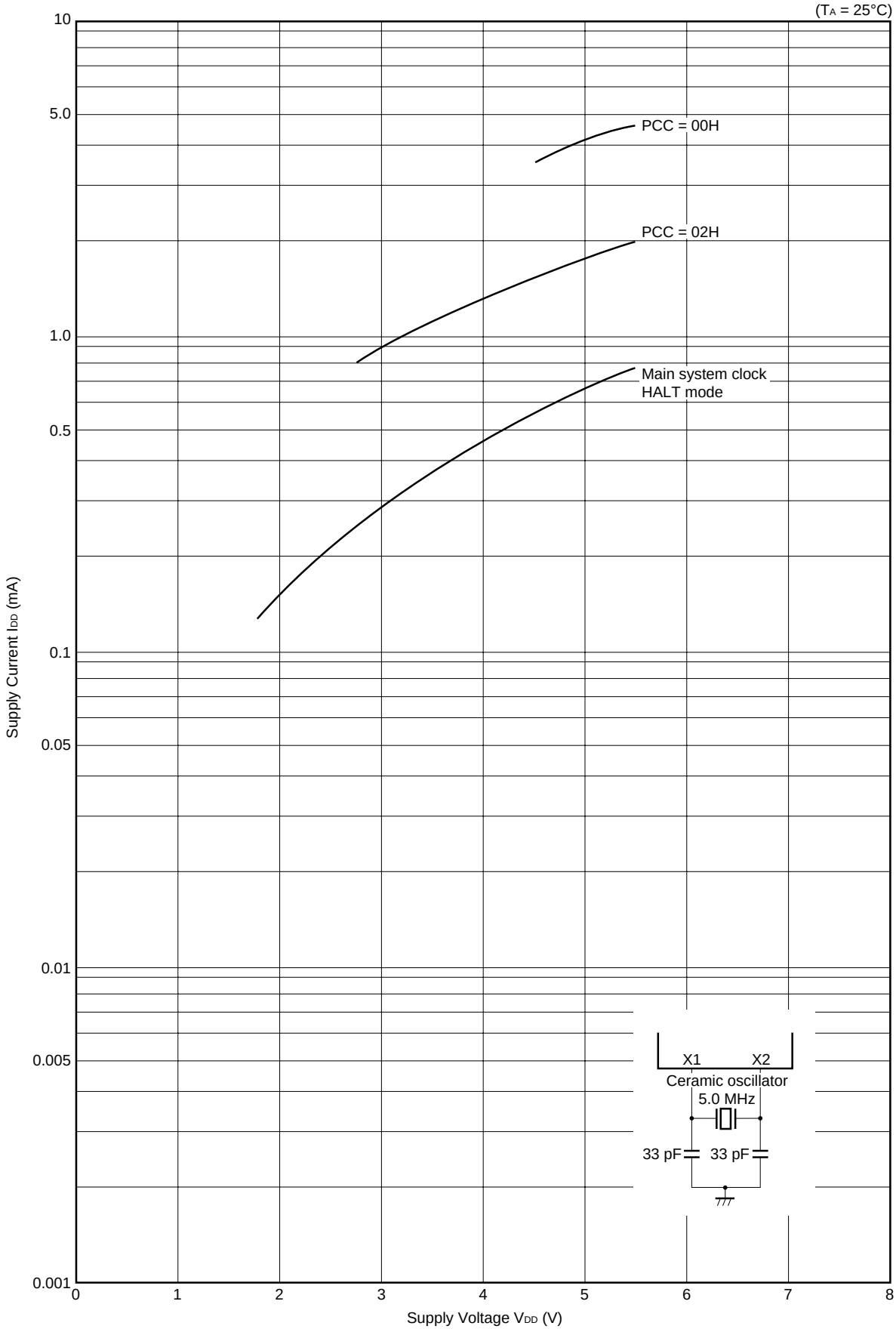


Program Memory Read Timing



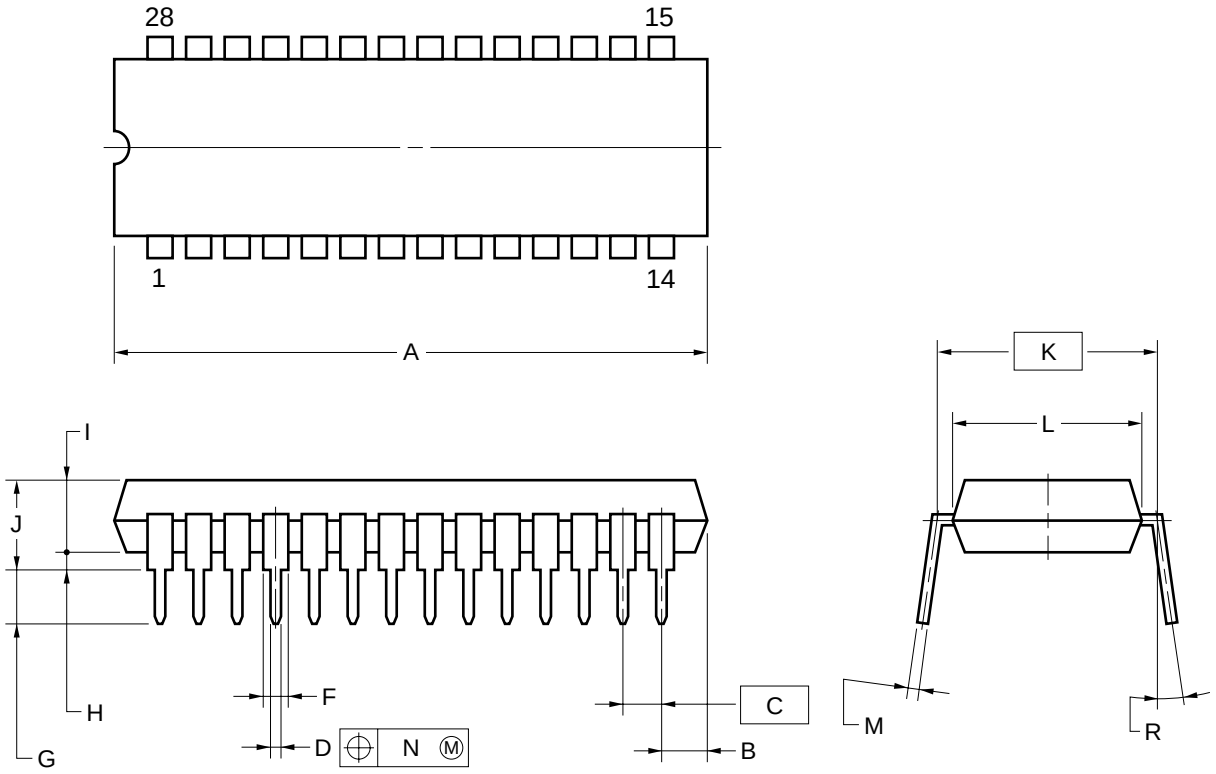
★ 9. CHARACTERISTIC CURVES (REFERENCE VALUES)

I_{DD} vs V_{DD} (Main system clock: 5.0 MHz ceramic oscillator)



10. PACKAGE DRAWINGS

28PIN PLASTIC SHRINK DIP (400 mil)



NOTES

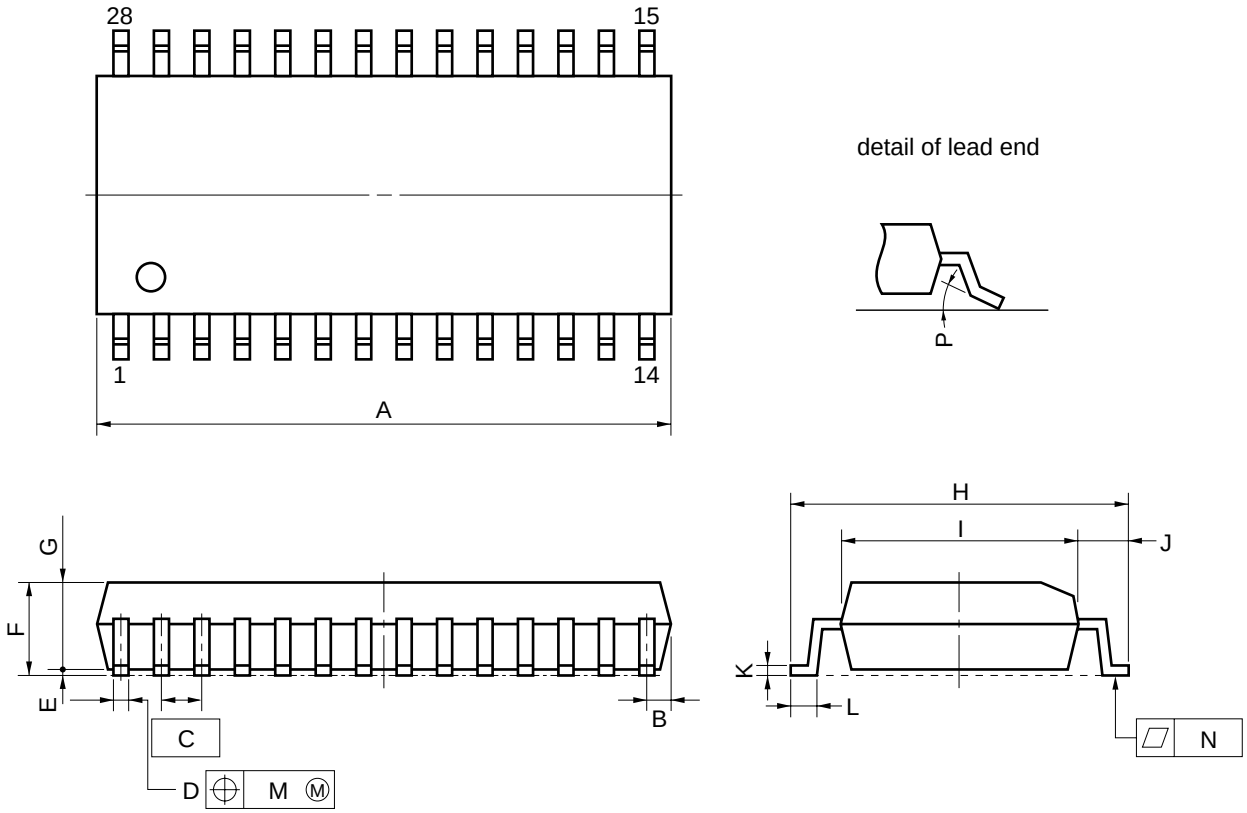
1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	28.46 MAX.	1.121 MAX.
B	2.67 MAX.	0.106 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2 ± 0.3	0.126 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6	0.339
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P28C-70-400A-1

28 PIN PLASTIC SOP (375 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.07 MAX.	0.712 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1±0.1	0.004±0.004
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	10.3±0.3	$0.406^{+0.012}_{-0.013}$
I	7.2	0.283
J	1.6	0.063
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005
N	0.15	0.006
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

P28GM-50-375B-3

★ 11. RECOMMENDED SOLDERING CONDITIONS

The μPD78P9014 should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual** (C10535E).

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 11-1. Soldering Conditions for Surface-mount Devices

μPD78P9014GT: 28-pin Plastic SOP (375 mils)

Soldering Method	Soldering Conditions	Recommended Condition Code
Infrared reflow	Package peak temperature: 235°C, Duration: 30 seconds max. (at 210°C or above) Number of times: two times max., Limit on the number of days: 7 days[Note] (Later, prebaking at 125°C for 20 hours is required.) Attention Articles other than a heat-resistant tray (magazine, taping, non-heat-resistant tray) cannot be baked in the packed state.	IR35-207-2
VPS	Package peak temperature: 215°C, Duration: 40 seconds max. (at 200°C or above) Number of times: two times max., Limit on the number of days: 7 days[Note] (Later, prebaking at 125°C for 20 hours is required.)	VP15-207-2
Wave soldering	Soldering bath temperature: 260°C max., Duration: 10 seconds max., Number of times: Once Preheating temperature: 120°C max.(Package surface temperature) Limit on the number of days: 7 days[Note] (Later, prebaking at 125°C for 20 hours is required.)	WS60-207-1
Partial heating	Pin temperature: 300°C max., Duration: 3 seconds max. (per device side)	–

Note The storage conditions are 25°C and 65% RH for the number of storage days after opening the seal of the dry pack.

Caution Using more than one soldering method should be avoided. (except in the case of partial heating)

Table 11-2. Soldering Conditions for Through-hole Devices

μPD78P9014CT: 28-pin Plastic Shrink DIP (400 mils)

Soldering Method	Soldering Conditions
Wave soldering (pin only)	Solder bath temperature: 260 °C max., Duration: 10 seconds max.
Partial heating	Pin temperature: 300 °C max., Duration: 3 seconds max.(per pin)

Caution Wave soldering is only for the lead part in order that jet solder cannot contact with the chip directly.

★ APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for the development of systems that employ the μPD78P9014.

Language Processing Software

RA78K0S[Notes 1, 2, 3]	78K/0S Series common assembler package
CC78K0S[Notes 1, 2, 3]	78K/0S Series common C compiler package
DF789014[Notes 1, 2, 3]	μPD789014 Subseries common device file
CC78K0S-L[Notes 1, 2, 3, 7]	78K/0S Series common C compiler library source file

PROM Writing Tools

PG-1500	PROM programmer
PA-78P9014GT	PROM programmer adapter connected to PG-1500
PG-1500 controller	PG-1500 control program

Debugging Tools

ND-K901[Notes 4, 7]	In-circuit emulator for the μPD789014 Subseries; included the screen debugger NS-78K9 in ND-K901
IF-98D[Note 4]	Interface board required when the PC-9800 Series (except for notebook PCs) is used as the host machine for NK-K901
IF-PCD[Note 4]	Interface board required when an IBM PC/AT or a compatible machine (except for notebook PCs) is used as the host machine for NK-K901
IF-CARD[Note 4]	Interface card required when a PC-9800 Series, an IBM PC/AT, or a compatible notebook is used as the host machine for NK-K901
NP-28CT[Note 4]	Emulation probe for the 28-pin plastic shrink DIP
NP-28GT[Note 4]	Emulation probe for the 28-pin plastic SOP
NJ-535[Note 4]	100V/120V-compatible voltage adapter
NJ-550W[Note 4]	100V to 240V-compatible voltage adapter
SM78K0S[Notes 5, 6]	78K/0S Series common system simulator
DF789014[Notes 5, 6]	Device file for the μPD789014 Subseries

Real-Time OS

MX78K0S[Notes 1, 2]	78K/0S Series OS

Notes 1. PC-9800 Series (MS-DOS™) based
2. IBM PC/AT™ and compatibles (PC DOS™/IBM DOS™/MS-DOS) based
3. HP9000 Series 700™ (HP-UX™) based, SPARCstation™ (SunOS™) based, NEWS™ (NEWS-OS™) based
4. This is a product of Naito Densei Machida Seisakusho Co., Ltd. (044-822-3813). To purchase, contact Naito Densei Machida Seisakusho Co., Ltd.
5. PC-9800 Series (MS-DOS + Windows™) based
6. IBM PC/AT and compatibles (PC DOS/IBM DOS/MS-DOS + Windows) based
7. Under development

Remark RA78K0S, CC78K0S, and SM78K0S are used with DF789014.

APPENDIX B. RELATED DOCUMENTS

Documents Related to Device

Document Name	Document No.	
	Japanese	English
μPD78P9014 Data Sheet	This document	To be prepared
μPD789011, 9012 Data Sheet	To be prepared	To be prepared
μPD789014 Subseries User's Manual	U11187J	U11187E
78K/0S Series User's Manual - Instruction	U11047J	U11047E

Development Tool Documents (User's Manual)

Document Name		Document No.	
		Japanese	English
RA78K0S Assembler Package	Operation	U11622J	U11622E
	Assembly language	U11599J	U11599E
	Structured assembly language	U11623J	U11623E
CC78K/0S C Compiler	Operation	U11816J	U11816E
	Language	U11817J	U11817E
SM78K0S System Simulator Windows based	Reference	U11489J	U11489E
SM78K Series System Simulator	External components user-open interface specification	U10092J	U10092E
PG-1500		U11940J	U11940E

Documents Related to Embedded Software (User's Manual)

Document Name	Document No.	
	Japanese	English
78K/0S Series OS MX78K0S	To be prepared	To be prepared

Caution The documents listed above are subject to change without notice. Be sure to use the latest documents for designing, etc.

Other Related Documents

Document Name	Document No.	
	Japanese	English
IC Package Manual	C10943X	
Semiconductor Device Surface Mount Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Device	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Electrostatic Discharge (ESD) Test	C11892J	C11892E
Guide to Quality Assurance for Semiconductor Device	C11893J	MEI-1202
Guide for Products Related to Microcomputer: Other Companies	U11416J	–

Caution The documents listed above are subject to change without notice. Be sure to use the latest documents for designing, etc.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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