UNITRODE

# Multimode SCSI 9 Line Terminator

## FEATURES

- Auto Selection Single Ended (SE) or Low Voltage Differential (LVD) Termination
- Meets SCSI-1, SCSI-2, SCSI-3, SPI, Ultra (Fast-20), Ultra2 (SPI-2 LVD) and Ultra3 Standards
- 2.7V to 5.25V Operation
- Differential Failsafe Bias
- Thermal packaging for low junction temperature and better MTBF
- Master/Slave Input
- Supports Active Negation
- 3pF Channel Capacitance
- Reversed Disconnect Polarity

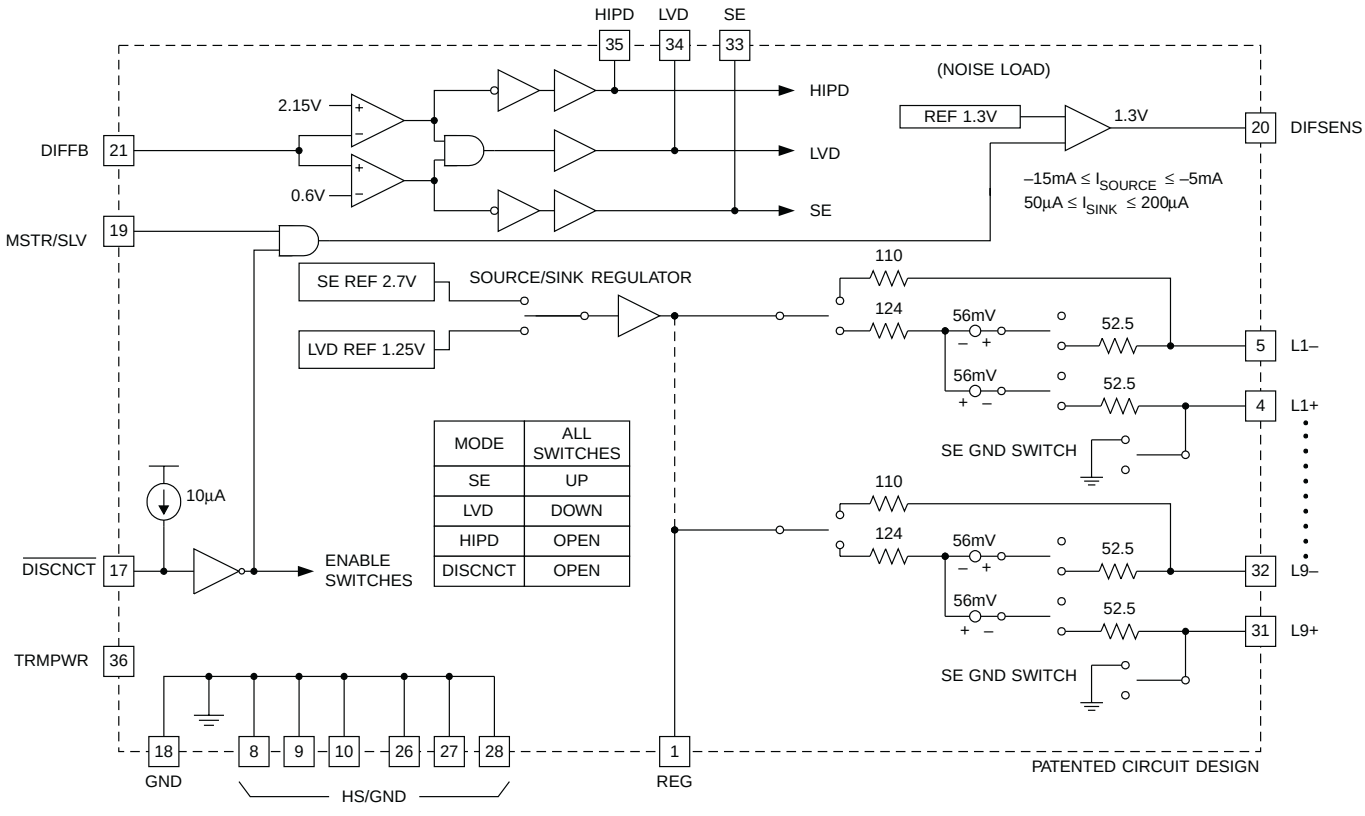
## DESCRIPTION

The UCC5631A Multimode SCSI Terminator provides a smooth transition into the next generation of the SCSI Parallel Interface (SPI-2). It automatically senses the bus, via DIFFB, and switches the termination to either single ended (SE) or low voltage differential (LVD) SCSI, dependent on which type of devices are connected to the bus. The UCC5631A can not be used on a HVD, EIA485, differential SCSI bus. If the UCC5631A detects a HVD SCSI device, it switches to a high impedance state.

The Multimode terminator contains all functions required to terminate and auto detect and switch modes for SPI-2 bus architectures. Single Ended and Differential impedances and currents are trimmed for maximum effectiveness. Fail Safe biasing is provided to insure signal integrity. Device/Bus type detection circuitry is integrated into the terminator to provide automatic switching of termination between single ended and LVD SCSI and a high impedance for HVD SCSI. The multimode function provides all the performance analog functions necessary to implement SPI-2 termination in a single monolithic device.

The UCC5631A is offered in a 36 pin SSOP package, as well as a 48 pin LQFP package for a temperature range of 0°C to 70°C.

## BLOCK DIAGRAM




*Note: Indicated pinout is for 36 pin SSOP package.*

## ABSOLUTE MAXIMUM RATINGS

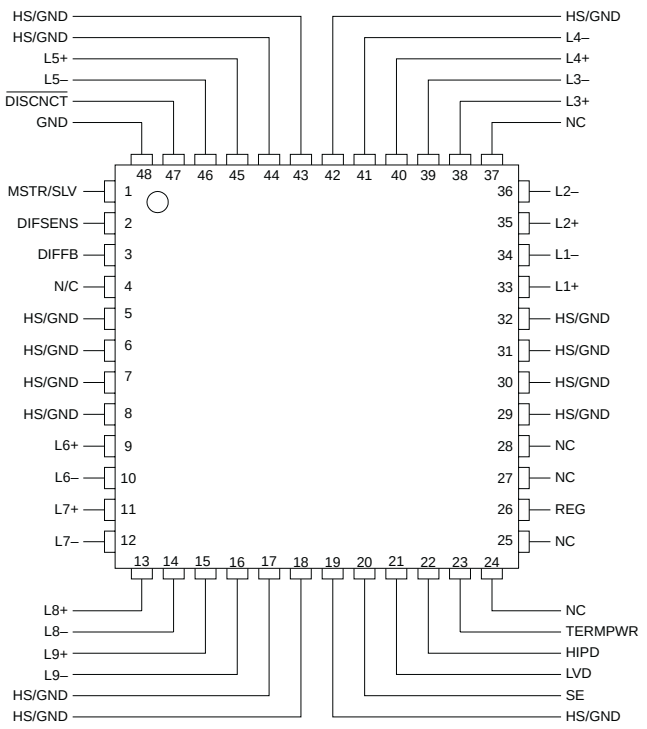
TRMPWR Voltage . . . . . 6V
Signal Line Voltage . . . . . 0V to TRMPWR
Package Power Dissipation . . . . . 2W
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10sec.) . . . . . +300°C

*All voltages are with respect to pin 18. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.*

## RECOMMENDED OPERATING CONDITIONS

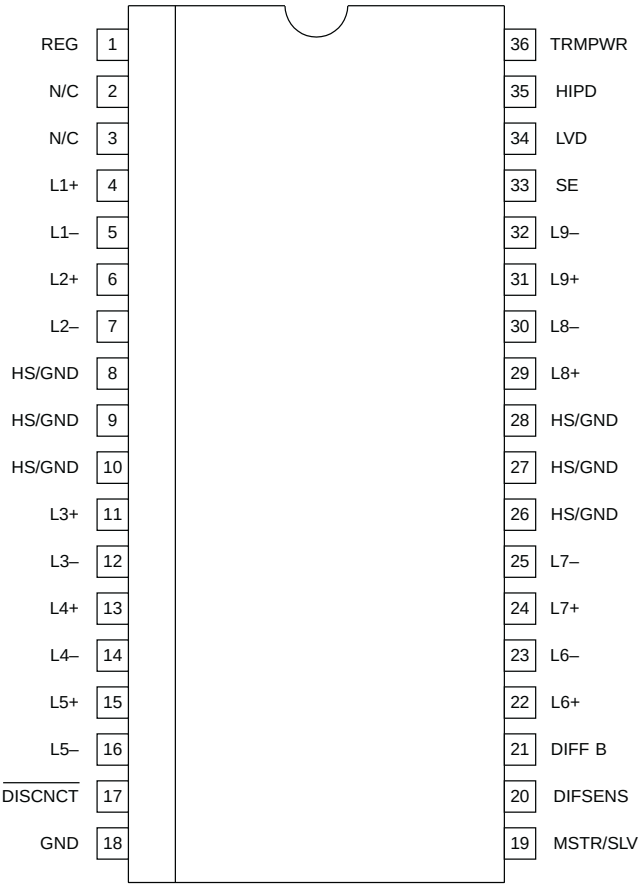
TRMPWR Voltage . . . . . 2.7V to 5.25V

**LQFP-48 (Top View)**
**FQP Package**




## CONNECTION DIAGRAM

**QSOP-36 (Top View)**
**MWP Package**



**ELECTRICAL CHARACTERISTICS** Unless otherwise stated, these specifications apply for $T_A = T_J = 0°C$ to 70°C, TRMPWR = 2.7V to 5.25V.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **TRMPWR Supply Current Section** | | | | | |
| TRMPWR Supply Current | LVD Mode (No Load) | | 13 | 20 | mA |
| | SE Mode (No Load) | | 1.6 | 10 | mA |
| | Disabled | | 250 | 400 | µA |
| **Regulator Section** | | | | | |
| REG Output Voltage (LVD Mode) | $0.5V \le V_{CM} \le 2.0V$ (Note1) | 1.15 | 1.25 | 1.35 | V |
| REG Output Voltage (SE Mode) | $0V \le V_{L-} \le 4.2V$ (Note2) | 2.5 | 2.7 | 3.0 | V |
| REG Short-Circuit Source Current (LVD and SE Modes) | $V_{REG}$= 0V | –800 | –420 | –225 | mA |
| REG Short-Circuit Sink Current (LVD and SE Modes) | $V_{REG}$= 3.0V | 100 | 180 | 800 | mA |
| **DIFSENS Output Section** | | | | | |
| Output Voltage | $-5mA \le I_{DIFSENS} \le 50\mu A$ | 1.2 | 1.3 | 1.4 | V |
| Short-Circuit Source Current | $V_{DIFSENS}$ = 0V | –15 | –8 | –5 | mA |
| Short-Circuit Sink Current | $V_{DIFSENS}$ = 2.75V | 50 | 80 | 200 | µA |
| **Differential Termination Section (**Applies to each line pair, 1-9, in LVD mode**)** | | | | | |
| Differential Impedance | | 100 | 105 | 110 | Ω |
| Common Mode Impedance | L+ and L– shorted together. (Note 3) | 110 | 140 | 165 | Ω |
| Differential Bias Voltage | | 100 | | 125 | mV |
| Common Mode Bias Voltage | L+ and L– shorted together. | 1.15 | 1.25 | 1.35 | V |
| Output Capacitance | Single ended measurement to ground. (Note 4) | | | 3 | pF |
| **Single Ended Termination Section (**Applies to each line pair, 1-9, in SE mode**)** | | | | | |
| Impedance | (Note 5) | 102.3 | 110 | 117.7 | Ω |
| Termination Current | Signal Level 0.2V | –25.4 | | –21 | mA |
| | Signal Level 0.5V | –22.4 | | –18 | mA |
| Output Capacitance | Single ended measurement to ground. (Note 4) | | | 3 | pF |
| Single Ended GND Switch Impedance | I= 10mA | | 20 | 60 | Ω |
| **Disconnected Termination Section (**Applies to each line pair, 1-9, in $\overline{\text{DISCNCT}}$ or HIPD mode**)** | | | | | |
| Output Leakage | | | | 400 | nA |
| Output Capacitance | Single ended measurement to ground. (Note 4) | | | 3 | pF |
| **$\overline{\text{DISCNCT}}$ and DIFFB Input Section** | | | | | |
| $\overline{\text{DISCNCT}}$ Threshold | | 0.8 | | 2.0 | V |
| $\overline{\text{DISCNCT}}$ Input Current | $V_{\overline{\text{DISCNCT}}}$ = 0V | –30 | –10 | – 3 | µA |
| DIFFB Single Ended to LVD Threshold | | 0.5 | | 0.7 | V |
| DIFFB LVD to HIPD Threshold | | 1.9 | | 2.4 | V |
| DIFFB Input Current | $0V \le V_{DIFFB} \le 2.75V$ | –1 | | 1 | µA |

**ELECTRICAL CHARACTERISTICS** Unless otherwise stated, these specifications apply for $T_A = T_J = 0°C$ to 70°C, TRMPWR = 2.7V to 5.25V.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **Master/Slave (MSTR/SLV) Input Section** | | | | | |
| MSTR/SLV Threshold | $V_{TRMPWR}$ = 2.7V | 0.8 | | 1.9 | V |
| | $V_{TRMPWR}$ = 3.3V | 1 | | 2.4 | V |
| | $V_{TRMPWR}$ = 5.25V | 1.5 | | 3.7 | V |
| MSTR/SLV Input Current | | –1 | | 1 | µA |
| **Status Bits (SE, LVD, HIPD) Output Section** | | | | | |
| $I_{SOURCE}$ | $V_{LOAD}$ = 2.4V | | –8.7 | –4 | mA |
| $I_{SINK}$ | $V_{LOAD}$ = 0.5V | 3 | 6 | | mA |
| | $V_{LOAD}$ = 0.4V | 2 | 5 | | mA |

***Note 1:*** *$V_{CM}$ is applied to all L+ and L– lines simultaneously.*

***Note 2:*** *$V_{L-}$ is applied to all L– lines simultaneously.*

***Note 3:*** $Z_{CM} = \frac{(2.0V - 0.5V)}{I_{(at\ V_{CM} = 2V)} - I_{(at\ V_{CM} = 0.5V)}}$;

***Note 4:*** *Guaranteed by design. Not 100% tested in production.*

*Note 5:* $Z = \frac{\left(V_{L(X)} - 0.2V\right)}{I_{L(X)}}$; *where*

*$VL_{(X)}$= Output voltage for each terminator minus output pin (L1– through L9–) with each pin unloaded.*
*$IL_{(X)}$= Output current for each terminator minus output pin (L1– through L9–) with the minus output pin forced to 0.2V.*

## PIN DESCRIPTIONS

**DIFFB:** Input pin for the comparators that select SE, LVD, or HIPD modes of operation. This pin should be decoupled with a 0.1µF capacitor to ground and then coupled to the DIFSENS pin through a 20kΩ resistor.

**DIFSENS:** Connects to the Diff Sense line of the SCSI bus. The bus mode is controlled by the voltage level on this pin.

**$\overline{\text{DISCNCT}}$:** Input pin used to shut down the terminator if the terminator is not connected at the end of the bus. Connect this pin to ground to disable the terminator or open pin to activate the terminator.

**HIPD:** TTL compatible status bit. This output pin is high when a high voltage differential device is detected on the bus.

**HS/GND:** Heat sink ground pins. These should be connected to large area PC board traces to increase the power dissipation capability.

**GND:** Power Supply return.

**L1– thru L9–:** Termination lines. These are the active lines in SE mode and are the negative lines for LVD mode. In HIPD mode, these lines are high impedance.

**L1+ thru L9+:** Termination lines. These lines switch to ground in SE mode and are the positive lines for LVD mode. In HIPD mode, these lines are high impedance.

**MSTR/SLV:** If the terminator is enabled, this input pin enables / disables the DIFSENS driver, when connected to TRMPWR or ground respectively. When the terminator is disabled, the DIFSENS driver is off, independent of this input.

**LVD:** TTL compatible status bit. This output pin is high when the SCSI bus is in LVD mode.

**REG:** Regulator output bypass pin. This pin must be connected to a 4.7µF capacitor to ground.

**SE:** TTL compatible status bit. This output pin is high when the SCSI bus is in SE mode.

**TRMPWR:** 2.7V to 5.25V power input pin.

## APPLICATION INFORMATION

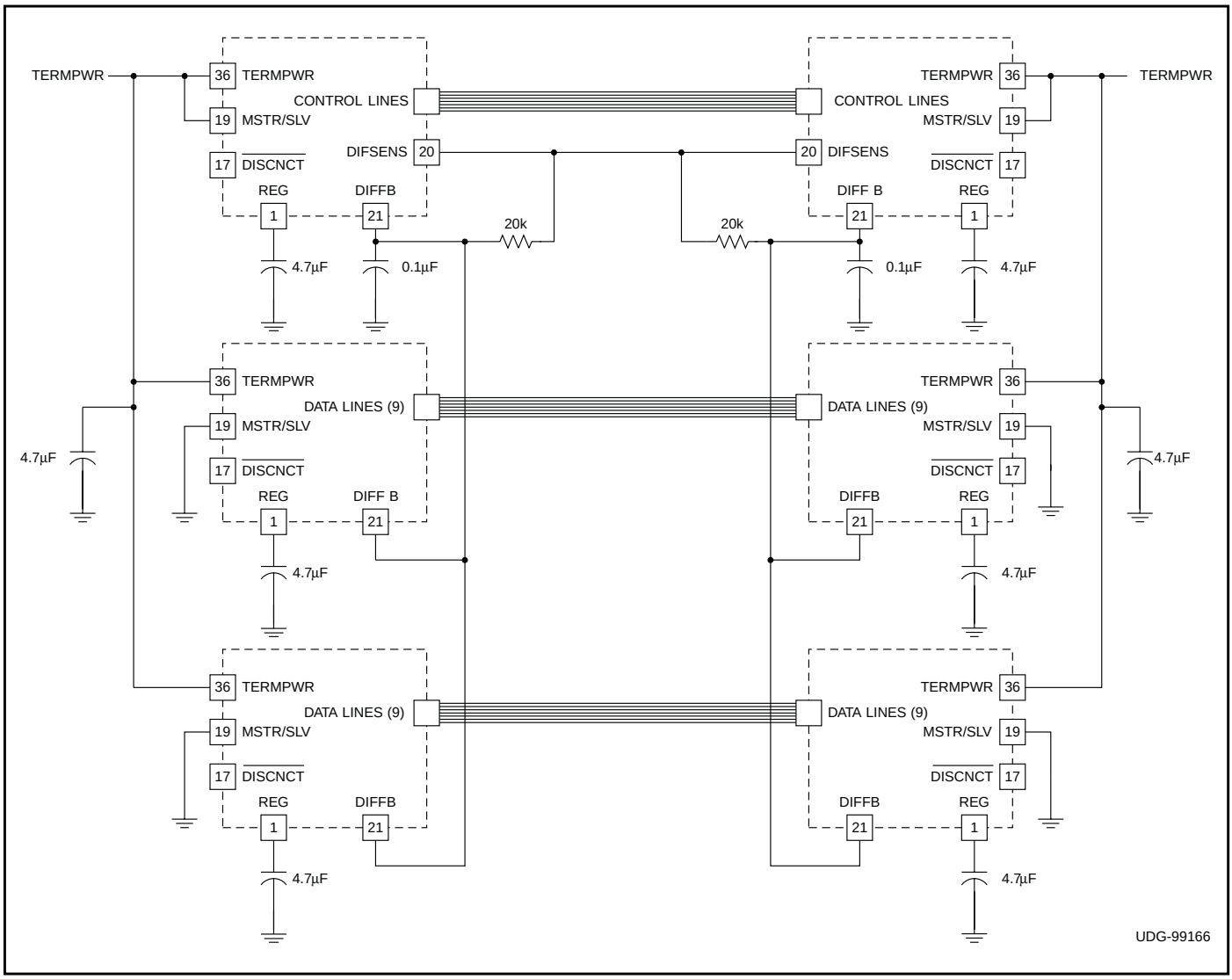



***Figure 2. Application diagram.***

All SCSI buses require a termination network at each end to function properly. Specific termination requirements differ, depending on which types of SCSI devices are present on the bus.

The UCC5631A is used in multi-mode active termination applications, where single ended (SE) and low voltage differential (LVD) devices might coexist. The UCC5631A has both SE and LVD termination networks integrated into a single monolithic component. The correct termination network is automatically determined by the SCSI bus "DIFSENS" signal.

The SCSI bus DIFSENS signal line is used to identify which types of SCSI devices are present on the bus. On power-up, the UCC5631A DIFSENS drivers will try to deliver 1.3V to the DIFSENS line. If only LVD devices are present, the DIFSENS line will be successfully driven to 1.3V and the terminators will configure for LVD operation. If any single ended devices are present, they will present a short to ground on the DIFSENS line, signaling the UCC5631A(s) to configure into the SE mode, accommodating the SE devices. Or, if any high voltage differential (HVD) devices are present, the DIFSENS line is pulled high and the terminator will enter a high impedance state, effectively disconnecting from the bus.

## APPLICATION INFORMATION (cont.)

The DIFSENS line is monitored by each terminator through a 50Hz noise filter at the DIFFB input pin. A set of comparators detect and select the appropriate termination for the bus as follows. If the DIFSENS signal is below 0.5V, the termination network is SE. Between 0.7V and 1.9V, the termination network switches to LVD, and above 2.4V is HVD, causing the terminators to disconnect from the bus. The thresholds accommodate differences in ground potential that can occur with long lines.

Three UCC5631A multi-mode parts are required at each end of the bus to terminate 27 (18 data, plus 9 control) lines. Each part includes a DIFSENS driver, but only one is necessary to drive the line. A MSTR/SLV input pin is provided to disable the other two. The "master" part must have its' MSTR/SLV pin connected to TRMPWR and the two "slave" parts must have the MSTR/SLV inputs grounded. Only the "master" is connected directly to the SCSI bus DIFSENS line. The DIFFB inputs on all three parts are connected together, allowing them to share the same 50Hz noise filter. This multi-mode terminator operates in full specification down to 2.7V TRMPWR voltage. This accommodates 3.3V systems, with allowance for the 3.3V supply tolerance (+/- 10%), a unidirectional fusing device and cable drop. In 3.3V TRMPWR systems, the UCC3912 is recommended in place of the fuse and diode. The UCC3912's lower voltage drop allows additional margin over the fuse and diode, for the far end terminator.

Layout is critical for Ultra2 and Ultra3 systems. The SPI-2 standard for capacitance loading is 10pF maximum from each positive and negative signal line to ground, and a maximum of 5pF between the positive and negative signal lines of each pair is allowed. These maximum capacitances apply to differential bus termination circuitry that is not part of a SCSI device, (e.g. a cable terminator). If the termination circuitry is included as part of a SCSI device, (e.g., a host adaptor, disk or tape drive), then the corresponding requirements are 30pF maximum from each positive and negative signal line to ground and 15pF maximum between the positive and negative signal lines of each pair.

The SPI-2 standard for capacitance balance of each pair and balance between pairs is more stringent. The standard is 0.75pF maximum difference from the positive and negative signal lines of each pair to ground. An additional requirement is a maximum difference of 2pF when comparing pair to pair. These requirements apply to differential bus termination circuitry that is not part of a SCSI device. If the termination circuitry is included as part of a device, then the corresponding balance requirements are 2.25pF maximum difference within a pair, and 3pF from pair to pair.

Feed-throughs, through-hole connections, and etch lengths need to be carefully balanced. Standard multi-layer power and ground plane spacing add about 1pF to each plane. Each feed-through will add about 2.5pF to 3.5pF. Enlarging the clearance holes on both power and ground planes will reduce the capacitance. Similarly, opening up the power and ground planes under the connector will reduce the capacitance for through-hole connector applications. Capacitance will also be affected by components, in close proximity, above and below the circuit board.

Unitrode multi-mode terminators are designed with very tight balance, typically 0.1pF between pins in a pair and 0.3pF between pairs. At each L+ pin, a ground driver drives the pin to ground, while in single ended mode. The ground driver is specially designed to not effect the capacitive balance of the bus when the device is in LVD or disconnect mode.

Multi-layer boards need to adhere to the 120Ω impedance standard, including the connectors and feed-throughs. This is normally done on the outer layers with 4 mil etch and 4 mil spacing between runs within a pair, and a minimum of 8 mil spacing to the adjacent pairs to reduce crosstalk. Microstrip technology is normally too low of impedance and should not be used. It is designed for 50Ω rather than 120Ω differential systems. Careful consideration must be given to the issue of heat management. A multi-mode terminator, operating in SE mode, will dissipate as much as 130mW of instantaneous power per active line with TRMPWR = 5.25V. The UCC5631A is offered in a 36 pin SSOP and a 48 lead LFQP. Both packages include heat sink ground pins. These heat sink/ground pins are directly connected to the die mount paddle under the die and conduct heat from the die to reduce the junction temperature. All of the HS/GND pins need to be connected to etch area or a feed-through per pin connecting to the ground plane layer on a multi-layer board.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

## IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.