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MULTIMODE SCSI 14-LINE TERMINATOR

FEATURES

- **Auto Selection Single Ended (SE) or Low Voltage Differential (LVD) Termination**
- **Meets SCSI–1, SCSI–2, SCSI–3, SPI, Ultra (Fast–20), Ultra2 (SPI–2 LVD), Ultra3, Ultra160 (SPI–3) and Ultra320 (SPI–4) Standards**
- **2.7V to 5.25V Operation**
- **Differential Failsafe Bias**
- **Thermal packaging for low junction temperature and better MTBF**

DESCRIPTION

The UCC5628 Multimode SCSI terminator provides a smooth transition into the low-voltage differential SCSI parallel interface (SPI–2, SPI–3 and SPI–4). It automatically senses the bus, via DIFFB, and switches the termination to either single ended (SE) or low-voltage differential (LVD) SCSI, dependent on which type of devices are connected to the bus. The UCC5628 can not be used on a high voltage differential (HVD), EIA485, differential SCSI bus. If the UCC5628 detects a HVD SCSI device, it switches to a high-impedance state.

BLOCK DIAGRAM

UDG–98099

![ESD warning symbol] These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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DESCRIPTION (CONTINUED)

The Multimode terminator contains all functions required to terminate and auto detect and switch modes for SPI–2, SPI–3 and SPI–4 bus architectures. Single ended, differential impedances and currents are trimmed for maximum effectiveness. Fail-safe biasing is provided to insure signal integrity. Device/bus type detection circuitry is integrated into the terminator to provide automatic switching of termination between single ended and LVD SCSI and a high impedance for HVD SCSI. The multimode function provides all the performance analog functions necessary to implement SPI–2 termination in a single monolithic device.

The UCC5628 is offered in a 48-pin LQFP package for a temperature range of 0°C to 70°C.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted†‡

	UCC5628	UNIT
TRMPWR voltage	6	V
Signal line voltage	0 to 6	
Package Dissipation	2	W
Storage temperature, T_{stg}	–65 to 150	°C
Operating junction temperature, T_J	–55 to 150	
Lead temperature (soldering, 10 sec.)	300	

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. Currents are positive into and negative out of, the specified terminal.

‡ Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.
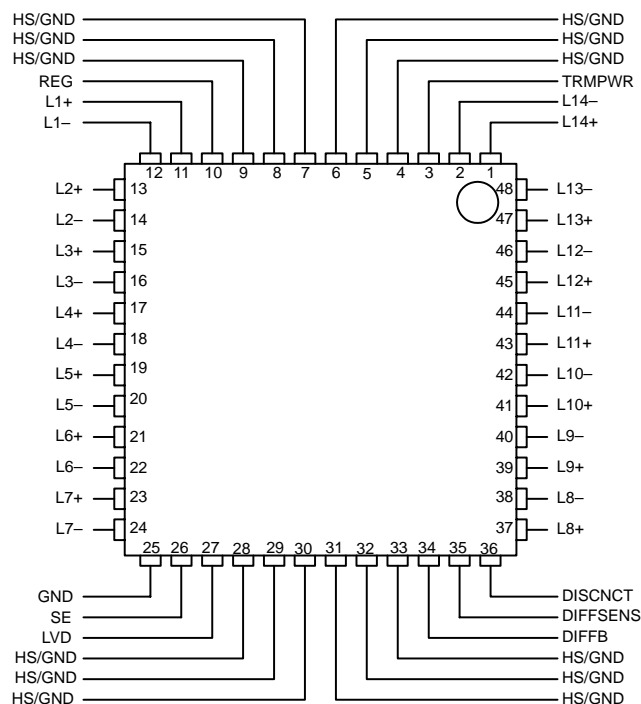
RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
TRMPWR voltage	2.7		5.25	V
Temperature ranges	0		70	°C

ORDERING INFORMATION

T_A	DISCONNECT STATUS	PACKAGED DEVICE†
		LQFP–48 (FQP)
0°C to 70°C		UCC5628FQP

† The LQFP packages are available taped and reeled. Add TR suffix to device type (e.g. UCC5628FQPTR) to order quantities of 2,500 devices per reel.

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CONNECTION DIAGRAM

ELECTRICAL CHARACTERISTICS

$T_A = T_J = 0°C$ to $70°C$, TRMPWR = 3.3 V, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TRMPWR Supply Current Section					
TRMPWR supply current	LVD mode		20	25	mA
	SE mode		1.6	10.0	
	Disabled terminator		250	400	μA
Regulator Section					
1.25-V regulator	LVD mode	1.15	1.25	1.35	V
1.25-V regulator source current	$V_{REG} = 0$ V	−375	−700	−1000	mA
1.25-V regulator sink current	$V_{REG} = 3.3$ V	170	300	700	
1.3-V regulator	Diff sense	1.2	1.3	1.4	V
1.3-V regulator source current	$V_{REG} = 0$ V	−15		−5	mA
1.3-V regulator sink current	$V_{REG} = 3.3$ V	50		200	μA
2.7-V regulator	SE mode	2.5	2.7	3.0	V
2.7-V regulator source current	$V_{REG} = 0$ V	−375	−700	−1000	mA
2.7-V regulator sink current	$V_{REG} = 3.3$ V	170	300	700	
Differential Termination Section					
Differential impedance		100	105	110	Ω
Common mode impedance	(2)	110	150	165	
Differential bias voltage		100		125	mV
Common mode bias		1.15	1.25	1.35	V
Output capacitance	Single Ended Measurement to Ground (Note 1)			3	pF

UCC5628

ELECTRICAL CHARACTERISTICS

$T_A = T_J = 0°C$ to $70°C$, TRMPWR = 3.3 V, (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Single Ended Termination Section						
Impedance	$Z = \dfrac{VL_X - 0.2\ V}{IL_X}$ (3)		102.3	110.0	117.7	W
Termination current	Signal level 0.2 V,	all lines low	−21.0	−24.0	−25.4	mA
	Signal level 0.5 V		−18.0		−22.4	
Output leakage					400	nA
Output capacitance	Single ended measurement to ground (1)				3	pF
Single ended GND impedance	I = 10 mA			20	60	W
Disconnect and Diff Buffer Input Section						
DISCNCT threshold			0.8		2.0	V
DISCNCT input current				10	30	mA
Diff buffer single ended to LVD threshold			0.5		0.7	V
Diff buffer LVD to HPD threshold			1.9		2.4	
DIFFB input current			−10		10	mA
Status Bits (SE, LVD) Output Section						
I_{SOURCE}	V_{LOAD} = 2.4 V		−4	−6		mA
I_{SINK}	V_{LOAD} = 0.4 V		2	5		

NOTES: 1. Ensured by design. Not production tested.

2. $Z_{CM} = \dfrac{1.2\ V}{I_{(VCM+0.6\ V)} - I_{(VCM-0.6\ V)}}$, where VCM=voltage measured with L+ tied to L– and zero current applied.

3. VL_X= Output voltage for each terminator minus output pin (L1– through L14–) with each pin unloaded.
IL_X = Output current for each terminator minus output pin (L1– through L14–) with the minus output pin forced to 0.2 V.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
DIFFB	34	I	DIFFSENS filter pin should be connected to a 4.7-µF capacitor and a 50-kΩ resistor.
DIFFSENS	35	O	The SCSI bus Diff sense line to detect what types of devices are connected to the SCSI bus.
DISCNCT	36	I	Disconnect pin shuts down the terminator when it is not at the end of the bus. The disconnect pin high enables the terminator.
GND	25		Analog ground.
HS/GND			Heatsink ground pins must be connected to a large ground area.
LINEn–			Signal line active line for single ended or negative line in differential applications for the SCSI bus.
LINEn+			Ground line for single ended or positive line for differential applications for the SCSI bus.
LVD	27	O	TTL compatible status bit indicating that the device has detected the bus in LVD mode. This output is not valid in disconnect mode.
REG	10	O	Regulator bypass pin, must be connected to a 4.7-µF capacitor.
SE	26	O	TTL compatible status bit indicating that the device has detected the bus in single ended mode. This output is not valid in disconnect mode.
TRMPWR	3		VIN 2.7-V to 5.25-V supply, bypass near the terminators with a 4.7-µF capacitor to ground.

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APPLICATION INFORMATION

The UCC5628 is a multimode active terminator with selectable single ended (SE) and low voltage differential (LVD) SCSI termination integrated into a monolithic component. Mode selection is accomplished with the *diff sense* signal.

The diff sense signal is a three level signal, which is driven at each end of the bus by one active terminator. A LVD or multimode terminator drives the diff sense line to 1.3 V. If diff sense is at 1.3 V, then bus is in LVD mode. If a single ended SCSI device is plugged into the bus, the diff sense line is shorted to ground. With diff sense shorted to ground, the terminator changes to single ended mode to accommodate the SE device. If a HVD device is plugged in to the bus, the diff sense line is pulled high and the terminator shuts down.

The diff sense line is driven and monitored by the terminator through a 50-Hz noise filter for SPI–2 and a 100-ms to 300-ms filter for SPI–3 and SPI–4 at the DIFFB input pin. A set of comparators, that allow for ground shifts, determine the bus status as follows. Any diff sense signal below 0.5 V is single ended, between 0.7 V and 1.9 V is LVD and above 2.4 V is HVD.

In the single ended mode, a multimode terminator has a 110-Ω terminating resistor connected to a 2.7-V termination voltage regulator. The 2.7-V regulator is used on all unitrode terminators designed for 3.3-V systems. This requires the terminator to operate in specification down to 2.7-V TRMPWR voltage to allow for the 3.3-V supply tolerance, an unidirectional fusing device and cable drop. At each L+ pin, a ground driver drives the pin to ground, while in single ended mode. The ground driver is specially designed so it will not effect the capacitive balance of the bus when the device is in LVD or disconnect mode. The device requirements call for 1.5-pF balance on the lines of a differential pair. The terminator capacitance has to be a small part of the capacitance imbalance.

Layout is very critical for Ultra2, Ultra3, Ultra160 and Ultra320 systems. Multilayer boards need to adhere to the 120-Ω impedance standard, including connector and feed-through. This is normally done on the outer layers with 4-mil etch and 4-mil spacing between the runs within a pair, and a minimum of 8-mil spacing to the next pair. This spacing between the pairs reduces potential crosstalk. Beware of feed-throughs and each through-hole connection adds a lot of capacitance. Standard power and ground plane spacing yields about 1 pF to each plane. Each feed-through will add about 2.5 pF to 3.5 pF. Enlarging the clearance holes on both power and ground planes can reduce the capacitance and opening up the power and ground planes under the connector can reduce the capacitance for through-hole connector applications. Microstrip technology is normally too low of impedance and should not be used. It is designed for 50 Ω rather than 120-Ω differential systems.

Capacitance balance is critical for Ultra2, Ultra3, Ultra160 and Ultra320. The balance capacitance standard is 0.5 pF per line with the balance between pairs of 2 pF. The components are designed with very tight balance, typically 0.1 pF between pins in a pair and 0.3 pF between pairs. Layout balance is critical, feed-throughs and etch length must be balanced, preferably no feed-throughs would be used. Capacitance for devices should be measured in the typical application, material and components above and below the circuit board effect the capacitance.

Multimode terminators need to consider power dissipation; the UCC5628 is offered in a power package with heat sink ground pins. These heat-sink ground pins are directly connected to the die mount paddle under the die and conduct heat from the die to reduce the junction temperature. These pins need to be connected to etch area or a feed-through per pin connecting to the ground plane layer on a multilayer board.

In 3.3-V TRMPWR systems, the UCC3912 should be used to replace the fuse and diode. This reduces the voltage drop, allowing for cable drop to the far end terminator. 3.3-V battery systems normally have a 10% tolerance. The UCC3912 is 150-mV drop under LVD loads, allowing 150-mV drop in the cable system. All Unitrode LVD and multimode terminators are designed for 3.3-V systems, operating down to 2.7 V.

UCC5628

APPLICATION INFORMATION
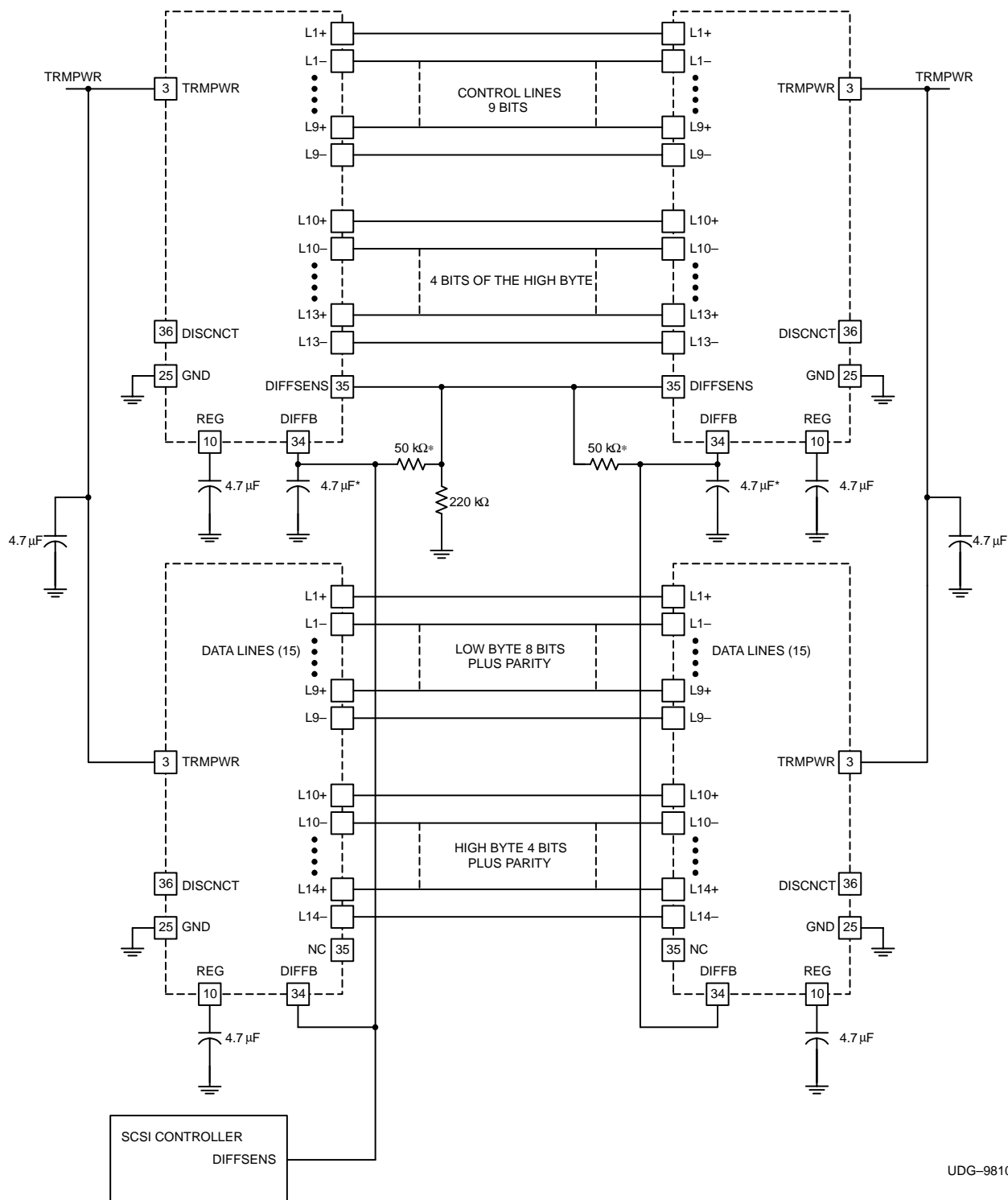
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NOTE: A 220-kΩ resistor is added to ground to insure the transceivers will come up in single-ended mode when no terminator is enabled. The controller DIFFSENS ties to the DIFFB pin on the terminators, only one RC network should be on a device.

NOTE: * For SPI–2 systems a 20-kΩ resistor and 0.1-µF capacitor is used. For SPI–3 and SPI–4 systems a 50-kΩ resistor and 4.7-µF capacitor is used.

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MECHANICAL DATA

PT (S-PQFP-G48)   **PLASTIC QUAD FLATPACK**

4040052/C 11/96
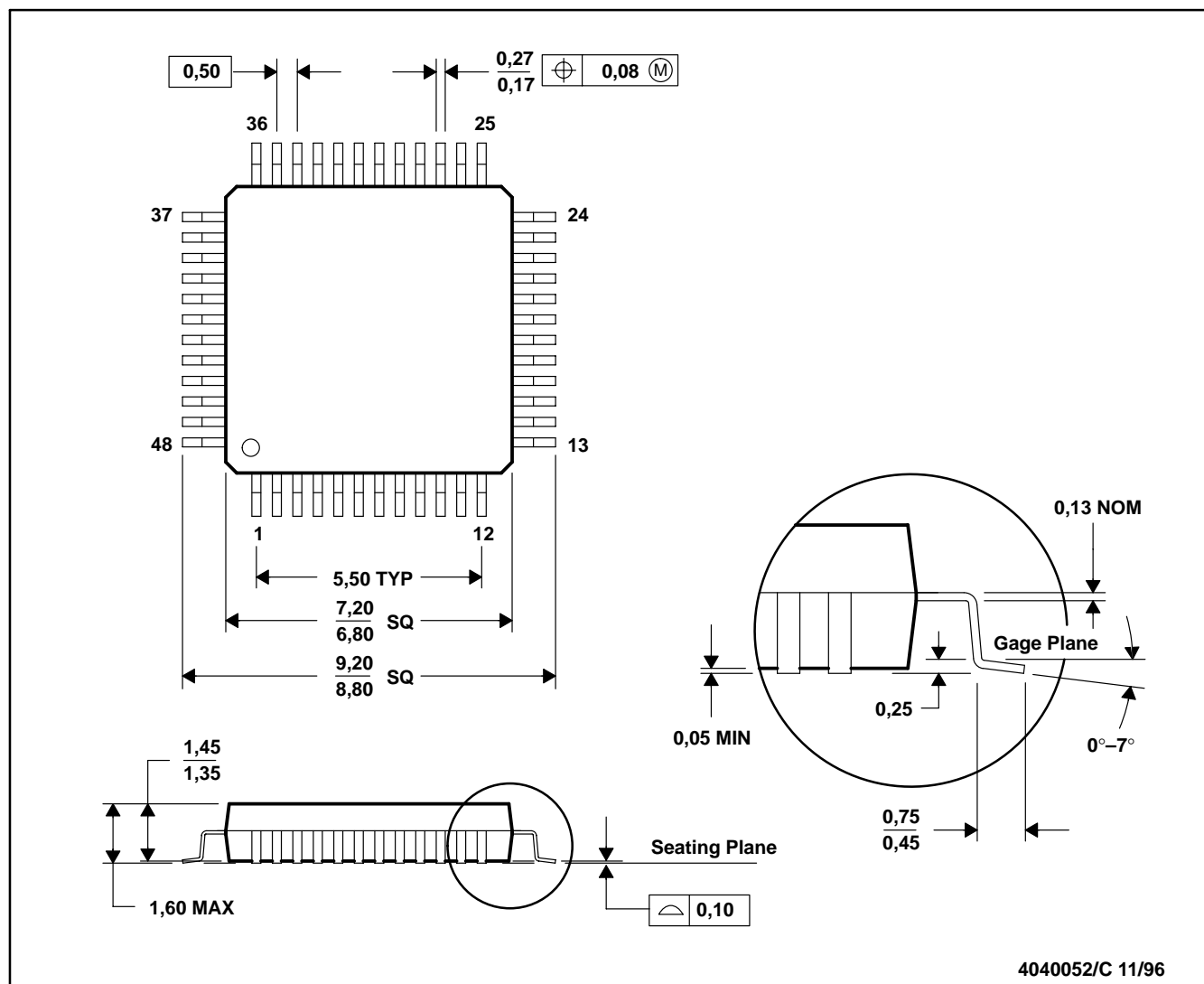
NOTES: A. All linear dimensions are in millimeters.
           B. This drawing is subject to change without notice.
           C. Falls within JEDEC MS-026
           D. This may also be a thermally enhanced plastic package with leads conected to the die pads.

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