Philips Semiconductors

The UAA3536 is a low-power GSM triple-band transceiver based on the N-ZIF (Near-Zero Intermediate Frequency) RF architecture. The UAA3536 is a GSM900/1800/1900 GPRS class 12-capable single-chip RF solution, with edge 4RX capabilities.

UAA3536

Low-power GSM/GPRS/EDGE triple-band Near-Zero IF transceiver

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Key Features

- Triple-band RF solution for GSM900/1800/1900 cellular phone systems
- Integrated on-chip data services: GPRS Class 12 (4RX-4TX) with data rate up to 57.6kB/s and EDGE (4RX) with data rate up to 237kb/s
- Low-cost N-ZIF architecture because of the low external components count
- Excellent power consumption performance
- Low noise and wide dynamic range Near Zero IF receiver:
  - More than 35-dB on-chip image rejection in receive
  - More than 84-dB gain control range in receive
- Integrated IF channel filter
- Integrated TX low pass filters
- High precision I&Q modulator
- Multi-Band Tx modulation loop architecture including offset mixer and phase-frequency detector
- Fully integrated fractional N RF synthesizer with AFC control capability
- Fully integrated RF VCO with integrated supply regulator
- Semi integrated reference oscillator with integrated supply regulator
- Fully differential design minimizing cross-talk and spurs
- Functional down to 2.6 V and up to 3.6 V
- 3-wire serial bus interface
- HVQFN40 package

The UAA3536 N-ZIF architecture, targeted at triple-band GSM900/1800/1900 GPRS Class 12 handsets with EDGE receiving capability, integrates many different features including a high dynamic range IF channel filter, a low-noise amplifier (LNA) with image rejecting front end, Fractional N frequency synthesizers and a transmit offset loop with integrated filters. It provides a definitive advantage compared to Zero-IF (ZIF) solutions in terms of immunity to interference, RF development cost, time and manufacturing.

This new architecture removes a conversion step between the RF and the baseband. Compared to other architectures, N-ZIF allows to remove the costly external IF channel filter. With the full integration of Rx VCO and fractional N synthesizer, it is a major innovation step towards higher integration within RF ICs.

Availability

The UAA3536 single-chip RF transceiver is about to sample, with mass production expected by mid 2001. It is manufactured in Philips Semiconductors' advanced QUBIC 3 BiCMOS process and is packaged in an HVQFN 40 package.

The UAA3536 interfaces with current and future Philips Semiconductors' products and will be at the heart of the company's chipset offerings. The IC will be fully compatible with OneC Baseband family, the new CGY2015 power amplifier and the PCF5060x power management unit platform.

UAA3536

Key Blocks

RF Receiver

The receiver front-end converts the aerial RF signal from EGSM (925 - 960 MHz), DCS (1805 - 1880 MHz) or PCS (1930 - 1990 MHz) bands down to a Near-Zero intermediate frequency (IF). The first stages are symmetrical low noise amplifiers (LNAs), followed by an I&Q down-mixer. The I&Q down-mixer consists of two mixers in parallel but is driven by quadrature out of phase LO signals. The In phase (I) and Quadrature phase (Q) IF signals are then low pass filtered to provide protection from high frequency offset interferers. The Near-Zero IF I and Q signals are then fed into the channel filter.

Channel filter and AGC

The front-end near Zero IF I and Q outputs enters the integrated bandpass channel filter. Being filtered the Near-Zero IF I and Q are further amplified with provision for 68dB Automatic Gain Control (AGC) and DC offset compensation. The IF channel is able to program the bandwidth between GSM and EDGE, to allow optimum performance in each mode.

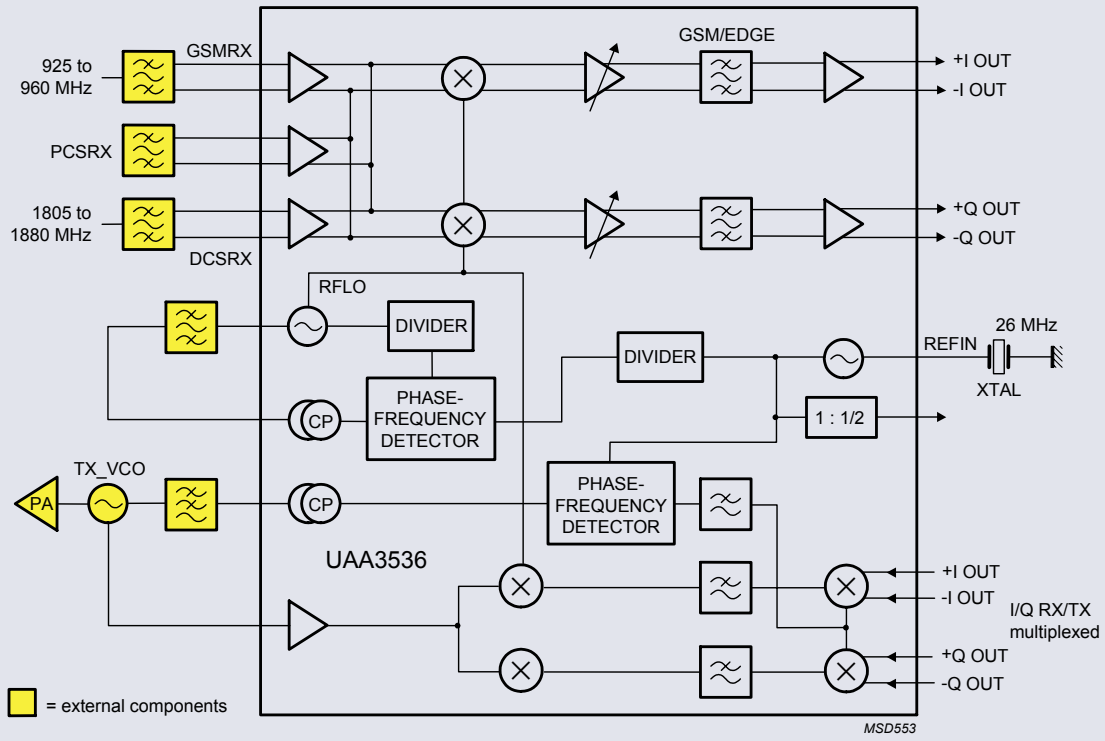
IQ modulator

I and Q baseband signals are applied to the IQ modulator that shifts the modulation spectrum up to the transmit IF. It is designed for low harmonic distortion, low carrier leakage and high image rejection to harmonic distortion, low carrier leakage and high image rejection to keep the phase error as small as possible. The modulator is loaded at its IF output by an integrated low pass filter that suppress unwanted spurs prior to get into the phase detector.

Transmit modulation loop

The analog transmit modulation loop is composed by on-chip offset mixer, a phase/frequency detector working in and by off-chip loop filter and transmit VCO. The analog PLL copies the modulation to the off-chip transmit VCO and acts as a tracking filter. A PLL of at least third order is required to meet noise requirements at 20 MHz offset from carrier. The PLL bandwidth is optimized in order to keep a low dynamic phase error and to minimize the acquisition time.

UAA3536 TRIPLE BAND GSM/EDGE(Rx) NZIF TRANSCEIVER



RF and IF LO sections

The RF LO input covering the 1788 to 2002 MHz bandwidth is connected to an internal RF VCO. The RF LO section includes the LO buffering for the RF PLL, a divider by two or one for GSM and DCS/PCS respectively which drives a quadrature generation network for use in the RX IQ down-mixer or the transmit modulation loop offset mixer. A new TX architecture does not require any IF LO.

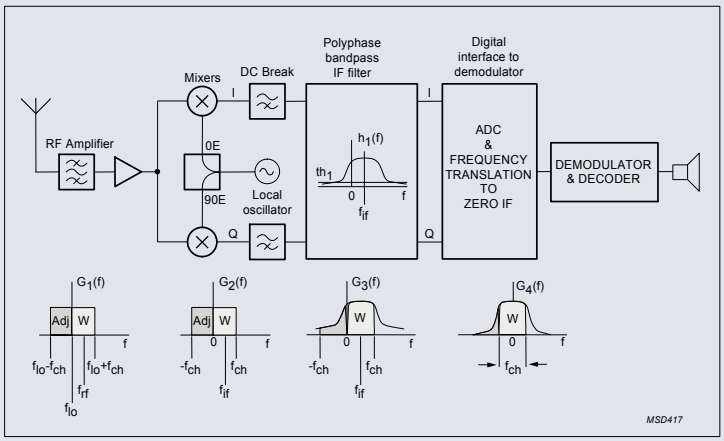
Dual PLL

A high performance RF fractional N PLL is included on chip which allows to synthesize the frequencies of the RF VCO on chip. Very low close-in phase noise is achieved allowing to widen the PLL loop bandwidth for shorter settling time, providing GPRS Class 12 capabilities in terms of hardware. The charge pump circuit has very low leakage current, in the nA range, so that the spurs are hardly detectable.

The programmable 'main' dividers are controlled by a Sigma Delta modulus divider. Their phase of the signal divided is then compared into a digital phase/frequency detector (PFD) to that of the 26MHz reference clock signal. The phase error information is fed back to the VCO via the charge pump circuit that 'sinks' into or 'sources' current from the loop filter capacitor, changing the VCO frequency such that the loop gets finally 'phase locked'.

N-ZIF architecture

The N-ZIF architecture integrates many different features including a high dynamic range IF channel filter, a low-noise amplifier (LNA) with image rejecting front end, fractional N frequency synthesizers and a transmit offset loop with integrated filters. It provides a definitive advantage compared to Zero-IF (ZIF) solutions in terms of immunity to interference, RF development cost, time and manufacturing. In addition to providing simplified signal processing for GSM applications, the high integration level it achieves provides significant cost and size reductions.



Near-Zero IF architecture - it eliminates the need for an external SAW filter and also prevents DC errors by allowing a DC break to be inserted into the IF path. The filters that are required are non-critical and can easily be implemented on-chip

Future

The UAA3536 joins a family of products that will pave the way for the continued evolution of GSM and the progression to 3G. Philips Semiconductors' next product offering will be focussed on 3G, with an even higher level of integration and new multimedia features to keep the company at the leading edge of cellular technology.

In addition to providing enhanced data rate capabilities, Philips Semiconductors' next generation of chipsets will integrate new capabilities such as Bluetooth, MP3 (Moving Picture Experts Group Layer-3 Audio) and GPS (Global Positioning System), and will directly address 3G standards such as UMTS (Universal mobile Telecommunications System)and W-CDMA (Wide-band Code Division Multiple Access).

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