

μ PD98452

PRELIMINARY

ADSL Analog Front-End LSI

Features

- Leading-edge combination analog/digital LSI adopting 0.35 μ m CMOS process
- Incorporates $\Sigma\Delta$ -type ADC and DAC with 13.5 effective bits
- PGA function having wide input range
- Incorporates built-in reference voltage supply and clock generator
- Operates on 3.3 V, dissipates 0.6 W ; low-voltage and low power consumption
- 100-pin QFP package

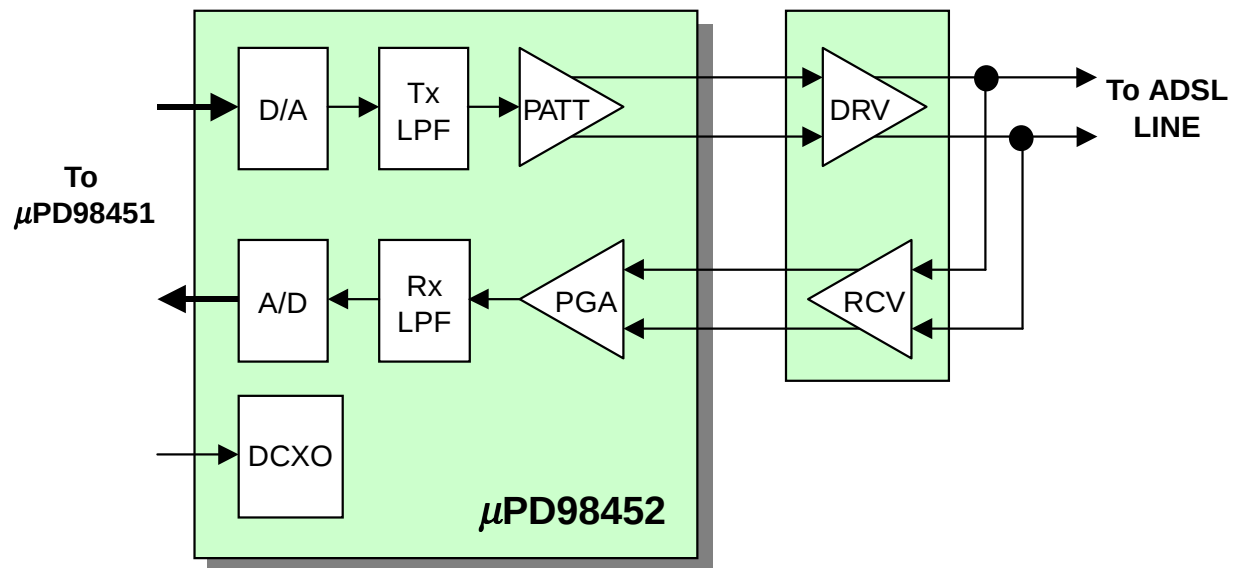
Receiver Features

Item	Value
PGA range	-26 to +22 dB
PGA step size	1.0 dB
Loopback noise filter (same for ATU-R and ATU-C)	cut-off: 1.104 MHz (MIN.) Degree 3rd
Output distortion	-84 dB (MAX.)
ADC resolution	16 bits
ADC valid bit	13.5 bits
ADC input range	1.2 Vpp
Output sample rate	8.8 MS/s

Transmitter Features

Item	Value
PATT range	0 to -12 dB
PATT step size	2.0 dB
Smoothing filter (same for ATU-R and ATU-C)	cut-off: 1.104 MHz (MIN.) Degree 3rd
Output distortion	-84 dB (MAX.)
DAC resolution	16 bits
DAC valid bit	13.5 bits
DAC output range	1.2 Vpp
Input sample rate	8.8 MS/s

Block Diagram



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