µPD98408 ATM PHYSICAL INTERFACE

The µPD98408 incorporates six 25.6 Mbps ATM physical interface circuits (ports) into a single chip, implementing complete physical layer functionality for transmission convergence (TC) and physical media dependent (PMD) sublayer functions. Each port has an encoder/decoder, scrambler/descrambler, line equalizer, and clock recovery circuit for totally independent channel operation. This device communicates with ATM layer devices using an integrated UTOPIA level 2 standard interface.

FEATURES

- Complies with the ATM Forum Specifications for 25.6 Mbps ATM interface
- Integrates six independent 25.6 Mbps physical interface circuits (ports)
- Performs NRZI and 4B/5B encoding and decoding functions
- Performs scrambler/descrambler, HEC generation/verification, and command byte insertion/detection functions
- Integrates an independent clock recovery and line equalizer circuit for each port
- Supports Operation and Maintenance (OAM) functions, including the detection of loss of signal (LOS), HEC errors, and 4B/5B code violations

BUS INTERFACE

- Uses the UTOPIA level 2 standard to ensure compatibility with multivendor ATM layer devices
- Provides a generic processor interface for device programming/option selection and status data gathering

MEDIA INTERFACE

- Supports STP and UTP (categories 3, 4 and 5) cable types

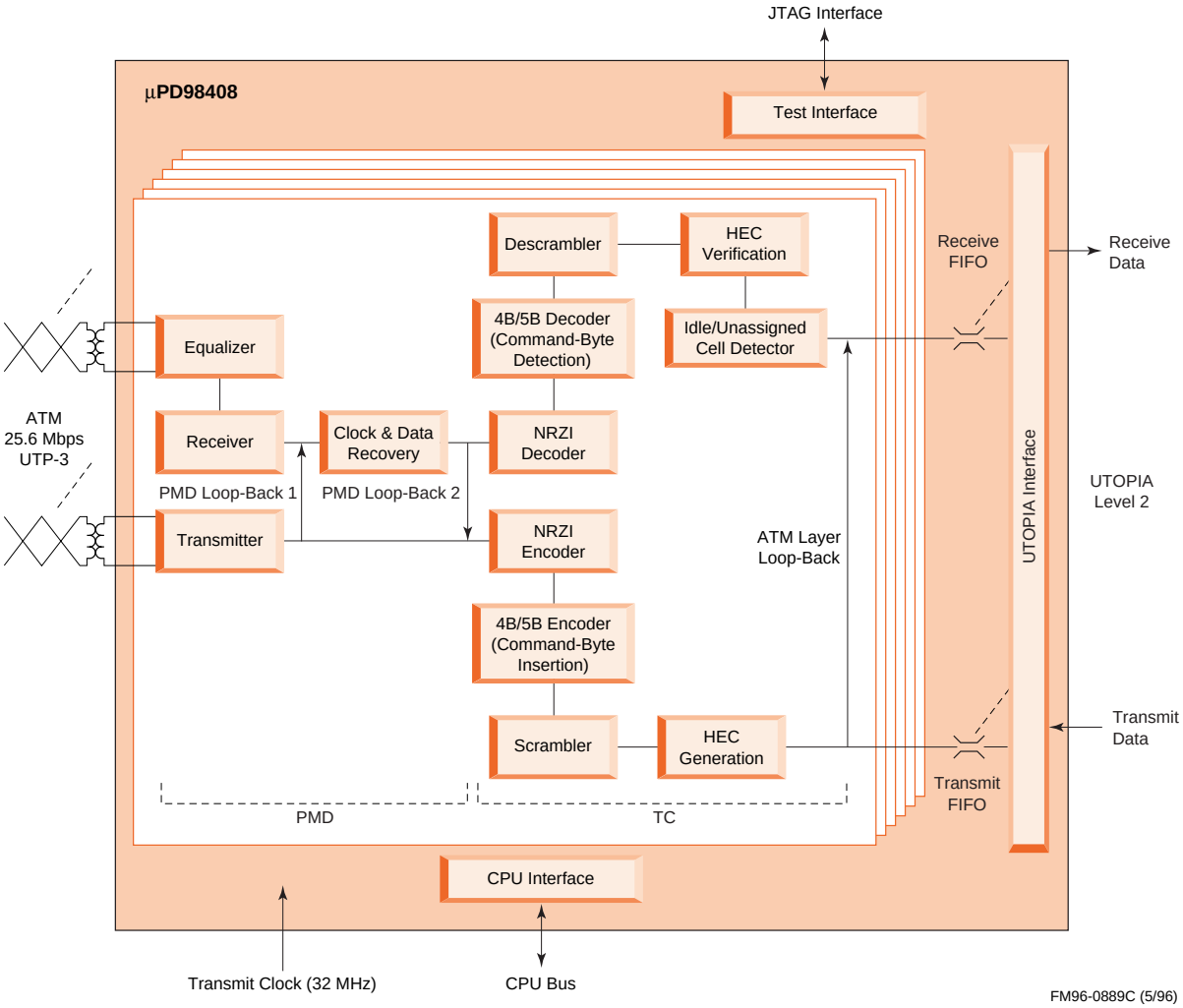
GENERAL

- Provides diagnostic capabilities: loopback of receive data at the physical side and transmit data at the UTOPIA interface, test signal generation and error insertion option
- Supports JTAG Boundary Scan
- Low-power CMOS technology (3.3-volt supply voltage)
- 208-pin plastic QFP package

APPLICATIONS

- ATM concentrators/multiplexers
- ATM switches/hubs
- WAN access devices

BLOCK DIAGRAM



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