Standard Products

UT4090 RadHard FPGA

Advanced Data Sheet

August 3, 2001, Rev D

IN DEVELOPMENT

FEATURES

- 0.35µm four-layer metal, anti-fuse epitaxial CMOS process for smallest die sizes
- One-time programmable, ViaLink™ antifuse technology for personalization
- 150 MHz 16-bit counters, 200 MHz datapaths, 80+ MHz FIFOs
- 90,000 usable PLD gates (non-volatile)
- I/Os
  - Interfaces with both 3.3 volt and 5 volt devices
  - PCI compliant with 3.3V and 5V busses
  - Full JTAG 1149.1 compliant
  - Registered I/O cells with individually controlled clocks and output enables
- Radiation-hardened design; total dose irradiation testing to MIL-STD-883 Test Method 1019
  - Total-dose: 30 krad(Si)
  - SEL Immune TBD
  - $LET_{TH}(0.25)$ TBD
  - Saturated Cross Section cm^2 per bit - TBD
- 22 dual-port RAM modules, organized in user-configurable 1,152 bit blocks
  - 5ns access times, each port independently accessible
  - Fast and efficient for FIFO, RAM, and ROM functions
- 100% routable with 100% utilization and complete pin-out stability
- Variable-grain logic cells provide high performance and 100% utilization
- Comprehensive design tools include high quality Verilog/ VHDL synthesis and simulation
- QuickLogic existing IP such as microcontrollers, DRAM controllers, USART and PCI can be accessed
- Packaged in a 208-pin Cerquad Flatpack
- Standard Microcircuit Drawing TBD
  - QML Q and T compliant part

INTRODUCTION

The UT4090 RadHard Field Programmable Gate Array (FPGA) offers 90,000 usable PLD gates including Dual-Port SRAM modules. It is fabricated on 0.35µm four-layer metal CMOS process. The UT4090 contains 1,584 logic cells and 22 dual port RAM modules (see Figure 1). Each RAM module has 1,152 RAM bits, for a total of 25,344 bits. RAM modules are Dual Port (one read port, one write port) and can be configured into one of four modes: 64 (deep) x 18(wide), 128x9, 256x4, or 512x2 (see Figure 2). The UT4090 is available in a 208-pin Cerquad Flatpack, allowing access to 166 bidirectional signal I/O, 8 high drive inputs, and 5 JTAG I/O.

Designers can cascade multiple RAM modules to increase the depth or width allowed in single modules by connecting corresponding address lines together and dividing the words between modules (see Figure 3). This approach allows a variety of address depths and word widths to be tailored to a specific application.

Aeroflex UTMC uses QuickLogic Corporation's licensed ESP (Embedded Standard Products) technology for the UT4090. QuickLogic is a pioneer in the FPGA semiconductor and the software tools field.

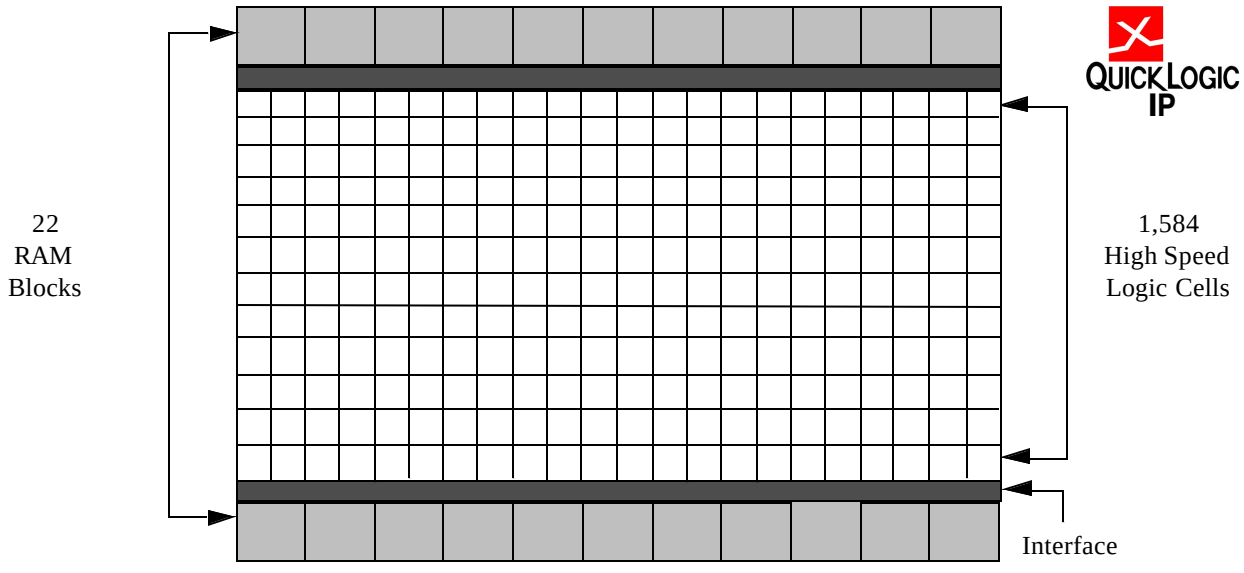


Figure 1. UT4090 FPGA Block Diagram

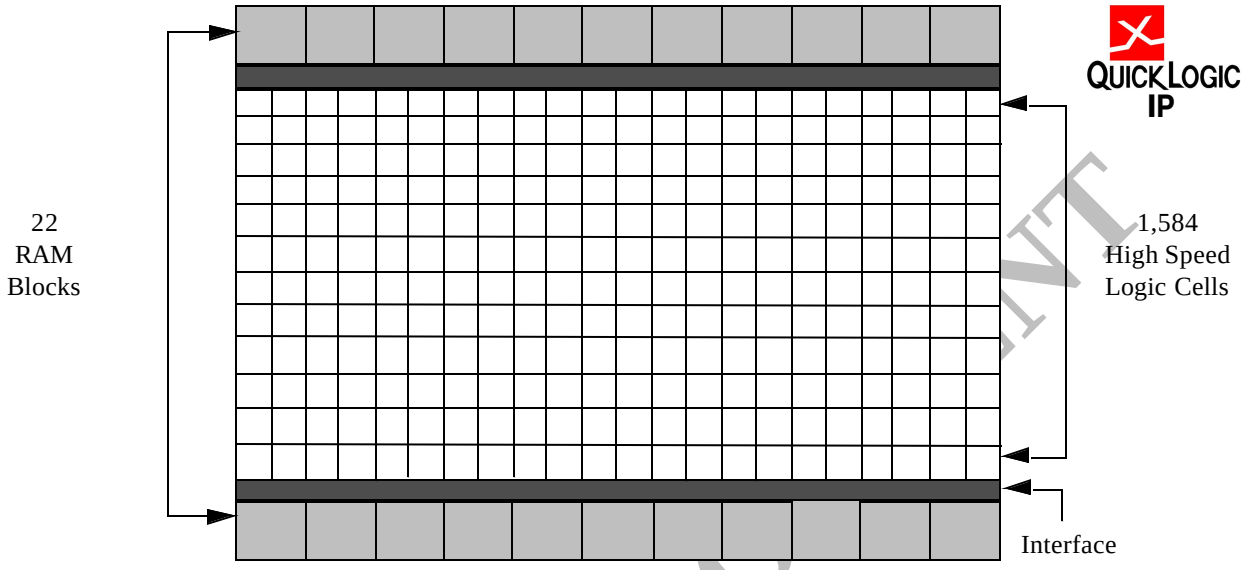


Figure 1. UT4090 FPGA Block Diagram

IN DEVELOPMENT

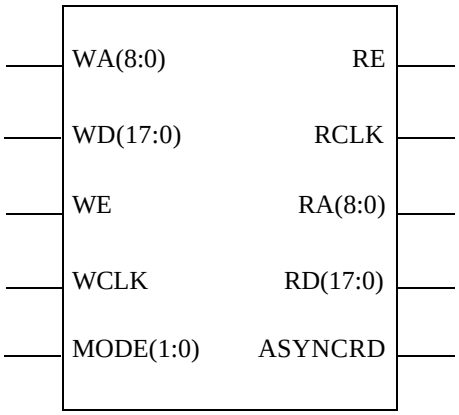


Figure 2. UT4090 FPGA RAM Module

Software support for the UT4090 is available from QuickLogic. The turnkey QuickWorks™ package provides the most complete software solution from design entry to logic synthesis, place and route, simulation and static timing analysis. The QuickTools ™ for Workstations package provides a solution for designers who use Cadence, Exemplar, Mentor, Synopsys, Synplicity, Viewlogic, Veribest or other third-party tools for design entry, synthesis or simulation. Please visit Quick Logic's website at www.quicklogic.com for more information.

The UT4090 variable grain logic cell features up to 16 simultaneous inputs and 5 outputs within a cell that can be fragmented into 5 independent cells. Each cell has a fan-in of 29 including register and control lines (see Figure 5).

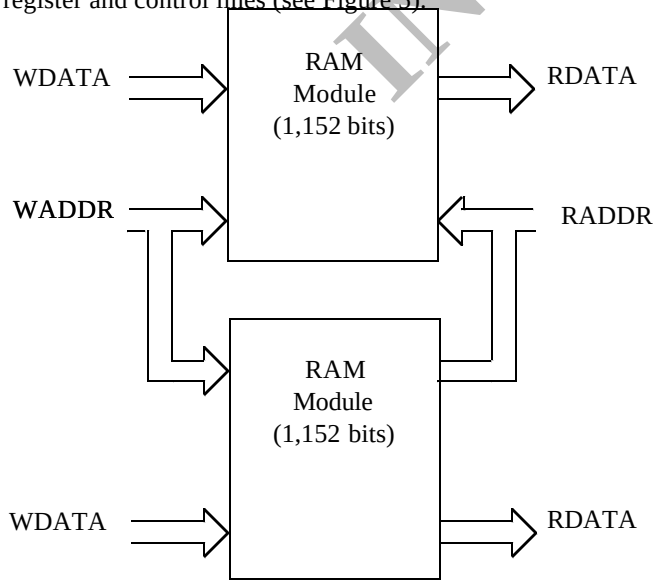


Figure 3. UT4090 FPGA Module Bits

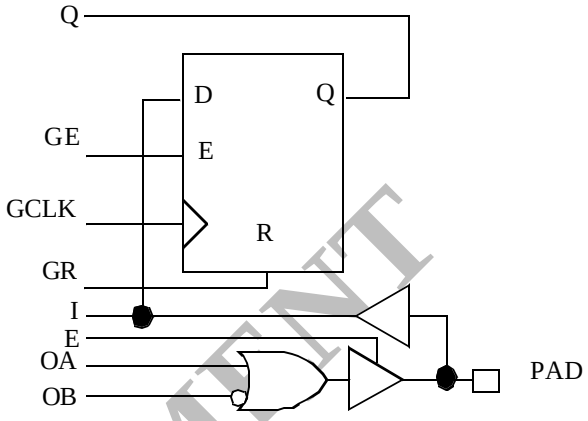


Figure 4. UT4090 FPGA I/O Cell

IN DEVELOPMENT

PRODUCT DESCRIPTION

I/O Pins

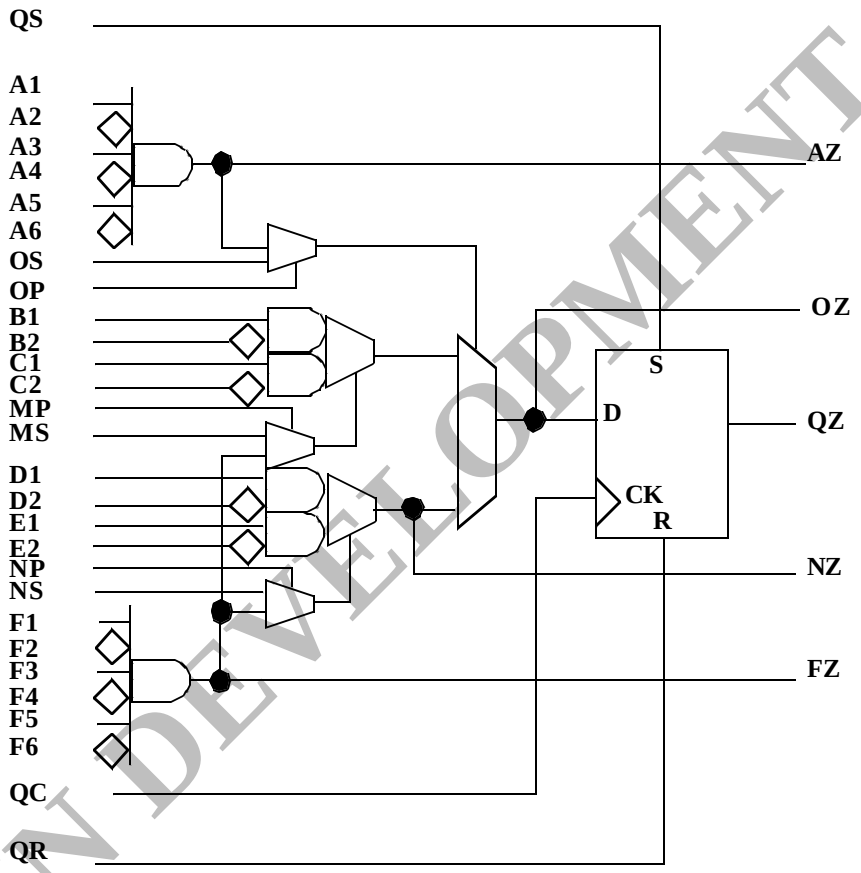
- 308 bi-directional input/output pins, PCI-compliant for 5V and 3.3V buses (see Figure 4)
- 8 high-drive input distributed network pins

Distributed Networks

- Two array clock/control networks available to the logic cell flip-flop clock, set and reset inputs - each driven by an input-only pin
- Six global clock/control networks available to the logic cell F1, flip-flop clock, set and reset inputs and the input and I/O register clock, reset and enable inputs, as well as the output enable control - each driven by an input-only or I/O pin, or any logic cell output, or I/O cell feedback.

Performance

- Input + logic cell + output total delays under 12ns
- Data path speeds over 200 MHz
- Counter speeds over 150 MHz
- FIFO speeds over 80+ MHz



IN DEVELOPMENT

Figure 5. UT4090 FPGA Logic Cell

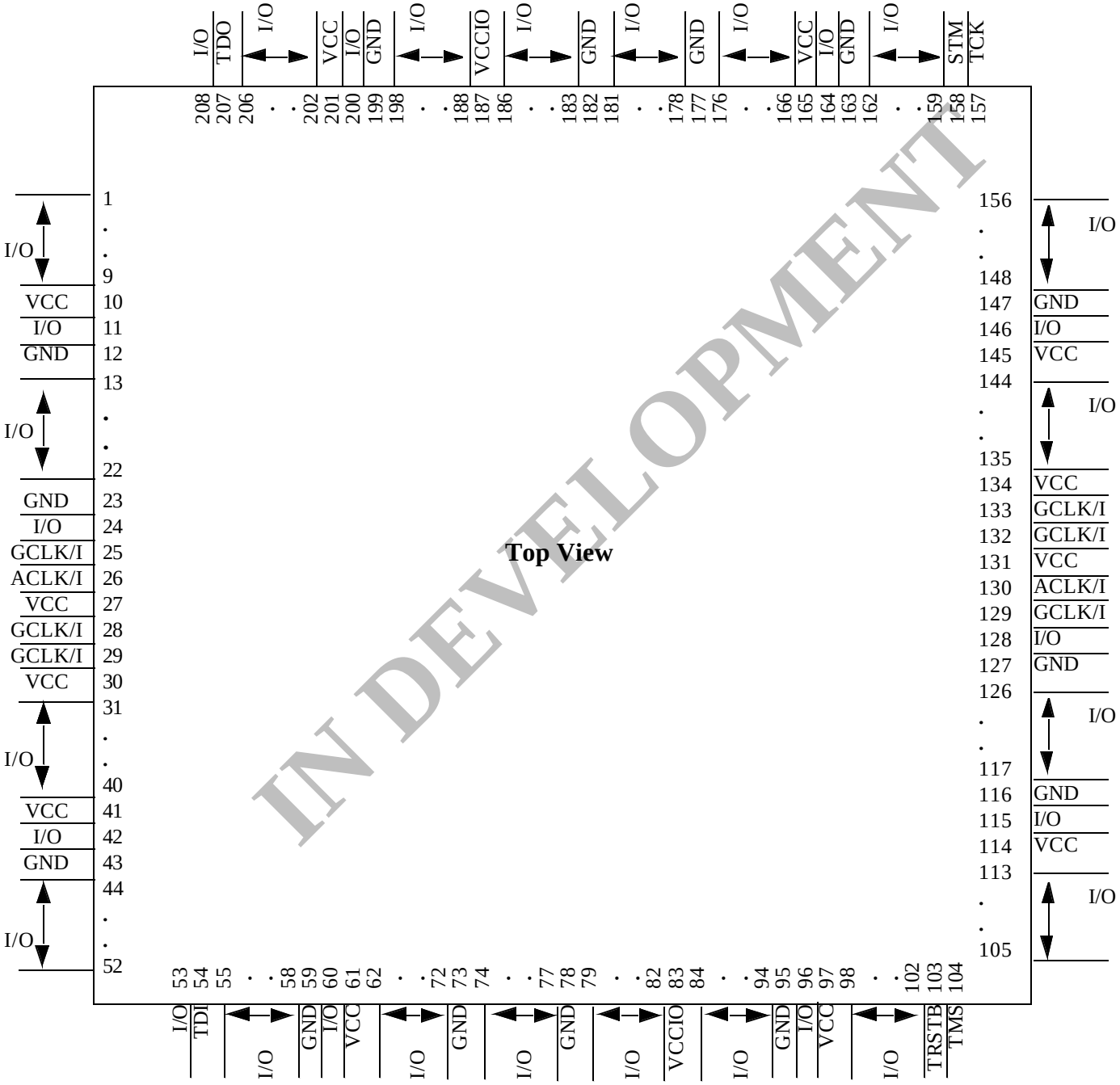


Figure 6. UT4090 FPGA Logic 208 Pinout

Table 1: UT4090 208-pin Cerquad Flatpack Pinout Table

1	I/O	**36**	I/O	**71**	I/O	**106**	I/O	**141**	I/O	**176**	I/O
2	I/O	**37**	I/O	**72**	I/O	**107**	I/O	**142**	I/O	**177**	GND
3	I/O	**38**	I/O	**73**	GND	**108**	I/O	**143**	I/O	**178**	I/O
4	I/O	**39**	I/O	**74**	I/O	**109**	I/O	**144**	I/O	**179**	I/O
5	I/O	**40**	I/O	**75**	I/O	**110**	I/O	**145**	VCC	**180**	I/O
6	I/O	**41**	VCC	**76**	I/O	**111**	I/O	**146**	I/O	**181**	I/O
7	I/O	**42**	I/O	**77**	I/O	**112**	I/O	**147**	GND	**182**	GND
8	I/O	**43**	GND	**78**	GND	**113**	I/O	**148**	I/O	**183**	I/O
9	I/O	**44**	I/O	**79**	I/O	**114**	VCC	**149**	I/O	**184**	I/O
10	VCC	**45**	I/O	**80**	I/O	**115**	I/O	**150**	I/O	**185**	I/O
11	I/O	**46**	I/O	**81**	I/O	**116**	GND	**151**	I/O	**186**	I/O
12	GND	**47**	I/O	**82**	I/O	**117**	I/O	**152**	I/O	**187**	VCCIO
13	I/O	**48**	I/O	**83**	VCCIO	**118**	I/O	**153**	I/O	**188**	I/O
14	I/O	**49**	I/O	**84**	I/O	**119**	I/O	**154**	I/O	**189**	I/O
15	I/O	**50**	I/O	**85**	I/O	**120**	I/O	**155**	I/O	**190**	I/O
16	I/O	**51**	I/O	**86**	I/O	**121**	I/O	**156**	I/O	**191**	I/O
17	I/O	**52**	I/O	**87**	I/O	**122**	I/O	**157**	TCK	**192**	I/O
18	I/O	**53**	I/O	**88**	I/O	**123**	I/O	**158**	STM	**193**	I/O
19	I/O	**54**	TDI	**89**	I/O	**124**	I/O	**159**	I/O	**194**	I/O
20	I/O	**55**	I/O	**90**	I/O	**125**	I/O	**160**	I/O	**195**	I/O
21	I/O	**56**	I/O	**91**	I/O	**126**	I/O	**161**	I/O	**196**	I/O
22	I/O	**57**	I/O	**92**	I/O	**127**	GND	**162**	I/O	**197**	I/O
23	GND	**58**	I/O	**93**	I/O	**128**	I/O	**163**	GND	**198**	I/O
24	I/O	**59**	GND	**94**	I/O	**129**	GCLK/I	**164**	I/O	**199**	GND
25	GCLK/I	**60**	I/O	**95**	GND	**130**	ACLK/I	**165**	VCC	**200**	I/O
26	ACLK/I	**61**	VCC	**96**	I/O	**131**	VCC	**166**	I/O	**201**	VCC
27	VCC	**62**	I/O	**97**	VCC	**132**	GCLK/I	**167**	I/O	**202**	I/O
28	GCLK/I	**63**	I/O	**98**	I/O	**133**	GCLK/I	**168**	I/O	**203**	I/O
29	GCLK/I	**64**	I/O	**99**	I/O	**134**	VCC	**169**	I/O	**204**	I/O
30	VCC	**65**	I/O	**100**	I/O	**135**	I/O	**170**	I/O	**205**	I/O
31	I/O	**66**	I/O	**101**	I/O	**136**	I/O	**171**	I/O	**206**	I/O
32	I/O	**67**	I/O	**102**	I/O	**137**	I/O	**172**	I/O	**207**	TDO
33	I/O	**68**	I/O	**103**	TRSTB	**138**	I/O	**173**	I/O	**208**	I/O
34	I/O	**69**	I/O	**104**	TMS	**139**	I/O	**174**	I/O		
35	I/O	**70**	I/O	**105**	I/O	**140**	I/O	**175**	I/O		

IN DEVELOPMENT

Table 2: UT4090 Pin Description

PIN	FUNCTION	DESCRIPTION
TDI/RSI	Test data in for JTAG/RAM initialization Serial Data In	Hold HIGH during normal operation. Connects to serial PROM data in for RAM initialization. Connect to VCC if unused.
TRSTB/RRO	Active low reset for JTAG/ RAM initialization reset out	Hold LOW during normal operation. Connects to serial PROM reset for RAM initialization. Connect to GND if unused.
TMS	Test mode select for JTAG	Hold HIGH during normal operation. Connect to VCC if not used for JTAG.
TCK	Test clock for JTAG	Hold HIGH or LOW during normal operation. Connect to VCC or ground if not used for JTAG.
TDO/RCO	Test data out for JTAG/RAM initialization clock out	Connect to serial PROM clock for RAM initialization. Must be left unconnected if not used for JTAG or RAM initialization.
STM	Special Test Mode	Must be grounded during normal operation.
I/ACLK	High-drive input and/or array network driver	Can be configured as either or both.
I/GCLK	High-drive input and/or global network driver	Can be configured as either or both
I	High-drive input	Use for input signals with high fanout
I/O	Input/Output pin	Can be configured as an input and/or output
V_{CC}	Power supply pin	Connect to 3.3V supply
V_{CCIO}	Input voltage tolerance pin	Connect to 5V supply if 5 volt input tolerance is required, otherwise connect to 3.3V supply
GND	Ground pin	Connect to ground

IN DEVELOPMENT

ABSOLUTE MAXIMUM RATINGS[1]
(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS
V_{CC}	Core supply voltage	-0.5 to 4.6V
V_{CCIO}	I/O supply voltage	-0.5 to 7.0V
$V_{I/O}$	Voltage on any pin	-0.5 to V_{CCIO} +0.5V
I_{LU}	Latch-up Immunity	±200mA
T_J	Maximum junction temperature[2]	-65°C to +150°C
ESDS	ESD pad protection	Class 1
I_I	DC input current	±20 mA
T_{LS}	Lead Temperature	300°C

Notes:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Maximum junction temperature may be increased to TBD during burn-in and steady-static life.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
V_{CC}	Core supply voltage	3.0 to 3.6V
V_{IO}	I/O Input Tolerance Voltage	3.0 to 5.5V
TA	Ambient Temperature	-55°C to +125°C
K[1]	Delay factor for RadHard FPGA	0.42 to 2.03

Notes:
1. To conclude best and worst case delays, multiply the RadHard K factor from the operating conditions with the delay values defined in the following AC delay tables.

IN DEVELOPMENT

DC ELECTRICAL CHARACTERISTICS (Pre/Post-Radiation)*

(-55°C to +125°C) (V_{DD} = 5.0V ± 10%)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V_{IH}	High-level input voltage		.5 V_{CC}	V_{CCIO}+.5	V
V_{IL}	Low-level input voltage		-.5	.3 V_{CC}	V
V_{OL1}	Low-level output voltage	I_{OL} = 8mA		.45	V
V_{OL2}	Low-level output voltage	I_{OL} =1.5mA		.1 V_{CC}	V
V_{OH1}	High-level output voltage	I_{OH} = -12mA	2.4		V
V_{OH2}	High-level output voltage	I_{OH} = -500µA	.9 V_{CC1}		V
C_{IN}[1]	Input capacitance	*f* = 1MHz @ 0V		10	pF
C_{INCLK}	Clock pin input capacitance	*f* = 1MHz @ 0V		12	pF
I_{IN}	Input leakage current	V_I = V_{CCIO} or Gnd	-10	10	µA
I_{OZ}	Three-state output leakage current	V_I = V_{CCIO} or Gnd	-10	10	µA
I_{OS}[2, 3]	Short-circuit output current	V_O = GND V_O = V_{CCIO}	-15 40	-180 210	mA mA
I_{CC}	DC supply current	V_I, V_O = V_{CCIO} or GND	.50	5	mA
I_{DD1}(OP)	DC supply current on V_{CCIO}		0	100	µA

Notes:

* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.

1. Capacitance is sample tested for initial qualification or design changes only.
2. Input only or I/O.
3. Not more than one output may be shorted at a time for maximum duration of one second.

IN DEVELOPMENT

AC CHARACTERISTICS LOGIC CELLS

(V_{CC} = 3.3V, TA = 25°C (K=1.00)

SYMBOL	PARAMETER	Propagation Delays (ns) Fanout[1]				
		1	2	3	4	8
T_{PD}	Combinatorial Delay[2]	1.4	1.7	1.9	2.2	3.2
T_{SU}	Setup Time[2]	1.7	1.7	1.7	1.7	1.7
T_{H}	Hold Time	0.0	0.0	0.0	0.0	0.0
T_{CLK}	Clock to Q Delay	0.7	1.0	1.2	1.5	2.5
T_{CWHI}	Clock High Time	1.2	1.2	1.2	1.2	1.2
T_{CWLO}	Clock Low Time	1.2	1.2	1.2	1.2	1.2
T_{SET}	Set Delay	1.0	1.3	1.5	1.8	2.8
T_{RESET}	Reset Delay	0.8	1.1	1.3	1.6	2.6
T_{SW}	Set Width	1.9	1.9	1.9	1.9	1.9
T_{RW}	Reset Width	1.8	1.8	1.8	1.8	1.8

Notes: * Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.

1. Stated timing for typical case propagation delay over process variation at V_{CC}=3.3V and TA=25°C. Multiply by the appropriate delay factor, K, for voltage and temperature settings as specified in operating range.
2. These limits are derived from a representative selection of the slowest paths through the logic cell including typical net delays. Worst case delay values for specific paths should be determined from timing analysis of your particular design.

IN DEVELOPMENT

AC CHARACTERISTICS RAM CELL SYNCHRONOUS WRITE TIMING

V_{CC} = 3.3V, TA = 25°C (K=1.00)

SYMBOL	PARAMETER	Propagation Delays (ns) Fanout				
		1	2	3	4	8
T_{SWA}	WA Setup time to WCLK	1.0	1.0	1.0	1.0	1.0
T_{HWA}	WA Hold time to WCLK	0.0	0.0	0.0	0.0	0.0
T_{SWD}	WD Setup time to WCLK	1.0	1.0	1.0	1.0	1.0
T_{HWD}	WD Hold time to WCLK	0.0	0.0	0.0	0.0	0.0
T_{SWE}	WE Setup time to WCLK	1.0	1.0	1.0	1.0	1.0
T_{HWE}	WE Hold time to WCLK	0.0	0.0	0.0	0.0	0.0
T_{WCRD}	WCLK to RD (WA=RA)[1]	5.0	5.3	5.6	5.9	7.1

Notes: * Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.

1. Stated timing for typical case propagation delay over process variation at V_{CC}=3.3V and TA=25°C. Multiply by the appropriate delay factor, K, for voltage and temperature settings as specified in operating range.

AC CHARACTERISTICS RAM CELLS SYNCHRONOUS READ TIMING

V_{CC} = 3.3V, TA = 25°C (K=1.00)

SYMBOL	PARAMETER	Propagation Delays (ns) Fanout				
		1	2	3	4	8
T_{SRA}	RA Setup time to RCLK	1.0	1.0	1.0	1.0	1.0
T_{HRA}	RA Hold time to RCLK	0.0	0.0	0.0	0.0	0.0
T_{SRE}	RE Setup time to RCLK	1.0	1.0	1.0	1.0	1.0
T_{HRE}	RE Hold time to RCLK	0.0	0.0	0.0	0.0	0.0
T_{RCRD}	RCLK to RD[1]	4.0	4.3	4.6	4.9	6.1

Notes: * Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.

1. Stated timing for typical case propagation delay over process variation at V_{CC}=3.3V and TA=25°C. Multiply by the appropriate delay factor, K, for voltage and temperature settings as specified in operating range.

AC CHARACTERISTICS RAM CELLS ASYNCHRONOUS READ TIMING

V_{CC} = 3.3V, TA = 25°C (K=1.00)

SYMBOL	PARAMETER	Propagation Delays (ns) Fanout				
		1	2	3	4	8
R_{PDRD}	RA TO RD[1]	3.0	3.3	3.6	3.9	5.1

Notes: * Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.

1. Stated timing for typical case propagation delay over process variation at V_{CC}=3.3V and TA=25°C. Multiply by the appropriate delay factor, K, for voltage and temperature settings as specified in operating range.

IN DEVELOPMENT

AC CHARACTERISTICS INPUT-ONLY/CLOCK CELLS

V_{CC} = 3.3V, TA = 25°C (K=1.00)

SYMBOL	PARAMETER	Propagation Delays (ns) Fanout[1]						
		1	2	3	4	8	12	24
T_{IN}	High drive input delay	1.5	1.6	1.8	1.9	2.4	2.9	4.4
T_{INI}	High drive input, inverting delay	1.6	1.7	1.9	2.0	2.5	3.0	4.5
T_{ISU}	Input register set-up time	3.1	3.1	3.1	3.1	3.1	3.1	3.1
T_{IH}	Input register hold time	0.0	0.0	0.0	0.0	0.0	0.0	0.0
T_{ICLK}	Input register clock to Q	0.7	0.8	1.0	1.1	1.6	2.1	3.6
T_{IRST}	Input register reset delay	0.6	0.7	0.9	1.0	1.5	2.0	3.5
T_{IESU}	Input register clock enable setup time	2.3	2.3	2.3	2.3	2.3	2.3	2.3
T_{IEH}	Input register clock enable hold time	0.0	0.0	0.0	0.0	0.0	0.0	0.0

Notes: * Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.

1. Stated timing for typical case propagation delay over process variation at V_{CC}=3.3V and TA=25°C. Multiply by the appropriate delay factor, K for voltage and temperature settings as specified in operating range.

AC CHARACTERISTICS CLOCK CELLS

V_{CC} = 3.3V, TA = 25°C (K=1.00)

SYMBOL	PARAMETER	Propagation Delays (ns) Fanout[1, 2]						
		1	2	3	4	8	10	11
T_{ACK}	Array clock delay	1.2	1.2	1.3	1.3	1.5	1.6	1.7
T_{GCKP}	Global clock pin delay	0.7	0.7	0.7	0.7	0.7	0.7	0.7
T_{GCKB}	Global clock buffer delay	0.8	0.8	0.9	0.9	1.1	1.2	1.3

Notes: * Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.

1. The array distributed networks consist of 40 half columns and the global distributed networks consist of 44 half columns, each driven by an independent buffer. The number of half columns used does not affect clock buffer delay. The array clock has up to 8 loads per half column. The global clock has up to 11 loads per half column.
2. Stated timing for typical case propagation delay over process variation at V_{CC}=3.3V and TA=25°C. Multiply by the appropriate delay factor, K for voltage and temperature settings as specified in operating range.

IN DEVELOPMENT

AC CHARACTERISTICS I/O CELL INPUT DELAYS

V_{CC} = 3.3V, TA = 25°C (K=1.00)

SYMBOL	PARAMETER	Propagation Delays (ns) Fanout[1]					
		1	2	3	4	8	10
$T_{I/O}$	Input delay (Bidirectional pad)	1.3	1.6	1.8	2.1	3.1	3.6
T_{ISU}	Input register set-up time	3.1	3.1	3.1	3.1	3.1	3.1
T_{IH}	Input register hold time	0.0	0.0	0.0	0.0	0.0	0.0
T_{IOCLK}	Input register clock to Q	0.7	1.0	1.2	1.5	2.5	3.0
T_{IORST}	Input register reset delay	0.6	0.9	1.1	1.4	2.4	2.9
T_{IESU}	Input register clock enable set-up time	2.3	2.3	2.3	2.3	2.3	2.3
T_{IEH}	Input register clock enable hold time	0.0	0.0	0.0	0.0	0.0	0.0

Notes: * Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.

1. Stated timing for typical case propagation delay over process variation at V_{CC}=3.3V and TA=25°C. Multiply by the appropriate delay factor, K, for voltage and temperature settings as specified in operating range.

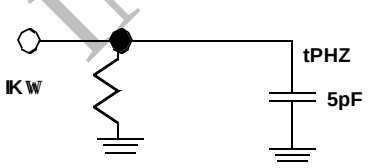
AC CHARACTERISTICS I/O CELL OUTPUT DELAYS

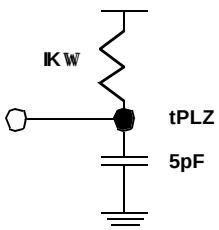
V_{CC} = 3.3V, TA = 25°C (K=1.00)

SYMBOL	PARAMETER	Propagation Delays (ns)[1] Output Load Capacitance (pF)				
		30	50	75	100	150
T_{IOUTLH}	Output delay low to high	2.1	2.5	3.1	3.6	4.7
T_{OUTHL}	Output delay high to low	2.2	2.6	3.2	3.7	4.8
T_{PZH}	Output delay tri-state to high	1.2	1.7	2.2	2.8	3.9
T_{PZL}	Output delay tri-state to low	1.6	2.0	2.6	3.1	4.2
T_{PHZ}	Output delay high to Tri-State[1]	2.0	n/a	n/a	n/a	n/a
T_{PLZ}	Output delay low to Tri- State[1]	1.2	n/a	n/a	n/a	n/a

Notes: * Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.

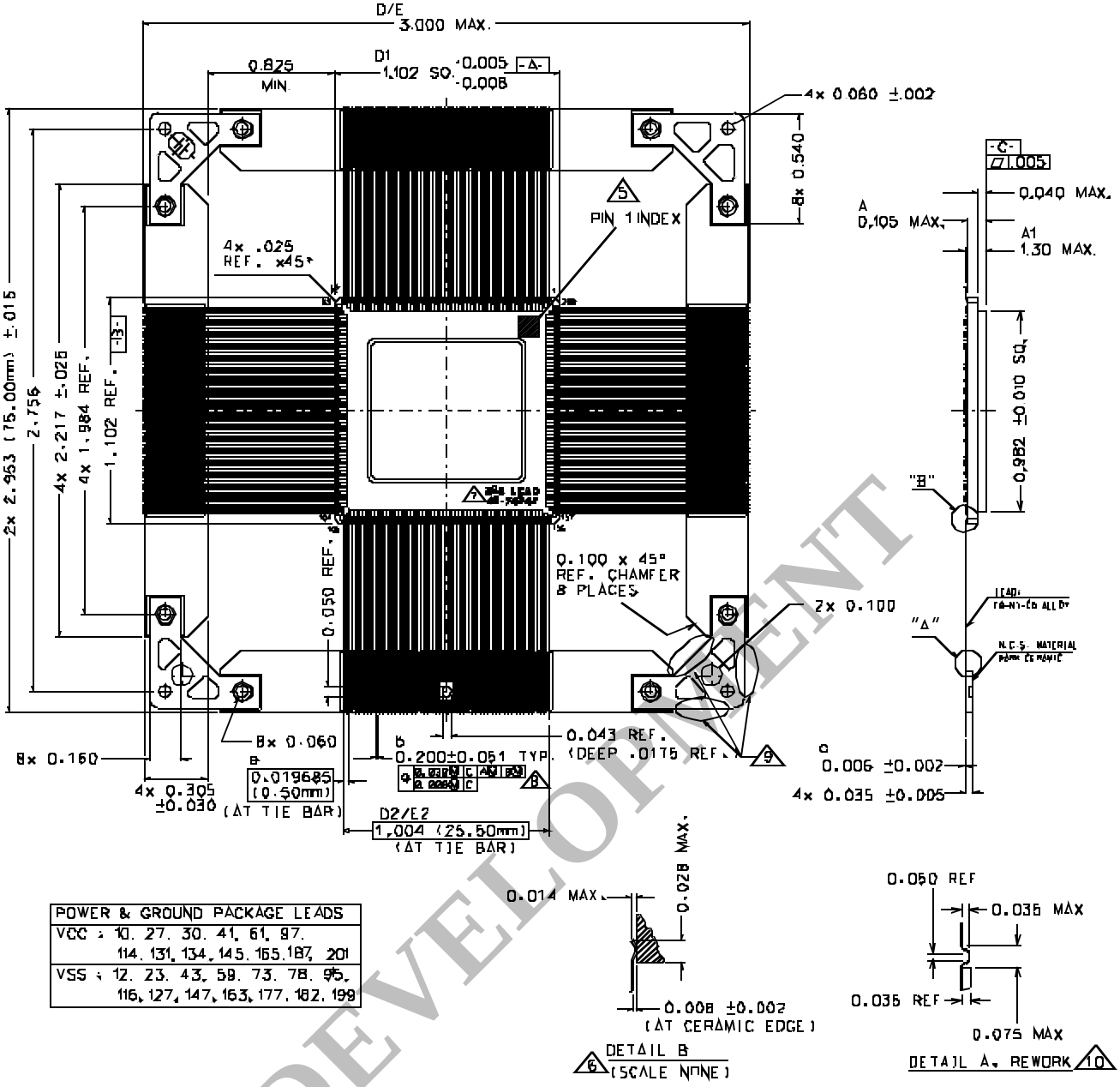
1. Stated timing for worst case propagation delay over process variation at V_{CC}=3.3V and TA=25°C. Multiply by the appropriate delay factor, K, for voltage and temperature settings as specified in operating range.
2. The following loads are used for T_{PXZ}.





IN DEVELOPMENT

PACKAGING



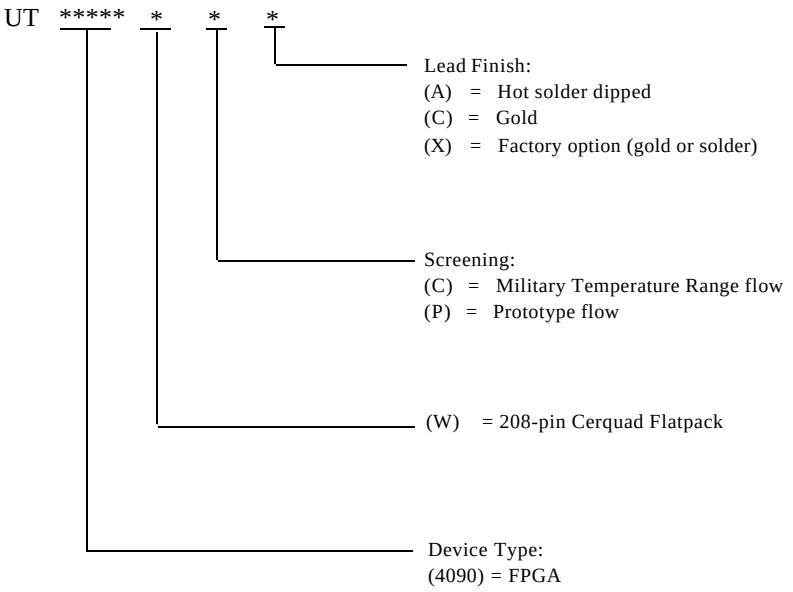
1. All exposed metalized areas are gold plated over electroplated nickel per MIL-PRF-38535.
2. Lead finishes are in accordance with MIL-PRF-38535.
3. Letter designations are to cross-reference to MIL-STD-1835.
4. The lid is connected to VSS; protruding cover dots are allowed.
5. Geometry optional and vendor option for shape.
6. Dogleg geometries are optional within dimensions shown.
7. Not subject to visual inspection criteria.
8. Lead true position tolerance and coplanarity are not measured.
9. These areas may have notches and tabs different than shown.
10. Packages may be shipped with repaired leads as shown. Coplanarity requirements do not apply in repaired areas.
11. Package weight is 14.82 grams.

Figure 7. 208-pin Ceramic FLATPACK

IN DEVELOPMENT

ORDERING INFORMATION

UT4090 RadHard FPGA:

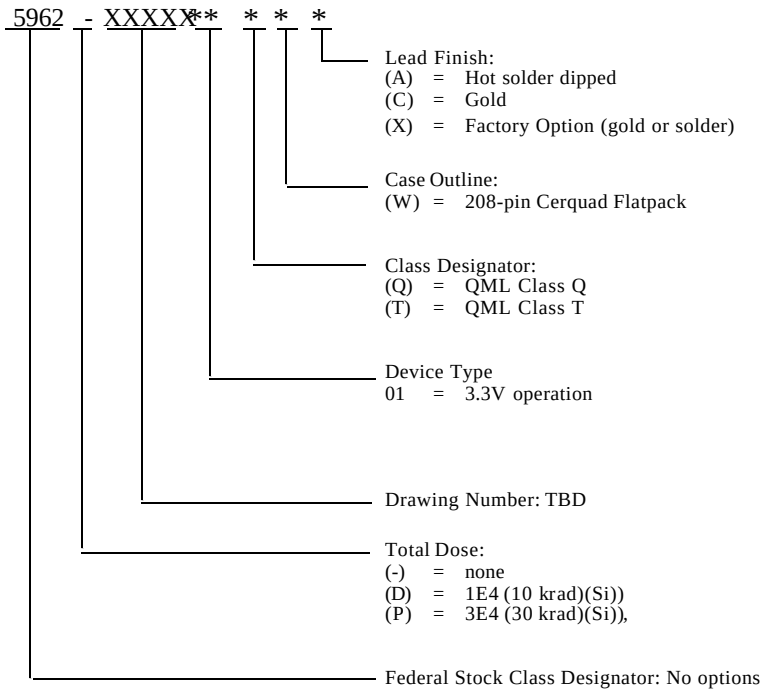


Notes:

1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Prototype flow per UTMC Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY. Radiation neither tested nor guaranteed.
4. Military Temperature Range flow per UTMC Manufacturing Flows Document. Devices are tested at -55°C, room temp, and 125°C. Radiation neither tested nor guaranteed.

IN DEVELOPMENT

UT4090 FPGA: SMD



Notes:

1.Lead finish (A,C, or X) must be specified.

2.If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).

3.Total dose radiation must be specified when ordering. QML Q and QML T not available without radiation hardening.

IN DEVELOPMENT