SME5421MCZ-333
SME5421MCZ-360

December 1998

UltraSPARC™-II*i* CPU Module

DATA SHEET 333 / 360 MHz CPU, 2-MByte E-cache, UPA64S, 66 MHz PCI

FUNCTIONAL DESCRIPTION

The UltraSPARC™-II*i* CPU Module [1] is a high performance, SPARC V9-compliant, small form-factor processor module. It interfaces to the UltraSPARC Port Architecture 64-bit Slave (UPA64S) interconnect bus, main memory, and the primary PCI bus.

The module consists of one UltraSPARC-II*i* CPU, one 64K x 18 cache-tag SRAM, four 256K x 18 cache-data SRAMs, and circuitry for generating clocks for the processor, SRAM, and UPA64S bus interface. PCI clocks are generated externally.

Module components nominally operate at 3.3 V and 2.6 V. All signal levels at the module interface are 3.3 V-LVTTL compatible, excepting both the differential UPA clock outputs, which operate at 3.3 V-PECL levels, and the PCI-interface signals, which are 3.3 V-PCI compatible. JTAG output signals are 2.6 V LVTTL compatible.

The SME5421MCZ-333 module runs at a 333 MHz internal CPU frequency; the SME5421MCZ-360 at 360 MHz. The clock synthesizer sets the frequency and division circuitry operates the UPA frequency at one third of the internal processor-frequency. The module interface uses two high-speed, impedance-controlled connectors: see *Figure 3*.

Features

- High performance UltraSPARC-II*i* CPU
- SPARC V9 compliant
- Implements VIS™ Instruction Set
- 64-bit wide data bus
- 2MB external cache (E-cache or L2-cache) clocked at 180 MHz (167 MHz for 333 MHz part)
- Components operate at 3.3V LVTTL and 2.6V LVTTL
- 66 MHz PCI bus to rev. 2.1 PCI specification
- 130 mm x 100 mm x 45 mm (height) form factor
- JTAG (IEEE 1149) boundary-scan interface
- System interface through two impedance-controlled connectors

Benefits

- 15.2 SPECint95 (est.),19.7 SPECfp95 (est.) at 360 MHz, 2 MB
- Runs applications that conform to the SPARC™ V8 or V9 ABI
- Comprehensive hardware support for 3D graphics, H-261 compression/decompression, and MPEG2 decompression
- Peak bandwidth of up to 475 MB/s (360 MHz CPU)
- UltraSPARC-II*i* CPU Module pipelined E-cache interface delivers high performance of up to 1.43 GB/s (360 MHz CPU)
- Very high bus speeds with power savings that minimize rate of heat generation
- Integrated interface simplifies I/O system design
- Small-footprint, modular construction
- Board-level testability
- High-performance and reliable signal integrity

1. The 360 MHz UltraSPARC-II*i* CPU Module is a recent addition to the UltraSPARC-*i* series. See URL: http://www.sun.com/microelectronics/UltraSPARC/ for other UltraSPARC-*i* series products.

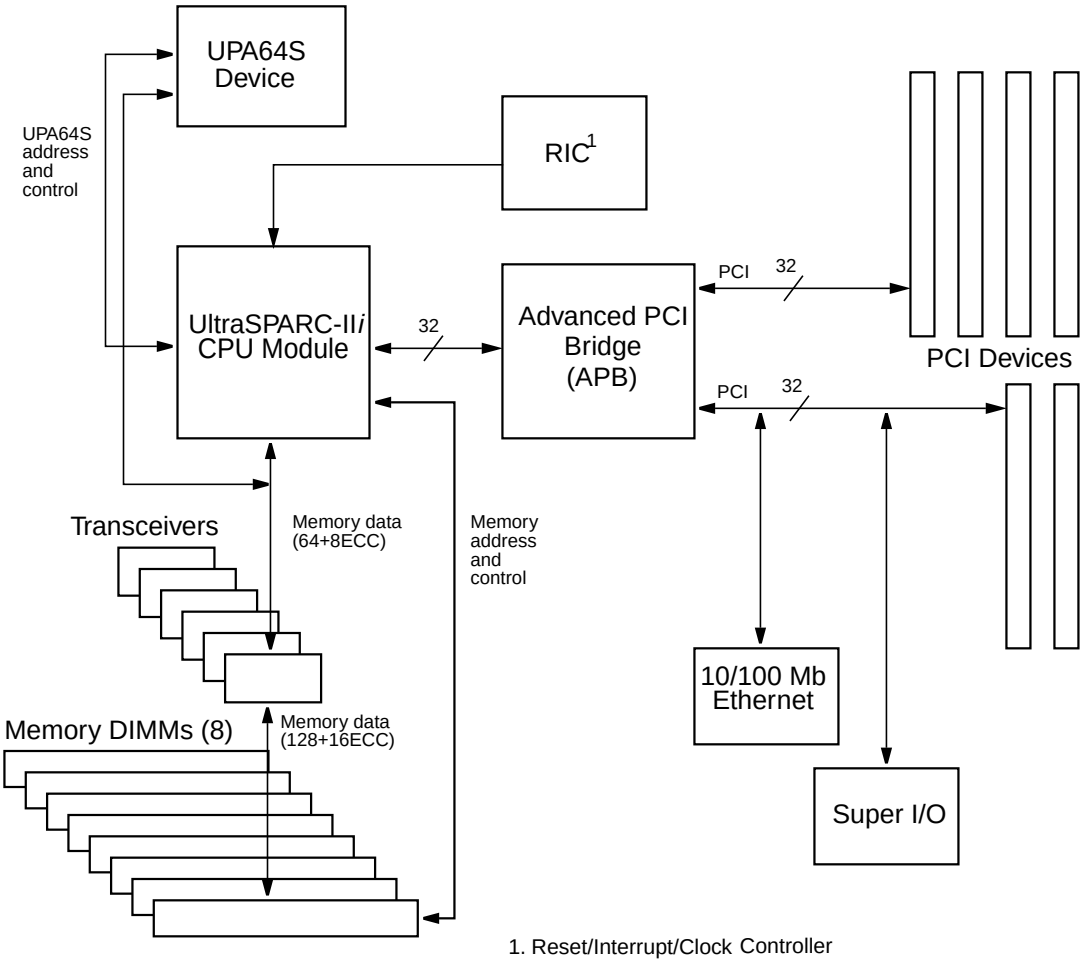


Figure 1. Typical System Block Diagram

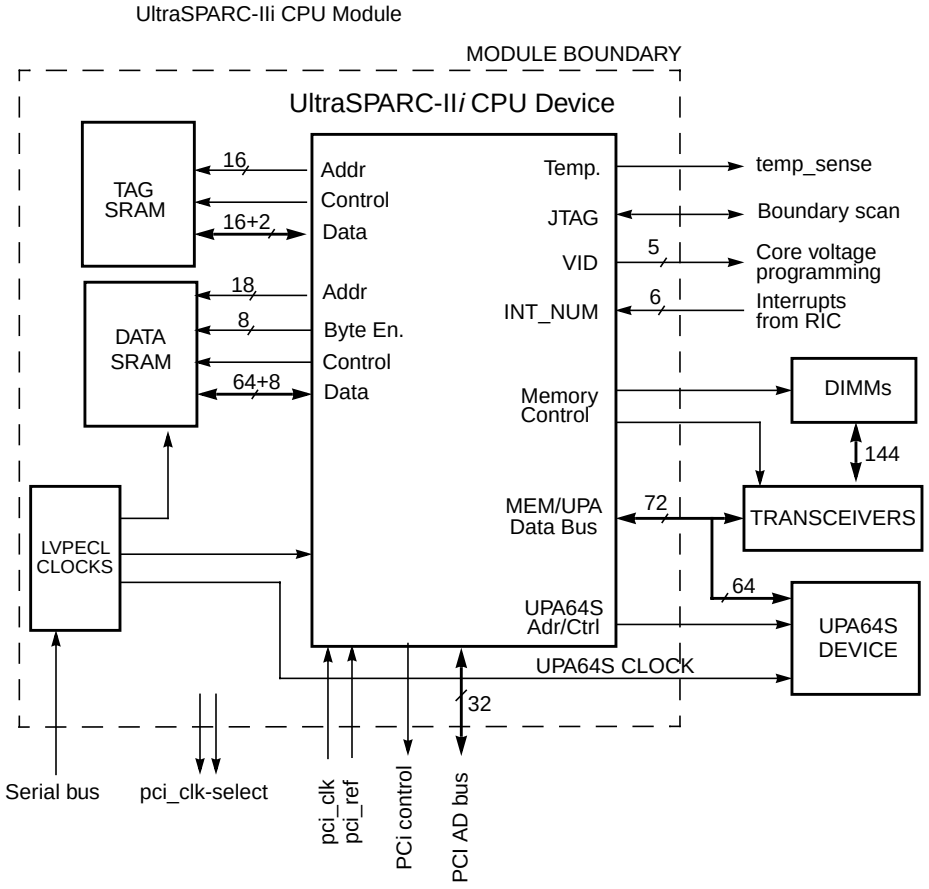


Figure 2. UltraSPARC-II*i* System Block Diagram

Component Overview

The SME5421MCZ-333 and the SME5421MCZ-360 UltraSPARC-II*i* CPU Modules consist of the following components.

- UltraSPARC-II*i* Processor in a ceramic LGA package
- 2-MByte E-cache, made up of four 256K X 18 data SRAM chips and one 64K X 18 tag SRAM
- Clock generator, divider, and buffer ICs
- PCI / JTAG / temperature sense interface connector
- Memory / UPA64S interface connector

UltraSPARC-IIi CPU

The UltraSPARC-II*i* CPU is a high-performance, highly integrated, superscalar CPU implementing the SPARC V9 64-bit RISC architecture. UltraSPARC-II*i* can sustain the execution of up to four instructions per cycle even in the presence of conditional branches and cache misses. It supports a 44-bit virtual address space and a 41-bit physical address space. The instruction set also includes the VIS Instruction Set that accommodates the functions:

- the most common operations related to two-dimensional image processing
- three-dimensional graphics
- video compression and decompression and other pixel-based algorithms
- support for high-bandwidth bcopy through block-load and block-store instructions

The UltraSPARC-II*i* CPU is contained in a 587-pin 1.27 mm pitch ceramic LGA package of dimensions 37.5 mm by 37.5 mm.

The PCI interface supports the PCI 2.1 specification with a 66-MHz clock rate or a 33-MHz rate across a PCI bridge, for example the Advanced PCI Bridge (APB™), part number SME2411BGA-66. PCI DMA transfers become cache coherent after they are presented to the CPU.

External Cache

The 2-MByte E-cache is connected to the E-cache data bus and is implemented in five synchronous register-latch SRAM ICs:

- four 256K x 18 data SRAMs configured on a 64-bit data + 8-bit error-correction code (ECC) interface
- one 64K x 18 cache-tag SRAM

The CPU-SRAM interface runs at half of the CPU pipeline frequency (180 MHz for the 360 MHz CPU, 167 MHz for the 333 MHz CPU). SRAM signals operate at 2.6V, LVTTL levels. The SRAM clock is a differential, LVPECL [1] signal.

Both of the external-cache SRAM interfaces operate in 2–2, register-latch mode, which means that it takes two processor clocks to send the address and access the SRAM array, and two clocks to return the data. The 2–2 mode has a four cycle pin-to-pin latency and provides the highest performance SRAM solution at a given frequency.

The external-cache SRAMs are housed in 119-pin, plastic, 50-mil, BGA packages, measuring 22 mm by 14 mm.

1. Low-Voltage, Positive, Emitter-Coupled Logic

Clock Generation

Motorola LVPECL devices are used to generate clocks for the processor, SRAM, and UPA64S interface. The processor doubles the input LVPECL clock frequency to generate the CPU pipeline frequency of 333 or 360 MHz.

System Functions

The following list gives system functions, with their corresponding CPU-derived clock rates.

- UPA 64S interface: 64-bit; 1/3 CPU pipeline frequency
- On-module E-cache SRAM: 64-bit; runs at 1/2 CPU pipeline frequency
- DRAM data interface: 64 + 8-ECC bits; configured for external multiplexing to 128 + 16-ECC bits at the DRAM interface; programmed by software at an equivalent of 1/4 or 1/5 of the CPU pipeline frequency

The PCI bus clock is generated by the system board and is an input to the module. It is asynchronous with respect to the CPU clock. The PCI bus is 32 bits wide and can run at a maximum frequency of 66 MHz.

External Connector Pin Assignments

This module requires two supply voltages, both driven by external system supplies:

- V_{DD}, nominally 3.3 V, powers the CPU I/O and the SRAM core
- V_{DD_CORE}, nominally 2.6 V, supplies the core of the processor chip and the SRAM I/O on the module

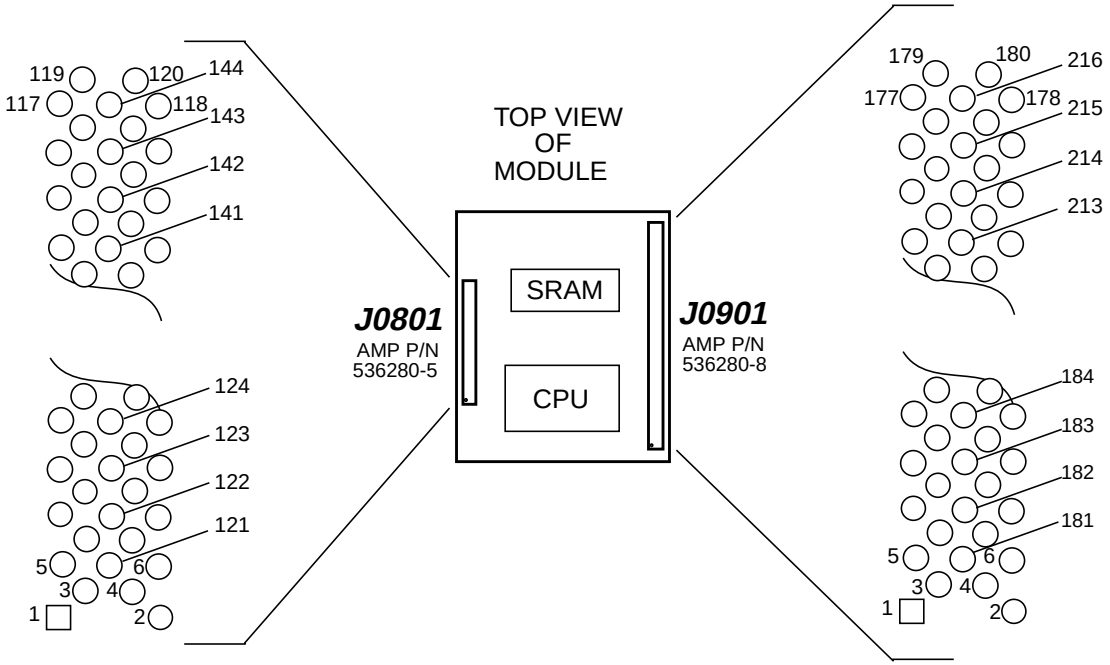


Figure 3. Module Connectors and Pin Assignments

TECHNICAL CAPABILITIES

All performance specifications are for a CPU with a 2-MByte E-cache operating in 2-2 mode.

SPEC Performance

Estimated Performance			Conditions
360 MHz CPU	SPECint95	15.2	peak; using 50 ns DIMMs
	SPECfp95	19.7	
333 MHz CPU	SPECint95	14.2	peak; 60 ns DIMMs
	SPECfp95	16.9	

One of the features of the UltraSPARC-II*i* CPU is the superior performance of its integrated I/O, DRAM and UPA64S interfaces.

Memory Performance

Parameter	Specification		Unit
	360 MHz CPU [1]	333 MHz CPU [2]	
Maximum E-cache read bandwidth	1.44	1.32	Gbyte/sec.
Maximum E-cache write bandwidth	1.44	1.32	Gbyte/sec.
Maximum DRAM random read bandwidth	415	385	Mbyte/sec.
Maximum DRAM random write bandwidth	415	385	Mbyte/sec.
Maximum same page read bandwidth	475	440	Mbyte/sec.
Memcopy, from DRAM to DRAM	360	333	Mbyte/sec.
Memcopy, from DRAM to UPA64S bus (120 MHz)	655	605	Mbyte/sec.

FP Vector

Specification	Sustained Performance		Unit
	360 MHz CPU [1]	333 MHz CPU [2]	
STREAM Copy (compiled)	237	219	Mbyte/sec.
STREAM Scale (compiled)	237	219	Mbyte/sec.
STREAM Add (compiled)	266	246	Mbyte/sec.
STREAM Triad (compiled)	266	231	Mbyte/sec.

1. Using 50 ns DIMMS
2. Using 60 ns DIMMS

Note: DRAM bandwidth is 25%–33% greater than these numbers since there is an initial DRAM read of the data locations that is used for store operations.

PCI Bandwidth

PCI Sustained Bandwidth			
From processor PCI Bus (DMA) to DRAM	66 MHz, 32-bit	Random 64-byte reads	132 Mbyte/sec.
		Random 64-byte writes	151 Mbyte/sec.
From processor PCI Bus (DMA) to E-cache	66 MHz, 32-bit	Random 64-byte reads	163 Mbyte/sec.
		Random 64-byte writes	186 Mbyte/sec.
From processor to processor PCI bus (PIO)	66 MHz, 32-bit	64-byte writes	200 Mbyte/sec.

All sustained DMA numbers are for a single device. Multiple devices on separate secondary buses can cause higher sustained bandwidths. In no case is the combined bandwidth from two secondary buses less than the peak bandwidth available from one bus. This is because of efficient internal arbitration between multiple events in the bus bridge.

UPA64S Bus Bandwidth

UPA PIO Bandwidth				
From the CPU to UPA64S bus (PIO)	360 MHz CPU	120 MHz, 64 bit	Random 64-byte writes	714 Mbyte/sec.
			Compressed 8-byte writes	950 Mbyte/sec.
	333 MHz CPU	111 MHz, 64 bit	Random 64-byte writes	660 Mbyte/sec.
			Compressed 8-byte writes	880 Mbyte/sec.

PCI Bandwidth with APB™ (33MHz Secondary Bus)

PCI Secondary Sustained Bandwidth			
From the processor, to the secondary PCI Bus (PIO)	33 MHz, 32-bit	64-byte writes	124 Mbyte/sec.
From the secondary PCI bus (DMA) to the DRAM	33 MHz, 32-bit	Random 64-byte reads	78 Mbyte/sec.
		Random 64-byte writes	124 Mbyte/sec.

SIGNAL DESCRIPTIONS

Clock Interface

Symbol	Type [1]	Name and Function
UPA_CLK_POS, UPA_CLK_NEG	O PECL	Differential 3.3V, low-voltage PECL clock supplied to the UPA64S interface
PCI_REF_CLK	I	PCI reference clock; should be 66 MHz. But this can be 33 MHz if a 33 MHz PCI interface is required
PCI_CLK	I	PCI clock; 66 MHz - doubled internally to 133 MHz for use in internal PCI logic

1. KEY: O – output; I – input; I/O – input or output; PECL – Positive Emitter Coupled Logic

JTAG/Test Interface

Symbol	Type	Name and Function
TDO	O	IEEE 1149 test data output; 2.6 V LV CMOS-compatible tri-state signal driven only when the TAP controller is in the shift-DR state
TDI	I	3.3 V IEEE 1149 test data input; pin is internally pulled to logic one when not driven
TCK	I	3.3 V IEEE 1149 test clock input; pin must always be driven to logical 1 or logical 0 if not tied to a clock source
TMS	I	3.3 V IEEE 1149 test mode select input; internally pulled to logic one when not driven
TRST_L	I	3.3 V IEEE 1149 test reset input (active low); internally pulled to logical one when not driven
TEMP_SENSE[1:0]	O	Temperature sensing thermistor terminals on the module
MFG_L	I	For manufacturing test use

Initialization Interface

Symbol	Type	Name and Function
PO_RST_L	I	For non power-on resets; for debug; asynchronous assertion and de-assertion; active low
S_DATA	I	Serial frequency-setting data for MC12430 module clock synthesizer
S_CLK	I	Data clock for module clock synthesizer
S_LOAD	I	Serial load mode pin for clock synthesizer
X_RESET_L	I	Driven to signal XIR traps; for debug; behaves as a non-maskeable interrupt; asynchronous assertion and de-assertion; active low
SYS_RESET_L	I	Driven for POR (power-on) resets; asynchronous assertion and de-assertion; active low
PCI_RESET_L	O	Resets PCI subsystem; asynchronous assertion and monotonic deassertion; also used for UPA64S device reset
PCI_CLKSEL[1:0]	O	Selects PCI clock frequency generated on external system board; see page 13

PCI interface

Symbol	Type	Name and Function
PPCI_AD[31:0]	I/O	Address and data bits are multiplexed on these PCI pins
PPCI_CBE_L[3:0]	I/O	Bus command and byte enables are multiplexed on these PCI pins
PPCI_PAR	I/O	Parity: even parity generated across AD[31:0] and CBE_L[3:0]
PPCI_DEVSEL_L	STS [1]	Device Select: indicates the driving device has decoded its address as the target of the current access: as input, indicates whether any device has been selected
PPCI_FRAME_L	STS	Cycle Frame: driven by current master to indicate beginning and end of an access
PPCI_REQ_L[3:0]	I	Request: indicates to arbiter that an external device requires use of the bus
PPCI_GNT_L[3:0]	T/S [2]	Grant: indicates to device that access to the bus has been granted
PPCI_IRDY_L	STS	Initiator Ready: indicates the bus master's ability to complete the current data phase
PPCI_TRDY_L	STS	Target Ready: indicates the selected device's ability to complete the current data phase.
PPCI_PERR_L	O/D [3]	Parity error: reports data parity errors
PPCI_SERR_L	O/D	System Error: reports address parity errors, data parity errors on special cycles, or any other catastrophic PCI errors
PPCI_STOP_L	STS	Stop: indicates that current target is requesting that the master stop the current transaction

1. Sustained tri-state, bidirectional; only one driver at a time; must drive high for one cycle before letting the line float. External pullups maintain the high voltage level between drives and are needed on the system board.

2. Tri-state output.

3. Open drain as STS, but allows multiple devices to be wire-ORd. A pullup is required to sustain the inactive state, and should be implemented on the system board.

Interrupt Interface

Symbol	Type	Name and Function
SB_DRAIN	O	Store Buffer Drain; asserted after Interrupts or by software to cause outstanding DMA writes to be flushed from buffers
SB_EMPTY[1:0]	I	Store Buffer Empty; asserted when external SIMBA PCI bus bridge has guaranteed that all DMA writes queued before the assertion of SB_DRAIN have left the bus bridge
INT_NUM[5:0]	I	Interrupt Number; sampled at 66 MHz PCI clock rate; encoded Interrupt request

Memory and Transceivers Interface

Symbol	Type	Name and Function
MEM_WE_L	O	Memory Write Enable: active low
MEM_CAS_L[1:0]	O	Memory Column Address Strobe: active low
MEM_RAST_L[3:0]	O	Memory Row Address Strobe, Top: active low
MEM_RASB_L[3:0]	O	Memory Row Address Strobe, Bottom: active low
SYS_DAT[63:0]	I/O	Memory / UPA64S Data
MEM_ECC[7:0]	I/O	Memory ECC bits

Memory and Transceivers Interface (Continued)

Symbol	Type	Name and Function
MEM_ADDR[12:0]	O	Memory Address: (row and column)
XCVR_OEA_L	O	Transceiver Output Enable A: active low
XCVR_OEB_L	O	Transceiver Output Enable B: active low
XCVR_SEL_L	O	Transceiver Select; Active low: picks high or low half of read data
XCVR_WR_CNTL[1:0]	O	Transceiver Write Control: Controls lock enables on internal registers
XCVR_RD_CNTL[1:0]	O	Transceiver Read Control: control clock enables on internal registers
XCVR_CLK[2:0]	O	Transceiver Clock: all data and control signals are registered by these clocks; multiple outputs to minimize loading effects of six transceivers; should be parallel terminated to GND on the system board

Quick Pin Reference - UPA64S Interface

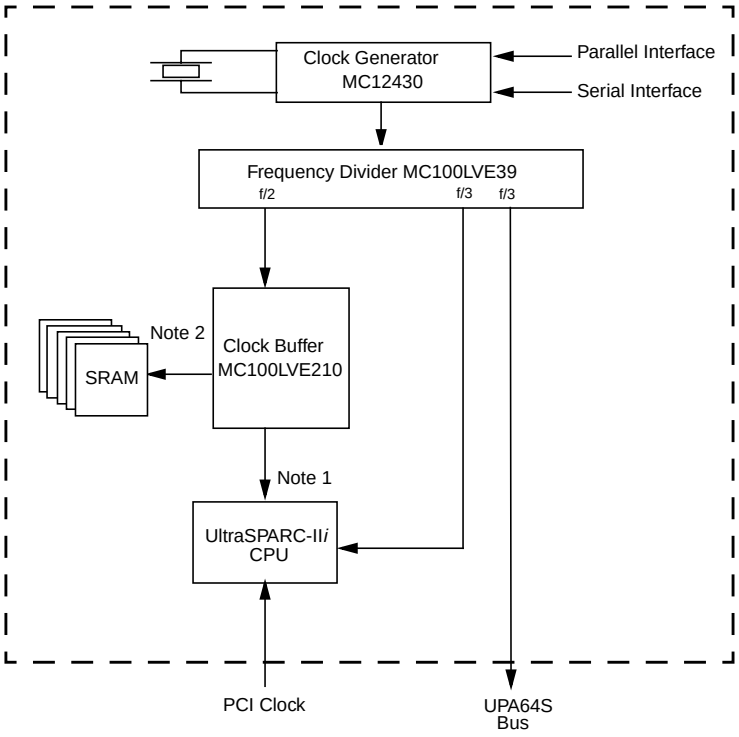
Symbol	Type	Name and Function
S_REPLY[2:0]	O	S Reply: encoded command that indicates arrival of write data on MEM_DATA[63:0], or command to drive MEM_DATA[63:0] with read data
P_REPLY[1:0]	I	P Reply: Encoded command that indicates consumption of prior write, or ability to provide read data
SYSADR[28:0]	O	System Address: sends two cycle-address packets to the UPA64S slave, or provides internal state debug information
ADR_VLD	O	Address Valid: asserted during first cycle of two cycle address packet

CLOCK DISTRIBUTION

A high-frequency clock signal is generated within the module using a Motorola MC12430 high frequency PLL clock generator from a 16MHz series resonant crystal. The clocks are differential Low Voltage Positive ECL (LVPECL). The MC12430 provides a serial and parallel interface for setting the frequency. The parallel interface pins are hardwired on the module and their state is loaded during reset. The serial interface signals S_LOAD, S_DATA, and S_CLOCK are brought out to the Memory / UPA64S external connector to allow frequency setting from the system board.

The high-frequency clock from the clock generator is divided down by a MC100LVEL39 clock divider to produce the processor and UPA64S clock signals. Only the UPA64S LV PECL clock signal (at 1 / 3 of the CPU clock frequency) is a module output. It appears on the 180-pin Memory / UPA64S external connector.

An MC100LVE210 clock buffer distributes the CPU and SRAM clock signals. *Figure 4* shows a schematic diagram of the module clock distribution.



Note 1: The CPU's PLL doubles the incoming frequency
Note 2: Multiple LVPECL pins connect to the SRAMs

Figure 4. Module Clock Distribution

The JTAG TCLK signal enters the module via the 120-pin PCI / JTAG / Temperature Sense connector and connects to the SRAMs and the UltraSPARC-II*i* processor.

Incoming system board PCI_CLK and the PCI_REF_CLK signals also arrive at the PCI / JTAG / Temperature Sense interface connector and travel to the UltraSPARC-II*i* CPU.

The UltraSPARC-II*i* CPU Module can select system board PCI clock generator frequency values to be in either the 66 MHz / 33 MHz or the 60 MHz / 30 MHz sets. PCI / Misc connector signals PCI_CLKSEL0 and PCI_CLKSEL1 provide frequency-encoding bits that conform to IC Works' CPU / PCI System Clock Generator (Part Number W48C60-422) specification. This PCI clock generator is located on the system board. The table: "PCI Frequency Selection" shows the frequency encoding.

PCI Frequency Selection

PCI_CLKSEL0	PCI_CLKSEL1	PCI MODE
0	1	60/30 MHz
1	0	66/33 MHz

SPECIFICATIONS

Absolute Maximum Ratings [1] [2]

Symbol	Parameter	Conditions	Rating	Units
V_{DD}	Supply voltage range for I/O	-	0 to 3.8	V
V_{DD_CORE}	Supply voltage range for CPU core	-	0 to 2.7 [3]	V
V_I	Input voltage range	-	V_{ss} - 0.5 < V_I < V_{DD} +0.5	V
V_O	Output voltage range	-	V_{ss} - 0.5 < V_O < V_{DD} +0.5	V
I_{IK}	Input clamp current	V_I < 0 - 0.5V or V_I > V_{DD} + 0.5V	20	mA
I_{OK}	Output clamp current	V_I < 0 - 0.5V or V_I > V_{DD} + 0.5V	±50	mA
I_{OL}	Current into any output in the low state	-	50	mA
-	Shock [4]	in any axis	15	g
-	Vibration [4]	peak value in any axis and within spectral range 5 ≤ f ≤ 500 Hz	0.25	g

1. Operation of the device at values exceeding those listed may result in degradation or destruction of the device. Functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. Unless otherwise noted, all voltages are with respect to V_{SS}.
3. At all times: $V_{DD\_CORE} \leq V_{DD}$ + 0.5 V
4. These specifications are for the module assembly alone and do not apply to the module connectors when installed in a system board. Sun uses an attachment device for the module in such an installation.

Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Supply voltage for I/O		3.14	3.3	3.46	V
V_{DD_CORE}	Supply voltage for the CPU core		2.52	2.6	2.68	V
I_{OH}	High-level output current		-	-	-4.0	mA
I_{OL}	Low-level output current		-	-	8.0	mA
T_J	Operating junction temperature		-	-	see notes[1][2]	°C
T_A	Operating ambient temperature		0	-		°C
-	Airflow over heatsink (333 MHz and 360 MHz CPU)	At 30 °C ambient and sea-level altitude	-	150		ft./m.
		At 40 °C ambient and 10,000 ft. altitude	-	300		ft./m.

1. Maximum allowable ambient temperature depends upon air flow rate and must be chosen so that the maximum junction temperature T_J is not exceeded. See "Thermal Considerations" on page 20.
2. For storage specifications, see "Storage and Shipping Environmental Specification" on page 30

DC Characteristics

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{OH}	High-level output voltage	2.6V signals	V_{DD} = Min, I_{OH} = Max	2.4	-	-	V
		3.3V non-PCI signals		2.4	-	-	V
		3.3V PCI signals	Iout = -500 µA	$0.9V_{DD}$	-	-	V
V_{OL}	Low-level output voltage	2.6V signals	V_{DD} = Min, I_{OL} = Max	-	-	0.4	V
		3.3V non-PCI signals		-	-	0.4	V
		3.3V PCI signals	Iout = 1500 µA	-	-	$0.1V_{DD}$	V
V_{IH}	High-level input voltage	2.6V signals	V_{DD_CORE} = Max	1.65	-	-	V
		PECL signals		-	V_{DD}- 0.7	-	V
		3.3V non-PCI signals	V_{DD} = Max	2.0	-	-	V
		3.3V PCI signals		$0.5V_{DD}$	-	V_{DD}+ 0.5	V
V_{IL}	Low-level input voltage	2.6V signals	V_{DD_CORE} = Min	-	-	1.15	V
		PECL signals			V_{DD}-1.4		V
		3.3V non-PCI signals	V_{DD} = Min	-	-	0.8	V
		3.3V PCI signals		- 0.5	-	$0.3V_{DD}$	V
I_{DD}	supply current for V_{DD}	360 MHz	V_{DD} = 3.3 V	-	4.8	5.8	A
		333 MHz		-	4.5	5.5	A
I_{DD_CORE}	Supply current for V_{DD_CORE}	360 MHz	V_{DD_CORE} = 2.6 V	-	8.3	10.0	A
		333 MHz		-	7.8	9.4	A
I_{OZ}	High-impedance output current		V_{DD} = Max, V_O = 2.4 V	-	-	20	µA
			V_{DD} = Max, V_O = 0.4 V	-	-	-20	µA
I_I	Input current (inputs without pullups)		V_{DD} = Max; V_I = V_{SS} to V_{DD}	-	-	20	µA
	Input current (inputs with pullups [1])		V_{DD} = Max; V_I = V_{SS} to V_{DD}	-	-	250	µA

1. See "JTAG/Test Interface" on page 9 for description of which inputs are attached to pullups.

POWER REQUIREMENTS

The UltraSPARC-II*i* CPU module requires two V_{DD} supply voltages, V_{DD} and V_{CC_CORE}, nominally at 3.3 V and 2.6 V respectively. These supplies pass to the module through connector blades on both 120 pin and 180 pin connectors. The V_{DD_CORE} supplied by the system board is programmable from the module through resistor stuffing options driving the VID[4:0] bits in accordance with *Table 2* on page 22.

Estimated maximum power consumption is 45 W for the 360 MHz module and 42 W for the 333 MHz module. This consumption value includes the power taken by the CPU and SRAMs.

Core Voltage Encoding

Module Pins					VDD_CORE	Module Pins					VDD_CORE
VID4	VID3	VID2	VID1	VID0	V (DC)	VID4	VID3	VID2	VID1	VID0	V(DC)
0	1	1	1	1	1.30	1	1	1	1	1	No CPU Module
0	1	1	1	0	1.35	1	1	1	1	0	2.1
0	1	1	0	1	1.40	1	1	1	0	1	2.2
0	1	1	0	0	1.45	1	1	1	0	0	2.3
0	1	0	1	1	1.50	1	1	0	1	1	2.4
0	1	0	1	0	1.55	1	1	0	1	0	2.5
0	1	0	0	1	1.60	1	1	0	0	1	2.6
0	1	0	0	0	1.65	1	1	0	0	0	2.7
0	0	1	1	1	1.70	1	0	1	1	1	2.8
0	0	1	1	0	1.75	1	0	1	1	0	2.9
0	0	1	0	1	1.80	1	0	1	0	1	3.0
0	0	1	0	0	1.85	1	0	1	0	0	3.10
0	0	0	1	1	1.90	1	0	0	1	1	3.20
0	0	0	1	0	1.95	1	0	0	1	0	3.30
0	0	0	0	1	2.00	1	0	0	0	1	3.40
0	0	0	0	0	2.05	1	0	0	0	0	3.50

TIMING SPECIFICATIONS

Timing design within the module makes demands upon signal timing at the module connectors. This section describes internal module timing when it is useful to explain external requirements. For detailed information on timing and latencies see Sun publications:

- "UltraSPARC–II*i* Highly Integrated RISC Processor, PCI Interface." Data Sheet, SME1040CGA [1]
- "UltraSPARC–II*i* User's Manual," SME1040CGA [2]

PCI

PCI_CLK and PCI_REF_CLK traces on the module are matched in length to within 0.5 in. trace length, or 100 ps at a nominal length corresponding to 550 ps. These signals have no added delay and their trace lengths are also within ± 0.5 in. of those of the other PCI signals. Setup, hold and propagation times are listed in the UltraSPARC-II*i* component Data Sheet, SME1040 [1]

DRAM

DRAM signals are all matched to within 0.5 in. trace length on the module.

1. Document Part Number: 805-0086-03
2. Document Part Number: 805-0087-01

SRAM

UltraSPARC-II*i*'s E-cache, or second level (L2) cache, is implemented using external synchronous SRAMs on a bus with 64 data bits and 8 parity bits, as well as using a tag SRAM on a 16-bit bus that includes two parity bits. While the tag and data SRAM busses share no signals, the tag implements the same timing scheme as the data SRAM bus for a given module.

UPA

Within the module design, the following sets of clock signals need to be concurrent:

- UltraSPARC-II*i* SRAM_CLK
- UltraSPARC-II*i* UPA_CLK
- UPA_CLK input to the fast-frame-buffer ASIC external to the module
- CPU_CLK input to the UltraSPARC-II*i* processor

Any timing mismatches between the UPA_CLK and the CPU_CLK linearly degrades the timing margin to and from the UltraSPARC-II*i* and the UPA64S device, for example the FFB.

Since the CPU_CLK signal is completely contained in the module, once a delay is designed into this module, system board implementations must match that delay value in the UPA_CLK signal or lose margin by the amount of the mismatch. Note that UPA_CLK is a convenient reference to the differential signal carried by lines: UPA_CLK_POS and UPA_CLK_NEG; see "Signal Descriptions" on page 9.

Even if traces are perfectly matched, a number of factors cause accumulation of clock skew between the on-board CPU clock and the UPA_CLK signals—as driven off module. These factors include:

- Separate buffers on the module: ± 200 ps
- UltraSPARC-II*i* and FFB sockets: ± 50 ps
- Board fabrication variance: ± 250 ps
- Setup / hold / clock input to data-output delay differences: ± 150 ps
- System noise: ± 150 ps

When doing a system timing budget, this total skew must be added to the setup, hold, and propagation times listed for UPA and DRAM signals in the UltraSPARC-II*i* CPU component data sheet SME1040CGA [1].

The UPA bus on the module is designed for 6 in. of system board trace plus 3.4 in. of FFB trace, plus simulated differences in ASIC / UltraSPARC-II*i* CPU setup times. These are internal ≈ 180 ps / in. traces**.**

1. Document Part Number: 805-0086-03

MECHANICAL SPECIFICATIONS

The UltraSPARC-IIi CPU module is characterized by:

- Dimensions: 100 mm x 130 mm x 45 mm (height)
- Heat Sink: Aluminum pin fin
- Connectors: AMP part number 536280-5 and AMP part number 536280-8

Figure 5 illustrates the module.

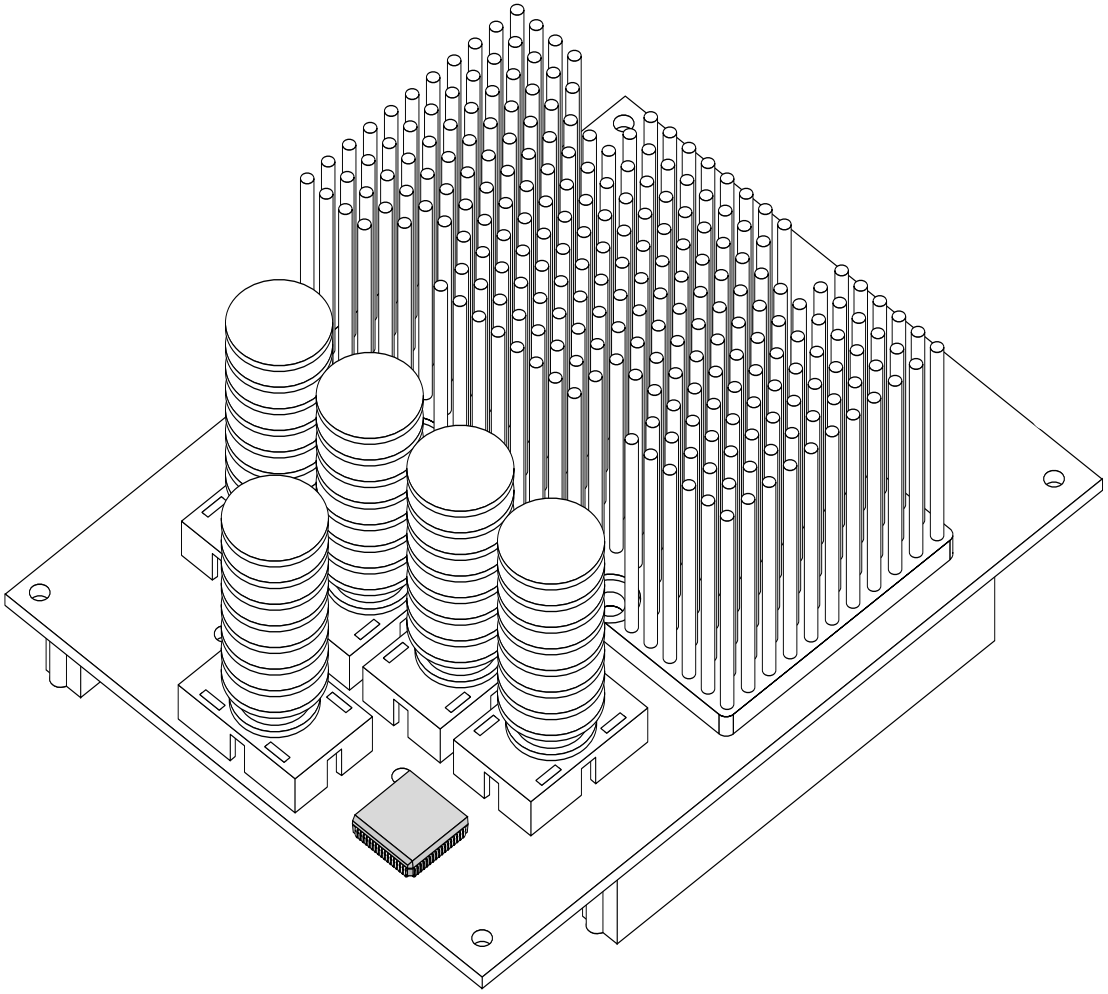


Figure 5. Module Assembly

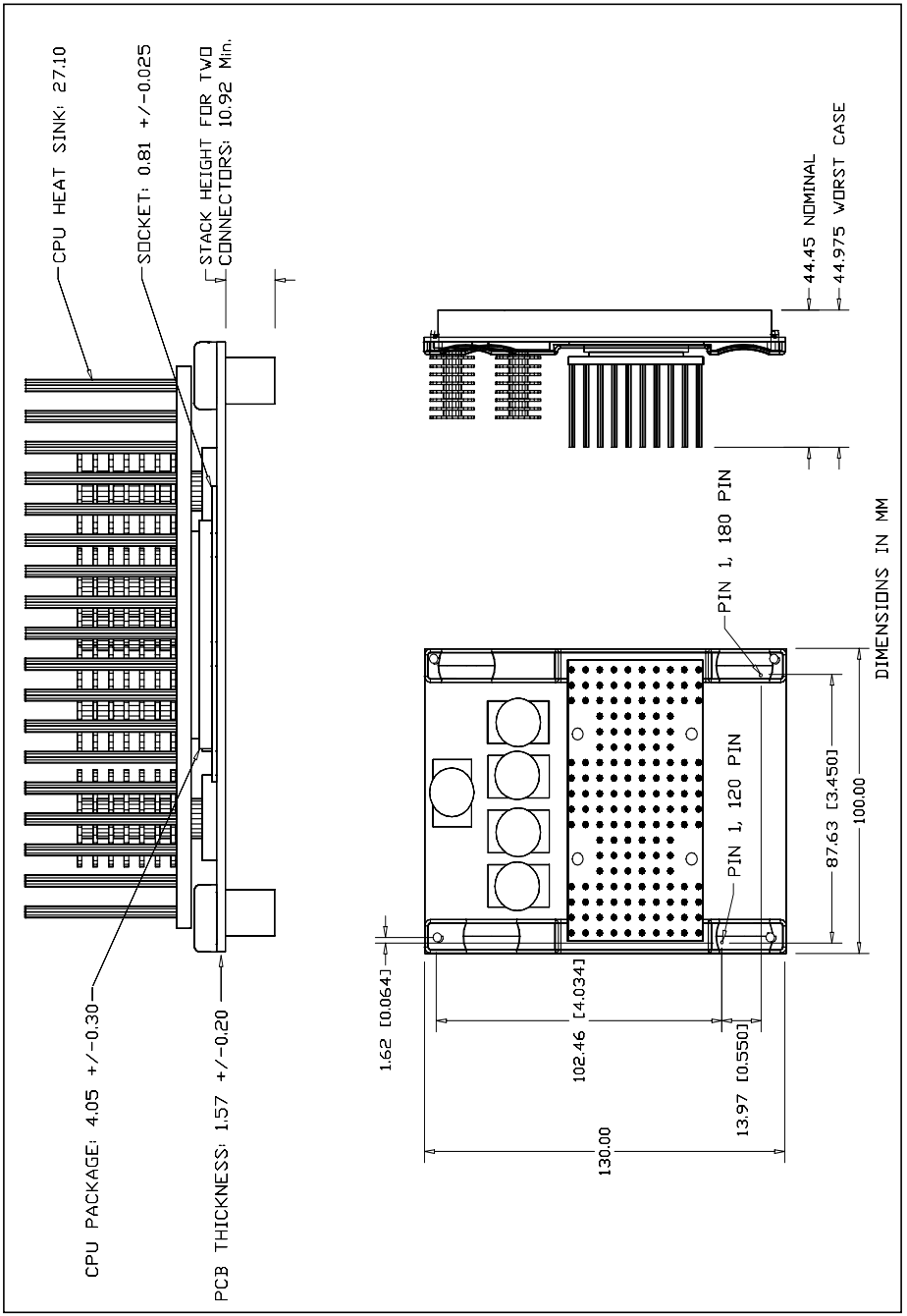


Figure 6. Module Dimensions

THERMAL CONSIDERATIONS

The CPU device's operating frequency and I/O timing is affected by its junction temperature (Tj). Airflow must be directed to the CPU heatsink to keep the CPU cool. Correct airflow maintains the junction temperature within its operating range. The airflow directed to the CPU is usually sufficient to keep the surrounding devices on the module cool, including the SRAMs and clock circuitry.

The CPU temperature specification is provided in terms of CPU junction temperature. It is related to the case temperature by the thermal resistance of the package and the CPU power dissipation.

The case temperature can be measured directly by a thermocouple probe to verify that the CPU junction temperature is correctly maintained over the entire operating range of the system. This determination can include factoring for load and environmental conditions. In some cases it is possible to measure the heatsink temperature and calculate the junction temperature. Both methods of calculating the junction temperature are presented below.

Table 1 specifies the terms, definitions, and specifications used to calculate thermal specifications for the UltraSPARC-II*i* CPU device.

TABLE 1: Thermal Definitions and Specifications

Term	Definition	Specification	Comments
Tj	Device junction temperature	105 °C [1]	Maximum value—a lower value is preferred; cannot be measured directly; must always be calculated
Tc	Case temperature		Measurable at the top-center of the device; requires a hole in the base of the heatsink to allow the thermocouple to contact the case
Ts	Heatsink temperature		Measurable as the temperature of the base of the heatsink; The best approach is to embed a thermocouple in a cavity drilled in the heatsink base. An alternative is to place the thermocouple between the fins/pins of the heatsink (insulated from the airflow) and in contact with the base plate of the heatsink
Ta	Module ambient air temperature		Air temperature adjacent to the heatsink
Pd	Typical dissipation of the CPU	25/24 W	For the UltraSPARC–IIi 360/333 MHz CPU
θjc	Junction-to-case thermal resistance of the package	0.5 °C/W	Approximate value for the UltraSPARC-II*i* CPU
θcs	Case-to-heatsink thermal resistance	0.1 °C/W	Approximate value when good thermal grease contact is made between the package and the heatsink
θsa	Heatsink-to-air thermal resistance	See page 22	Value is dependent on the heatsink design, the airflow direction, and the airflow velocity; see *Table 2*
Airflow	Free stream airflow		Unchanneled airflow velocity approaching the heatsink

1. A junction temperature of 105 °C translates into a 90 °C heatsink temperature, corresponding to approximately 150 fpm. airflow at 38.5 °C

Two Step Approach to the Thermal Design:

Step One determines the air flow requirements based on the CPU power dissipation and the thermal characteristics of the CPU package and the surrounding heatsink assembly. The specifications for the heatsink are provided in the table "Heatsink-to-Air Thermal Resistance" "Heatsink-to-Air Thermal Resistance" on page 22.

Step Two verifies cooling effectiveness by measuring the heatsink or case temperature and calculating the junction temperature. The junction temperature must not exceed the CPU specification. In addition, the lower the junction temperature, the higher the system reliability. The CPU temperature must be calculated for a range of loads and environmental conditions, using one of the temperature measuring methods described in the following sections.

Temperature Estimating and Measuring Methods

The following methods can be used to measure the case temperature of the module and to estimate the airflow required to cool it.

Case Temperature Method

The relationship between case temperature and junction temperature is described in the following thermal equation.

If Tc is known, then Tj can be calculated:

$$Tj = Tc + (Pd \times \theta jc)$$

There is good tracking between the case temperature and the heatsink temperature.

Heatsink Temperature Method (Preferred Method)

Measuring the heatsink temperature is sometimes easier than measuring the case temperature. This method provides accurate results for most designs. If the heatsink temperature (Ts) is known then the following thermal equation can be used to estimate the junction temperature.

$$Tj = Ts + [Pd (\theta jc + \theta cs)]$$

Airflow Cooling Estimate Method

The relationship between air temperature and junction temperature is described in the thermal equation:

$$Tj = Ta + [Pd (\theta jc + \theta cs + \theta sa)]$$

Determination of the ambient air temperature (Ta) and the “free-stream” air velocity is required in order to apply the airflow method. The table:"Heatsink-to-Air Thermal Resistance" on page 22 uses the air velocity direction relative to the heatsink orientation to find the thermal resistance between the heatsink and air (θsa).

Note that the airflow velocity can be measured using a velocity meter. Alternatively, it may be determined by knowing the performance of the fan that is supplying the airflow. Calculating the airflow velocity is difficult. It is subject to the interpretation of the term “free-stream.”

Note: Use the Airflow Cooling Estimate method only when an approximate result suffices. Accuracy can only be assured using the Case Temperature method or the Heatsink Temperature method. Apply these methods for the greatest accuracy.

"Heatsink-to-Air Thermal Resistance" specifies the thermal resistance of the heatsink as a function of the air velocity. Notice that the airflow direction also affects the performance of the heatsink.

TABLE 2: Heatsink-to-Air Thermal Resistance

Air Velocity (ft./min) [1]	150	200	300	400	500	650	800	1000
θ_{SA} (°C/W) [2]	1.48	1.21	0.97	0.80	0.71	0.63	0.58	0.55
θ_{SA} (°C/W) [3]	2.06	1.75	1.42	1.13	0.98	0.85	0.76	0.71

1. Free-stream air velocity at sea level
2. Airflow direction parallel to the shorter axis of the pin-fin heat sink (1.9"L x 3.6"W x 1.1"H)
3. Airflow parallel to the longer axis of the heat sink base

COOLING AIRFLOW

These specifications are recommended for a reference configuration:

150 linear feet per minute (LFM) @ 30 °C ambient up to 2000 feet. altitude, maximum

300 LFM @ 40 °C ambient up to 10,000 feet, altitude, maximum

TESTABILITY INTERFACE (JTAG)

These UltraSPARC-II*i* CPU modules implement the IEEE 1149.1 standard to aid board level testing. Boundary Scan Description Language (BSDL) is available for the device.

AC Characteristics - JTAG Timing (estimated values)

Symbol	Parameter	Signals	Conditions	360 or 333 MHz			Units
				Min	Typ	Max	
t_W ($\overline{TRST}$)	Test reset pulse width	$\overline{TRST}$[1]		5	–	–	ns
t_{SU} (TDI)	Input setup time to TCK	TDI		–	3	–	ns
t_{SU} (TMS)	Input setup time to TCK	TMS		–	4	–	ns
t_H(TDI)	Input hold time to TCK	TDI		–	1.5	–	ns
t_H(TMS)	Input hold time to TCK	TMS		–	1.5	–	ns
t_{PD}(TDO)	Output delay from TCK [2]	TDO	I_{OL} = 8 mA I_{OH} = -4 mA	–	6	–	ns
t_{OH}(TDO)	Output hold time from TCK [2]	TDO	C_L = 35 pF V_{LOAD} = 1.5V	3	–	–	ns

1. $\overline{TRST}$ is an asynchronous reset.
2. TDO is referenced from falling edge of TCK.

JTAG Timing

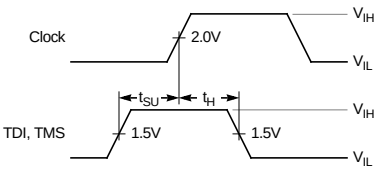


Figure 7. Voltage Waveforms - Setup and Hold Times

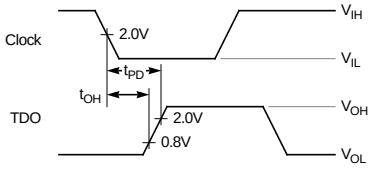


Figure 8. Voltage Waveforms - Propagation Delay Times

MODULE CONNECTOR PIN ASSIGNMENTS

The following list specifies external-interface connector J0901 pin assignments for the Memory / UPA64S signals.

J0901 Memory/UPA64S Interface Connector Pin Assignments

Pin#	Signal Name	Pin #	Signal Name
1	VID0	2	VID1
3	VID2	4	VID3
5	SPARE	6	VID4
7	GND	8	MFG_L
9	XCVR_CLK0	10	GND
11	GND	12	XCVR_CLK1
13	XCVR_CLK2	14	GND
15	GND	16	XCVR_RD_CNTL_0
17	XCVR_OEA_L	18	XCVR_SEL_L
19	XCVR_OEB_L	20	XCVR_RD_CNTL_1
21	XCVR_WR_CNTL_0	22	XCVR_WR_CNTL_1
23	SPARE	24	GND
25	GND	26	MEM_ADR2
27	MEM_ADR0	28	MEM_ADR3
29	MEM_ADR1	30	MEM_ADR6
31	MEM_ADR4	32	MEM_ADR8
33	MEM_ADR5	34	MEM_ADR9
35	MEM_ADR7	36	MEM_ADR10
37	MEM_ADR11	38	MEM_ADR12
39	GND	40	GND
41	SYS_DAT0	42	SYS_DAT2
43	SYS_DAT1	44	SYS_DAT4
45	SYS_DAT3	46	SYS_DAT6
47	SYS_DAT5	48	SYS_DAT8
49	SYS_DAT7	50	SYS_DAT10
51	SYS_DAT9	52	SYS_DAT12
53	SYS_DAT11	54	SYS_DAT14
55	SYS_DAT13	56	SYS_DAT16
57	SYS_DAT15	58	SYS_DAT18
59	SYS_DAT17	60	SYS_DAT20
61	SYS_DAT19	62	SYS_DAT22
63	SYS_DAT21	64	SYS_DAT24

J0901 Memory/UPA64S Interface Connector Pin Assignments (Continued)

Pin#	Signal Name	Pin #	Signal Name
65	SYS_DAT23	66	SYS_DAT26
67	SYS_DAT25	68	SYS_DAT28
69	SYS_DAT27	70	SYS_DAT30
71	SYS_DAT29	72	SYS_DAT32
73	SYS_DAT31	74	SYS_DAT34
75	SYS_DAT33	76	SYS_DAT36
77	SYS_DAT35	78	SYS_DAT37
79	GND	80	SPARE
81	SPARE	82	VDD
83	MEM_WR_L	84	MEM_RAST_L1
85	MEM_CAS_L0	86	MEM_CAS_L1
87	MEM_RAST_L0	88	MEM_RAST_L2
89	MEM_RAST_L3	90	MEM_RASB_L0
91	MEM_RASB_L1	92	MEM_RASB_L2
93	MEM_RASB_L3	94	GND
95	VDD	96	SYS_DAT38
97	SYS_DAT39	98	SYS_DAT40
99	SYS_DAT41	100	SYS_DAT42
101	SYS_DAT43	102	SYS_DAT44
103	GND	104	SYS_DAT46
105	SYS_DAT45	106	SYS_DAT48
107	SYS_DAT47	108	SYS_DAT50
109	SYS_DAT49	110	SYS_DAT52
111	SYS_DAT51	112	GND
113	SYS_DAT53	114	SYS_DAT54
115	SYS_DAT55	116	SYS_DAT56
117	SYS_DAT57	118	SYS_DAT58
119	SYS_DAT59	120	SYS_DAT60
121	SYS_DAT61	122	SYS_DAT62
123	SYS_DAT63	124	MEM_ECC0
125	MEM_ECC1	126	MEM_ECC2
127	MEM_ECC3	128	MEM_ECC4
129	MEM_ECC5	130	MEM_ECC6
131	SPARE	132	MEM_ECC7
133	SYSADR14	134	VDD
135	SYSADR13	136	SYSADR28

J0901 Memory/UPA64S Interface Connector Pin Assignments (Continued)

Pin#	Signal Name	Pin #	Signal Name
137	SYSADR12	138	SYSADR27
139	SYSADR11	140	SYSADR26
141	SYSADR10	142	SYSADR25
143	SYSADR09	144	SYSADR24
145	SYSADR08	146	SYSADR23
147	SYSADR07	148	SYSADR22
149	SYSADR06	150	SYSADR21
151	SYSADR05	152	SYSADR20
153	SYSADR04	154	SYSADR19
155	SYSADR03	156	SYSADR18
157	SYSADR02	158	SYSADR17
159	SYSADR01	160	SYSADR16
161	SYSADR00	162	SYSADR15
163	GND	164	VDD
165	UPA_CLK_POS	166	SPARE
167	UPA_CLK_NEG	168	S_DATA
169	GND	170	GND
171	ADR_VLD	172	S_REPLY2
173	P_REPLY1	174	P_REPLY0
175	S_REPLY0	176	S_REPLY1
177	S_CLK	178	S_LOAD
179	VDD	180	VDD
181	GND	182	GND
183	GND	184	GND
185	VDD	186	VDD
187	VDD	188	VDD
189	GND	190	GND
191	GND	192	GND
193	VDD	194	VDD
195	VDD	196	VDD
197	GND	198	GND
199	GND	200	GND
201	VDD	202	VDD
203	VDD	204	VDD
205	GND	206	GND
207	GND	208	GND

J0901 Memory/UPA64S Interface Connector Pin Assignments (Continued)

Pin#	Signal Name	Pin #	Signal Name
209	VDD	210	VDD
211	VDD	212	VDD
213	GND	214	GND
215	GND	216	GND

PCI, JTAG and Temperature Sense Interface

The following list gives external-interface connector J0801pin assignments for the PCI, JTAG and temperature-sense signals.

J0801 PCI/JTAG/Temperature Sense Interface Connector Pin Assignments

Pin #	Signal Name	Pin #	Signal Name
1	VDD_CORE	2	VDD_CORE
3	GND	4	GND
5	VDD_CORE	6	VDD_CORE
7	GND	8	GND
9	GND	10	GND
11	GND	12	GND
13	VDD_CORE	14	VDD_CORE
15	GND	16	GND
17	GND	18	GND
19	VDD_CORE	20	VDD_CORE
21	GND	22	GND
23	VDD_CORE	24	VDD_CORE
25	GND	26	GND
27	GND	28	GND
29	GND	30	GND
31	VDD_CORE	32	VDD_CORE
33	GND	34	GND
35	VDD_CORE	36	VDD_CORE
37	GND	38	GND
39	PPCI_AD0	40	PPCI_AD1
41	PPCI_AD2	42	PPCI_AD3
43	PPCI_AD4	44	PPCI_AD5
45	PPCI_AD6	46	PPCI_CBE_L0
47	PPCI_AD7	48	PPCI_AD9
49	PPCI_AD8	50	PPCI_AD10

J0801 PCI/JTAG/Temperature Sense Interface Connector Pin Assignments (Continued)

Pin #	Signal Name	Pin #	Signal Name
51	PPCI_AD11	52	PPCI_AD12
53	PPCI_AD13	54	PPCI_AD14
55	PPCI_AD15	56	PPCI_CBE_L1
57	PPCI_PAR	58	PPCI_SERR_L
59	SPARE	60	PPCI_REQ_L2
61	PPCI_PERR_L	62	PPCI_DEVSEL_L
63	PPCI_REQ_L3	64	PPCI_IRDY_L
65	PPCI_STOP_L	66	PPCI_CBE_L2
67	PPCI_TRDY_L	68	PPCI_AD17
69	PPCI_FRAME_L	70	PPCI_AD19
71	PPCI_AD16	72	PPCI_AD21
73	PPCI_AD18	74	PPCI_AD22
75	PPCI_AD20	76	PPCI_AD23
77	PPCI_REQ_L1	78	PPCI_CBE_L3
79	PPCI_AD24	80	PPCI_AD27
81	PPCI_AD25	82	PPCI_AD28
83	PPCI_AD26	84	PPCI_AD29
85	PPCI_AD30	86	PPCI_AD31
87	PPCI_GNT_L0	88	PCI_CLKSEL0
89	PCI_RESET_L	90	PPCI_REQ_L0
91	GND	92	GND
93	PCI_CLK	94	PCI_REF_CLK
95	GND	96	GND
97	PPCI_GNT_L2	98	PPCI_GNT_L1
99	SB_EMPTY0	100	PPCI_GNT_L3
101	SB_EMPTY1	102	SB_DRAIN
103	INT_NUM0	104	INT_NUM1
105	INT_NUM2	106	INT_NUM3
107	INT_NUM4	108	INT_NUM5
109	SYS_RESET_L	110	PO_RST_L
111	X_RESET_L	112	TCK
113	TDO	114	TMS
115	TDI	116	TEMP_SENSE1
117	TRST_L	118	TEMP_SENSE0
119	PCI_CLKSEL1	120	EPD
121	VDD_CORE	122	VDD_CORE

J0801 PCI/JTAG/Temperature Sense Interface Connector Pin Assignments (Continued)

Pin #	Signal Name	Pin #	Signal Name
123	VDD_CORE	124	VDD_CORE
125	VDD_CORE	126	VDD_CORE
127	VDD_CORE	128	VDD_CORE
129	GND	130	GND
131	GND	132	GND
133	VDD	134	VDD
135	VDD	136	VDD
137	GND	138	GND
139	GND	140	GND
141	VDD	142	VDD
143	VDD	144	VDD

STORAGE AND SHIPPING ENVIRONMENTAL SPECIFICATION

Symbol	Parameter	Conditions	Value			Unit
			Min.	Typ.	Max	
-	Temperature	ambient	- 40	–	90	°C
-	Temperature ramp	ambient	–	–	10	°C/min.
-	Shock (shipping)	Drop height on to any edge, corner, or side of shipping box—single module package	–	–	21	in.
-	Shock (shipping)	Drop height on to any edge, corner, or side of shipping box—multi-module package	–	–	18	in.

HANDLING CPU MODULES

Handle a module by carefully holding it by its edges and by the large CPU heatsink. Do not bump or handle the SRAM heatsinks because this action can cause unseen damage to the solder connections. Always handle modules and other electronic devices in an ESD-controlled environment. Mishandling may cause BGA solder joints to fail.

ORDERING INFORMATION

Part Number	Speed	Description
SME5421MCZ-360	360 MHz CPU, 120 MHz UPA	360 MHz CPU module with a UPA64S bus of 120 MHz using UltraSPARC-II*i* CPU (SME1040CGA-360) with 2MB cache and 66 MHz PCI
SME5421MCZ-333	333 MHz CPU, 111 MHz UPA	333 MHz CPU module with a UPA64S bus of 111 MHz using UltraSPARC-II*i* CPU (SME1040CGA-333) with 2MB cache and 66 MHz PCI

DOCUMENT REVISION HISTORY

Date	Document No.	Change
November 1998	805-5004-02	added description for 360 MHz UltraSPARC-II*i* module
June 1998	805-5004-01	created; describes 333 MHz UltraSPARC-II*i* module

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