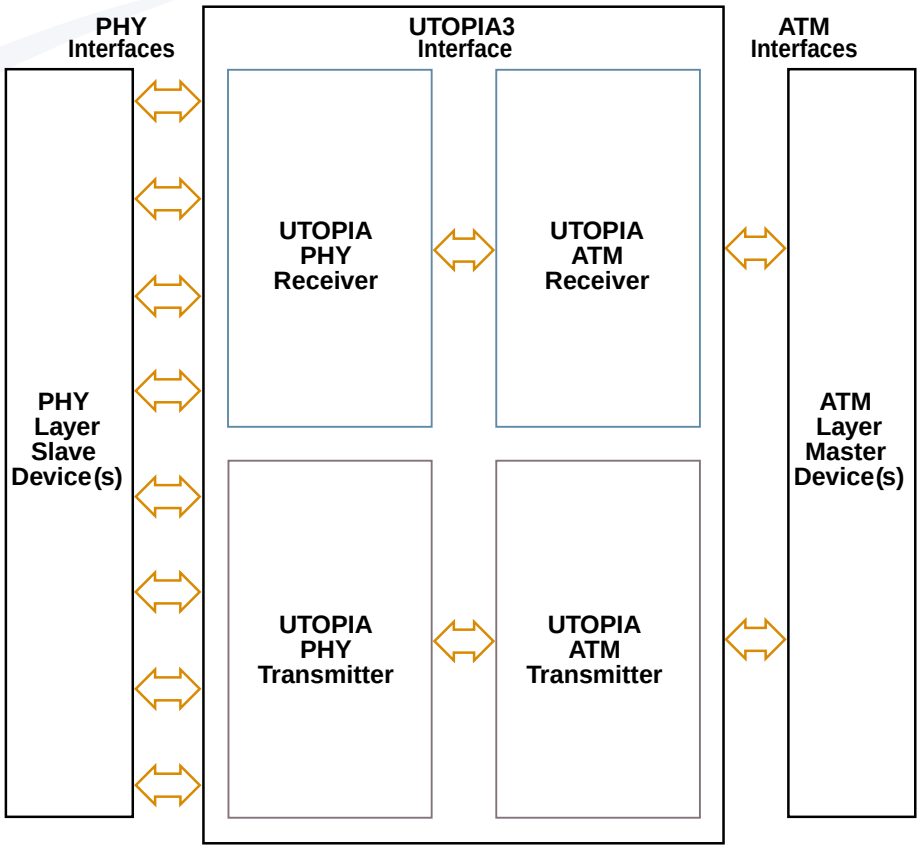
UTOPIA3
UTOPIA 3 Physical Layer Interface Controller

Highlights:

- Fully compliant with ATM Forum's *UTOPIA 3 Physical Layer Interface* specification
- Supports all UTOPIA Physical Layer 3 operation modes
  - Single-PHY (SPHY), Multi-PHY (MPHY)
  Polled or Direct Status
- Configurable data bus widths (8, 16, and 32 bits)
- 150MHz operation speed exceeds specification speed of 104MHz
- Configurable cell formats
- - 52 to 56 octets
- UTOPIA interface error detection and FIFO underflow control
- Configurable number of connected physical (PHY) layer devices
  - one (SPHY mode) to 32 (MPHY mode) PHY devices
- Configurable FIFO size from two cells and up
- Low gate count
- Availability in synthesizable VHDL or Verilog



Overview

inSilicon's UTOPIA3 Physical Layer Interface Controller manages data flow between physical (PHY) layer slave devices and Asynchronous Transfer Mode (ATM) layer master devices. inSilicon's UTOPIA3 Interface Controller is fully compliant with the ATM Forum *UTOPIA3 Physical Layer Interface* specification (af-phy-0a36.000). With the introduction of 32-bit data bus capacity (in addition to 8 and 16 bits), UTOPIA3 handles bit rates of up to 3.2 Gbit/s and runs at 150MHz, exceeding the 104MHz UTOPIA3 specification speed. UTOPIA3 design simplicity enables easy SOC integration, high-speed operation, and suitability for both ASIC and FPGA implementations.

UTOPIA3 PHY-side components provide a bridge between PHY layer devices and the UTOPIA interface. These components consist of several FIFO controller modules (one per each PHY interface) and one UTOPIA interface controller. The FIFO controllers handle dual-port memory reading/writing and perform FIFO depth management and notification to the UTOPIA interface controller. The UTOPIA3 Interface Controller, within these components, provides a data bridge and flow control functionality. The PHY-side components also detect cells of invalid length (discarding cells that are too short and truncating cells that are too long) and assert the FIFO overflow flags if there is no room for the next incoming cell.

Overview (continued)

The ATM-side components transmit and receive ATM cells between an ATM layer device and the UTOPIA Level 3 interface. The status of the PHY components (and their respective FIFO levels) is passed to the ATM layer components through Direct Status or Polling operations. These components provide all the physical interface and protocol functionality described in the specification. The ATM interface is easily integrated into application-specific designs.

UTOPIA3 Configurability

UTOPIA3 may be configured through synthesis-time options, including data bus width, the number of logical PHYs, and the type of polling mode to apply. No CPU interface is associated with this device.

Complete Verification, Test Environment, and Documentation

inSilicon's thorough test methodology verifies functional compliance and verification using complete vector testing. To facilitate system verification, the device is delivered with a comprehensive test environment that verifies functional compliance to the UTOPIA Level 3 specification. Thorough user manuals on the UTOPIA3 interface controller and test environment are also included in the database.

inSilicon Maintenance Program

inSilicon offers a maintenance program for UTOPIA3. The maintenance program provides the customer with regular product updates for compatibility, errata, and application notes. Full customer support is available via hotline (1-888-482-4477) and e-mail (support@inSilicon.com).

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