UT1553B RTI Remote Terminal Interface

FEATURES

- ❒ Complete MIL-STD-1553B Remote Terminal interface compliance
- ❒ Dual-redundant data bus operation supported
- ❒ Internal illegalization of selected mode code commands
- ❒ External illegal command definition capability
- ❒ Automatic DMA control and address generation
- ❒ Operational status available via dedicated lines or internal status register
- ❒ ASD/ENASC (formerly SEAFAC) tested and approved
- ❒ Available in ceramic 84-lead leadless chip carrier and 84-pin pingrid array
- ❒ Full military operating temperature range, -55°C to +125°C, screened to the specific test methods listed in Table I of MIL-STD-883, Method 5004, Class B
- ❒ JAN-qualified devices available

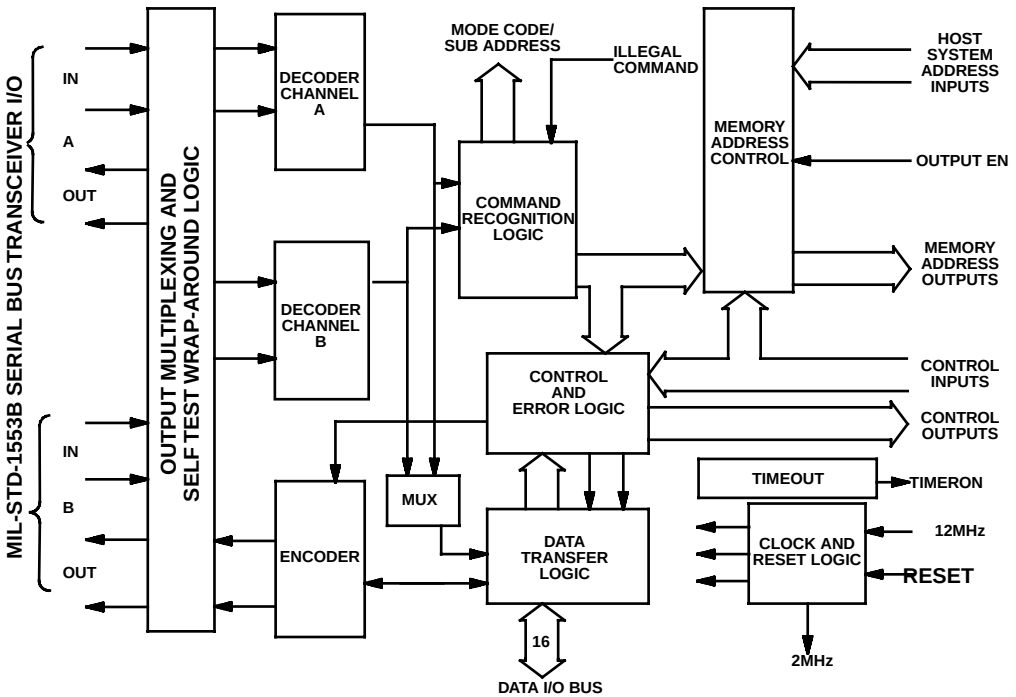


Figure 1. UT1553B RTI Functional Block Diagram

Table of Contents

1.0 ARCHITECTURE AND OPERATION

The UT1553B RTI is an interface device linking a MIL-STD-1553 serial data bus and a host microprocessor system. The RTI's MIL-STD-1553B interface includes encoding/decoding logic, error detection, command recognition, memory address control, clock, and reset circuits.

Decoders
The UT1553B RTI contains two separate free-running decoders to insure that all redundancy requirements of MIL-STD-1553B are met. Each decoder receives, decodes, and verifies biphase Manchester II data. Proper frequency and edge skew are also verified.

Command Recognition Logic
The command recognition logic monitors the output of both decoders at all times. Recognition of a valid command causes a reset of present interface activity followed by execution of the command. This procedure meets the requirement for superseding valid commands.

Encoder
The encoder receives serial data from the data transfer logic, converts it to Manchester II form with proper synchronization and parity, and passes it to the output and self-test logic.

Data Transfer Logic
The data transfer logic provides double-buffered 16-bit parallel-to-serial and serial-to-parallel conversion during reception and transmission of data.

Memory Address Control
The memory address control logic controls the output of the three-state address lines during memory access. In DMA system implementations, the memory address control provides RTI-generated addresses. In a pseudo-dual-port memory configuration, the memory address control logic provides either RTI-generated or host system addressing.

Control and Error Logic
The control and error logic performs the following four major functions:

- Interface control for proper processing of MIL-STD-1553B commands
- Error checking of both MIL-STD-1553B data and RTI operation
- Memory control (DMA or pseudo-dual-port) for proper data transfer
- Operational status and control signal generation

Output Multiplexing and Self-Test Logic
This logic directs the output of the encoder to one of four places:- Channel A outputs
- Channel B outputs
- Channel A decoders during self-test
- Channel B decoders during self-test

Clock and Reset Logic
The UT1553B RTI requires a 12MHz input clock to operate properly. The RTI provides a 2MHz output for the system designer to use. The device provides a hardware reset pin as well as software-generated reset.

Timer Logic
The UT1553B RTI has a built-in 730ms timer that is activated when the encoder is about to transmit. The timer is reset upon receipt of a valid command, master reset, or a time-out condition.

1.1 HOST INTERFACE

Configure the RTI into the host system for either a direct memory or transparent memory access. The following sections discuss the system configuration for each method of memory management.

1.1.1 Direct Memory Access
In the direct memory access configuration the RTI and host arbitrate for the shared 2K x 16 memory space. To request access to memory the RTI asserts direct memory request output (DMARQ); the system bus arbiter grants the RTI access to memory by asserting the direct memory access grant signal ($\overline{\text{MEMCK}}$). The system arbiter should not assert the $\overline{\text{MEMCK}}$ signal before the RTI has requested access to memory (i.e., DMARQ asserted).

Once granted access to memory, the RTI address out (ADDR OUT(10:0)), RAM chip select ($\overline{\text{RCS}}$), RAM read/write (RRD/$\overline{\text{RWR}}$), and Data bus (DATA I/O(15:0)) provide the interface signals to control the memory access. Figure 2 shows an example of a direct memory access system configuration; for clarity the interface buffers and logic are excluded. The host microprocessor also gains access to memory by arbitration.

Take care to insure that bus contention does not occur between the host and RTI Address buses or memory control signals. To place the RTI Address Out bus in a high impedance state negate the $\overline{\text{ADOEN}}$ input pin. Also note that outputs $\overline{\text{RCS}}$ and RRD/$\overline{\text{RWR}}$ are not three-state outputs. When the RTI is not writing to memory, bidirectional Data bus DATA I/O(15:0) is an input (i.e., not actively driving the bus).

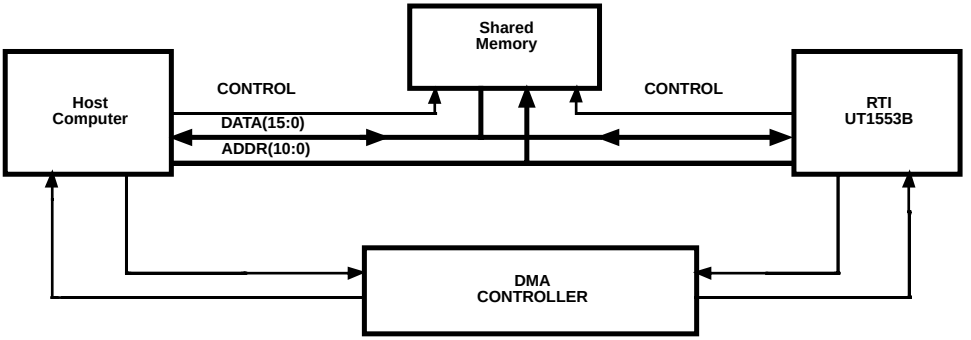


Figure 2. Direct Memory Access Configuration

The host microprocessor gains access to the RTI internal registers by controlling input pins $\overline{CS}$, $\overline{CTRL}$, ADDR IN (10:0), and RD/$\overline{WR}$. During message processing the host microprocessor should limit access to RTI internal registers.

1.1.2 Transparent Memory Access
Configured in the transparent memory mode the host microprocessor accesses shared memory through the RTI. Arbitration for access to the bus is performed as discussed in section 1.1.1 of this document.

When granted access to memory, the RTI asserts memory control signals ADDR OUT(10:0), $\overline{RCS}$, and RRD/$\overline{RWR}$. For host-controlled memory accesses the RAM memory address from the host is propagated from the Address In bus ADDR IN (10:0) to the Address Out bus ADDR OUT (10:0). Memory control signals RD/$\overline{WR}$ and $\overline{CS}$ are also propagated through the RTI as RRD/$\overline{RWR}$ and $\overline{RCS}$. Input $\overline{CTRL}$ is negated during all transparent memory accesses to prevent the RTI from inadvertently performing an internal register access or software reset. While $\overline{CS}$ is asserted, the RTI's bidirectional Data bus DATA I/O (15:0) is an input (i.e., not actively driving bus).

The host microprocessor gains access to the RTI internal registers by controlling input pins $\overline{CS}$, $\overline{CTRL}$, ADDR IN (10:0), and RD/$\overline{WR}$. During message processing the host microprocessor should limit access to RTI internal registers. The host should not assert $\overline{CS}$ while the RTI is performing a memory access.

1.2 Internal Register Description
The RTI uses three internal registers to allow the host to control the RTI operation and monitor its status. The host uses the following inputs Control ($\overline{CTRL}$), Chip Select ($\overline{CS}$), Read/Write (RD/$\overline{WR}$), and ADDR IN (0) to read the 16-bit System Register or write to the 8-bit Control Register. The Control Register toggles bits in the MIL-STD-1553B status word, enables biphase inputs, selects terminal active flag, and puts the part in self-test. The System Register supplies operational status of the UT1553B RTI to the host. The Last Command Register saves the command word for a Transmit Last Command mode code, along with operational status from the System Register.

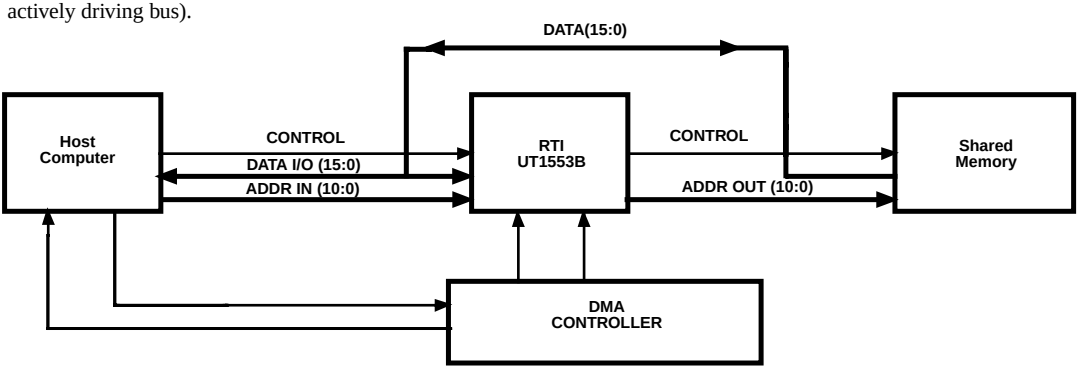


Figure 3. Transparent Memory Access Configuration

Control Register (Write Only)

The 8-bit write-only Control Register manages the operation of the RTI. Write to the Control Register by applying a logic zero to $\overline{CS}$, $\overline{CTRL}$, RD/$\overline{WR}$, and ADDR IN (0); if ADDR IN (0) is a logic one a master reset occurs. Data is loaded into the Control Register via I/O pins DATA(7:0). Control Register writes must occur 50ns before the rising edge of $\overline{COMSTR}$ to latch data in the outgoing status word.

Bit Number	Initial Condition	Description
0	[0]	Channel A Enable. A logic one enables Channel A biphase inputs.
1	[0]	Channel B Enable. A logic one enables Channel B biphase inputs.
2	[0]	Terminal Flag. A logic one sets the Terminal Flag bit of the Status Register.
3	[0]	System Busy. A logic one sets the Busy bit of the System Register and inhibits RTI access to memory. No data words are retrieved or stored; command word is stored.
4	[0]	Subsystem Busy. A logic one sets the Subsystem Flag bit of the Status Register.
5	[0]	Self-Test Channel Select. This bit selects which channel the internal self-test checks; a logic one selects Channel A and a logic zero selects Channel B.
6	[0]	Self-Test Enable. A logic one sets the RTI in the internal self-test mode and inhibits its normal operation. Internal testing is not visible on biphase output channels.
7	[0]	Service Request. A logic one sets the Service Request bit of the Status Register.

CONTROL REGISTER (WRITE ONLY)

X	X	X	X	X	X	X	X	SRV RQ	SELF TEST	SELF CH	SUBS	BUSY	TF	CH B EN	CH A EN
								[0]	[0]	[0]	[0]	[0]	[0]	[0]	[0]
MSB															LSB

[ ] defines reset state

Figure 4. Control Register

System Register (Read Only)

The 16-bit read-only System Register provides the RTI system status. Read the System Register by applying a logic zero to $\overline{CS}$, $\overline{CTRL}$, ADDR IN (0), and a logic one to RD/$\overline{WR}$. The 16-bit contents of the System Register are read from data I/O pins DATA(15:0).

Bit Number	Initial Condition	Description
0	[0]	MCSA(0). The LSB of the mode code or subaddress as indicated by the logic state of bit 5.
1	[0]	MCSA(1). Mode code or subaddress as indicated by the state of bit 5.
2	[0]	MCSA(2). Mode code or subaddress as indicated by the state of bit 5.
3	[0]	MCSA(3). Mode code or subaddress as indicated by the state of bit 5.
4	[0]	MCSA(4). Mode code or subaddress as indicated by the state of bit 5.
5	[0]	$\overline{MC}$/SA. A logic one indicates that bits 4 through 0 are the subaddress of the last command word, and that the last command word was a normal transmit orreceive command. A logic zero indicates that bits 4 through 0 are a mode code, and that the last command was a mode code.
6	[1]	Channel A/$\overline{B}$. A logic one indicates that the most recent command arrived onChannel A; a logic zero indicates that it arrived on Channel B.

7	[0]	Channel B Enabled. A logic one indicates that Channel B is available for both reception and transmission.
8	[0]	Channel A Enabled. A logic one indicates that Channel A is available for both reception and transmission.
9	[1]	Terminal Flag Enabled. A logic one indicates that the Bus Controller has not issued an Inhibit Terminal Flag mode code. A logic zero indicates that the Bus Controller, via the above mode code, is overriding the host system's ability to set the Terminal Flag bit of the status word.
10	[0]	Busy. A logic one indicates the Busy bit is set. This bit is reset when the SystemBusy bit in the Control Register is reset.
11	[0]	Self-Test. A logic one indicates that the RTI is in the self-test mode. This bit isreset when the self-test is terminated.
12	[0]	TA Parity Error. A logic one indicates the wrong Terminal Address parity; it causes the biphase inputs to be disabled and a message error condition. This bit is reset by reloading the terminal address latch with correct parity.
13	[0]	Message Error. A logic one indicates that a message error has occurred since the last System Register read. This bit is not reset until the System Register has been examined and the message error condition is removed.
14	[0]	Valid Message. A logic one indicates that a valid message has been received since the last System Register read. This bit is not reset until the System Register has been examined.
15	[0]	Terminal Active. A logic one indicates the device is executing a transmit or receive operation. The state of this bit is the logical NAND of the external $\overline{\text{XMIT}}$ and $\overline{\text{RCV}}$ pins.

SYSTEM REGISTER (READ ONLY)

TERM ACTV	VAL MESS	MESS ERR	TAPA ERR	SELF-TEST	BUSY	TFEN	CH A EN	CH B EN	CHNL A/B	$\overline{\text{MC}}$/SA	MCSA 4	MCSA 3	MCSA 2	MCSA 1	MCSA 0
[0]	[0]	[0]	[0]	[0]	[0]	[1]	[0]	[0]	[1]	[0]	[0]	[0]	[0]	[0]	[0]

MSB LSB

[ ] defines reset state

Figure 5. System Registers

Last Command Register (Read Only)
The 16-bit read-only Last Command Register provides the host with last command and operational status information. The RTI transmits the lower 11 bits of this register along with terminal address upon receipt of a Transmit Last Command mode code. Read the Last Command Register by applying a logic zero to $\overline{CS}$, $\overline{CTRL}$, and a logic one to RD/$\overline{WR}$ and ADDR IN (0). The 16-bit contents of the Last Command Register are read from data I/O pins DATA(15:0).

Bit Number	Initial Condition	Description
0 through 10	[all 1s]	Least significant 11 bits of the last command word.
11	[0]	Busy Bit. System Register bit 10.
12	[0]	Self-test. System Register bit 11.
13	[1]	Terminal Flag Enabled. System Register bit 9.
14	[1]	Channel A/$\overline{B}$. System Register bit 6.
15	[1]	Illegal Command. The RTI illegalized the last command.

1.3 Mode Codes and Subaddresses

The UT1553B RTI provides subaddress and mode code decoding meeting MIL-STD-1553B. In addition, the device has automatic internal illegal command decoding for reserved MIL-STD-1553B mode codes. Upon command word validation and decode, status pins MCSA(4:0) and $\overline{MC}$/SA become valid. Status pin $\overline{MC}$/SA will indicate whether the data pins MCSA(4:0) are mode code or subaddress information. Status Register bits 5 through 0 contain the same information as pins MCSA(4:0) and $\overline{MC}$/SA.

The system designer can use signals MCSA(4:0), $\overline{MC}$/SA, $\overline{BRDCST}$, $\overline{XMIT}$, and $\overline{RCV}$ to illegalize mode codes, subaddresses, and other message formats via the Illegal Command (ILL COMM) input (see figure 23 on page 36).

The RTI will internally decode the following mode codes as illegal:

- Dynamic Bus Control
- Selected Transmitter Shutdown
- Override Selected Transmitter Shutdown
- All Reserved Mode Codes

If the RTI receives one of the above mode codes, the RTI responds by transmitting a status word with the Message Error bit set to logic one.

.

Mode codes which involve data transfer are processed like receive and transmit commands. The RTI will not generate DMA request for Transmit Status Word and Transmit Last Command mode codes since the information is stored internal to the RTI.

The following mode codes require assistance from the host:

- Synchronize
- Initiate Self-Test
- Reset Remote Terminal

For example, the RTI will accept and respond to a Reset Remote Terminal mode code; however it will not perform a reset operation. The host must interpret the mode code and take appropriate action.

The RTI does not define or interpret the following data words associated with mode code commands:

- Transmit Vector Word
- Synchronize With Data Word
- Transmit Bit Word

The RTI will accept and respond to mode code with data; the host must interpret or define the data word. The RTI will store or retrieve the data required for mode code command from block #1 of the receive or transmit page

RTI MODE CODE HANDLING PROCEDURE

T/$\overline{R}$	Mode Code	Function	Operation
0	10100	Selected Transmitter Shutdown [2]	1. Command word stored 2. MES ERR pin asserted 3. Message error latch set in System Register 4. Status word transmitted
0	10101	Override Selected Transmitter Shutdown [2]	1. Command word stored 2. MES ERR pin asserted 3. Message error latch set in System Register 4. Status word transmitted
0	10001	Synchronize (w/data)	1. Command word stored 2. Data word stored 3. Status word transmitted
1	00000	Dynamic Bus Control [2]	1. Command word stored 2. MES ERR pin asserted 3. Message error latch set in System Register 4. Status word transmitted
1	00001	Synchronize [1]	1. Command word stored 2. Status word transmitted
1	00010	Transmit Status Word [3]	1. Command word stored 2. Status word transmitted
1	00011	Initiate Self-Test [1]	1. Command word stored 2. Status word transmitted
1	00100	Transmitter Shutdown	1. Command word stored 2. Alternate bus shutdown 3. Status word transmitted
1	00101	Override Transmitter Shutdown	1. Command word stored 2. Alternate bus enabled 3. Status word transmitted
1	00110	Inhibit Terminal Flag Bit	1. Command word stored 2. Terminal Flag bit set to zero and disabled 3. Status word transmitted
1	00111	Override Inhibit Terminal Flag Bit	1. Command word stored Bit 2. Terminal Flag bit enabled, but not set to logic one 3. Status word transmitted
1	01000	Reset Remote Terminal [1]	1. Command word stored 2. Status word transmitted
1	10010	Transmit Last Command Word [3]	1. Status word transmitted 2. Last command word transmitted
1	10000	Transmit Vector Word	1. Command word stored 2. Status word transmitted 3. Data word transmitted
1	10011	Transmit BIT Word	1. Command word stored 2. Status word transmitted 3. Data word transmitted

Notes:

1. Further host interaction required for mode code operation.
2. Reserved mode code; A) MES ERR pin asserted, B) Message Error bit set, C) status word transmitted (ME bit set to logic one).
3. Status word not affected.

1.4 MIL-STD-1553B Subaddress and Mode Code Definitions

Table 1. Subaddress and Mode Code Definitions Per MIL-STD-1553B

Subaddress Field Binary (Decimal)	Message Format		Description
	Receive	Transmit	
00000 (00)	1	1	Mode Code Indicator
00001 (01)	User Defined	User Defined	
00010 (02)	User Defined	User Defined	
00011 (03)	User Defined	User Defined	
00100 (04)	User Defined	User Defined	
00101 (05)	User Defined	User Defined	
00110 (06)	User Defined	User Defined	
00111 (07)	User Defined	User Defined	
01000 (08)	User Defined	User Defined	
01001 (09)	User Defined	User Defined	
01010 (10)	User Defined	User Defined	
01011 (11)	User Defined	User Defined	
01100 (12)	User Defined	User Defined	
01101 (13)	User Defined	User Defined	
01110 (14)	User Defined	User Defined	
01111 (15)	User Defined	User Defined	
10000 (16)	User Defined	User Defined	
10001 (17)	User Defined	User Defined	
10010 (18)	User Defined	User Defined	
10011 (19)	User Defined	User Defined	
10100 (20)	User Defined	User Defined	
10101 (21)	User Defined	User Defined	
10110 (22)	User Defined	User Defined	
10111 (23)	User Defined	User Defined	
11000 (24)	User Defined	User Defined	
11001 (25)	User Defined	User Defined	
11010 (26)	User Defined	User Defined	
11011 (27)	User Defined	User Defined	
11100 (28)	User Defined	User Defined	
11101 (29)	User Defined	User Defined	
11110 (30)	User Defined	User Defined	
11111 (31)	1	1	Mode Code Indicator

Note:
1. Refer to mode code assignments per MIL-STD-1553B

1.5 Remote Terminal Address

Assign the RTI remote terminal address by either a software or hardware exercise. The host assigns the RTI remote terminal address by performing a Control Register write; the Terminal Address bus (TA(4:0)) is strobed into the RTI Remote Terminal Address Register upon completion of the Control Register write. To assign the RTI remote terminal address via hardware, use the $\overline{\text{TALEN}}$/PARITY input pin operating in the terminal latch address enable mode. The Terminal Address bus is latched into the RTI while the $\overline{\text{TALEN}}$ is asserted (i.e., logic low). Valid remote terminal addresses (RTA) include decimal 0 through 31 if Broadcast is disabled, 0 through 30 if Broadcast is enabled

Parity Checker

An address parity check is performed to insure the remote terminal address applied to TA(4:0) was properly latched into the Remote Terminal Address Register. To perform a parity check, enable the RTI parity circuit via EXT TEST and EXT TST CH SEL A/$\overline{\text{B}}$ input pins. The parity bit is entered through the $\overline{\text{TALEN}}$/PARITY input pin operating in the parity mode. Input pins EXT TEST and EXT TST CH SEL A/$\overline{\text{B}}$ control dual-function input pin $\overline{\text{TALEN}}$/PARITY; see table 2 for description of operation.

If a parity error exists, the Parity Error bit of the System Register is set to a logic one, biphase Channels A and B are disabled (set to logic zero), the Message Error bit set to logic one, and the message error pin is asserted.

Table 2. Parity Checking

STATE #	EXT TEST	EXT TST CH SEL A/$\overline{B}$	Function of $\overline{TALEN}$/PARITY
0	0	0	Terminal Address Latch Enable. Active low signal used to latch TA(4:0) into RTI. Internal parity checker disabled.
1	0	1	Parity. Internal remote terminal address parity checker enabled. $\overline{TALEN}$/PARITY pin functions as parity bit for TA(4:0) bus. Proper operation requires odd parity.
2	1	0	Terminal Address Latch Enable. Do not assert EXT TST during reset, otherwise self-test is invoked.
3	1	1	Terminal Address Latch Enable. Do not assert EXT TST during reset, otherwise self-test is invoked.

The following are examples of sequences used to enter remote terminal addresses into the RTI.

Example 1. Hardware-Controlled Remote Terminal Address (parity check disabled):

$\overline{STATE}$ 0, 2, or 3 (i.e., 00, 10, or 11)
$\overline{TALEN}$ - asserted (i.e., logic low)
TA(4:0) - valid RTA

Example 2. Software-Controlled Remote Terminal Address (parity check disabled):

EXT TEST and EXT TST CH SEL A/$\overline{B}$ in $\overline{STATE}$ 0, 2, or 3 (i.e., 00, 10, or 11)
$\overline{CTRL}$ - logic zero
$\overline{CS}$ - logic zero
RD/$\overline{WR}$ - logic zero
$\overline{ADDR}$ IN (0) - logic zero
$\overline{TALEN}$ - logic one
TA(4:0) - valid RTA

Example 3. Software Controlled Remote Terminal Address (parity check enabled):

EXT TEST and EXT TST CH SEL A/$\overline{B}$ in $\overline{STATE}$ 1 (i.e., 01)
$\overline{CTRL}$ - logic zero
$\overline{CS}$ - logic zero
RD/$\overline{WR}$ - logic zero
ADDR IN (0) - logic zero
PARITY - input must provide odd parity
for the TA(4:0) bus
TA(4:0) - valid RTA

For examples 1 and 2, enabling the parity check circuit (STATE 1) after the remote terminal address is stored results in a parity check of the data loaded into the Remote Terminal Address Register.

1.6 Internal Self-Test

Setting bit 6 of the Control Register to a logic one enables the internal self-test. Disable Channels A and B at this time to prevent bus activity during self-test by setting bits 0 and 1 of the Control Register to a logic zero. Normal operation is inhibited when internal self-test is enabled. The RTI's self-test capability is based on the fact that the MIL-STD-1553B status word sync pulse is identical to the command word sync pulse. Thus, if the status word from the encoder is fed back to the decoder, the RTI will recognize the incoming status word as a command word and thus cause the RTI to transmit another status word. After the host invokes self-test, the RTI self-test logic forces a status word transmission even though the RTI has not received a command word. The status word is sent to decoder A or B depending on the channel the host selected for self-test. The host controls the self-test by periodically changing the bit patterns in the status word being transmitted. Writing to the Control Register bits 2, 3, 4, and 8 changes the status word. Monitor the self-test by sampling either the System Register or the external status pins (i.e. Command Strobe ($\overline{COMSTR}$), Transmit ($\overline{XMIT}$), Receive ($\overline{RCV}$)). For a more detailed explanation of internal self-test, consult the UTMC publication *RTI Internal Self-Test Routine.*

1.7 Power-up Master Reset

Reset the RTI by invoking either a hardware or software master reset after power-up to place the device in a known state. The master reset clears the decoder and encoder registers, the command recognition logic, the control and error logic (which includes the Status, Control and System Registers), the data transfer logic, and the memory address control logic. After reset, configure the device for operation via a Control Register write.

Perform a hardware reset by asserting the $\overline{\text{MRST}}$ input pin for a minimum of 500ns. During reset negate the EXT TEST pin (i.e., logic low); assertion of the EXT TEST pin forces the RTI to enter the external self-test mode of operation.

Software reset the RTI by simultaneously applying a logic zero to input pins $\overline{\text{CS}}$, RD/$\overline{\text{WR}}$, and $\overline{\text{CTRL}}$ while the least significant bit of the address input bus is a logic one (ADDR IN (0)=0).

1.8 Encoder and Decoder

The RTI interfaces directly to a bus transmitter/receiver via the RTI Manchester II encoder/decoder. The UT1553B RTI receives the command word from the MIL-STD-1553B bus and processes it either by the primary or secondary decoder. Each decode checks for the proper sync pulse and Manchester waveform, edge skew, correct number of bits, and parity. If the command is a receive command, the RTI processes each incoming data word for correct word count and contiguous data. If an invalid message error is detected, the message error pin is asserted, the RTI ceases processing the remainder (if any) of the message, and it then suppresses status word transmission. Upon command validation recognition, the external status outputs are enabled. Reception of illegal commands does not suppress status word transmission.

A timer precludes transmission greater than 730ms by the assertion of fail-safe timer ($\overline{\text{TIMERON}}$). This timer is reset upon receipt of another valid command.

1.9 Illegal Command Decoding

The host has the option of asserting the ILL COMM pin to illegalize a received command word. On receipt of an illegal command, the RTI sets the message error bit in the status word, sets the Message Error output, and sets the message error latch in the System Register.

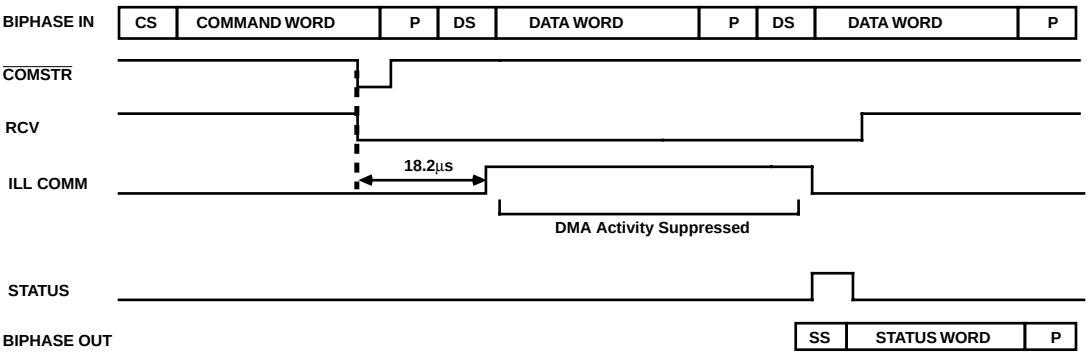
Use the following RTI outputs to externally decode an illegal command, Mode Code or Subaddress indicator ($\overline{\text{MC}}$/SA), Mode Code or Subaddress bus MCSA(4:0), Command Strobe ($\overline{\text{COMSTR}}$), Broadcast ($\overline{\text{BRDCST}}$), etc. (See figure 6 pages 11-12).

To illegalize a transmit command the ILL COMM pin is asserted 3.3ms after STATUS goes to a logic one. Assertion of the ILL COMM pin within 3.3ms allows the RTI to respond with the Message Error bit of the outgoing status word at a logic one.

For an illegal receive command, the ILL COMM pin is asserted within 18.2ms after the $\overline{\text{COMSTR}}$ transitions to a logic zero in order to suppress data words from being stored (suppress DMARQ assertions). In addition, the ILL COMM pin must be at a logic one throughout the reception of the message until STATUS is asserted.

If the illegal command is mode code 2, 4, 5, 6, 7, or 18, assert the ILL COMM pin within 664ns after Command Strobe ($\overline{\text{COMSTR}}$) transitions to logic zero. Asserting the ILL COMM pin within the 664 nanoseconds inhibits the mode code function.

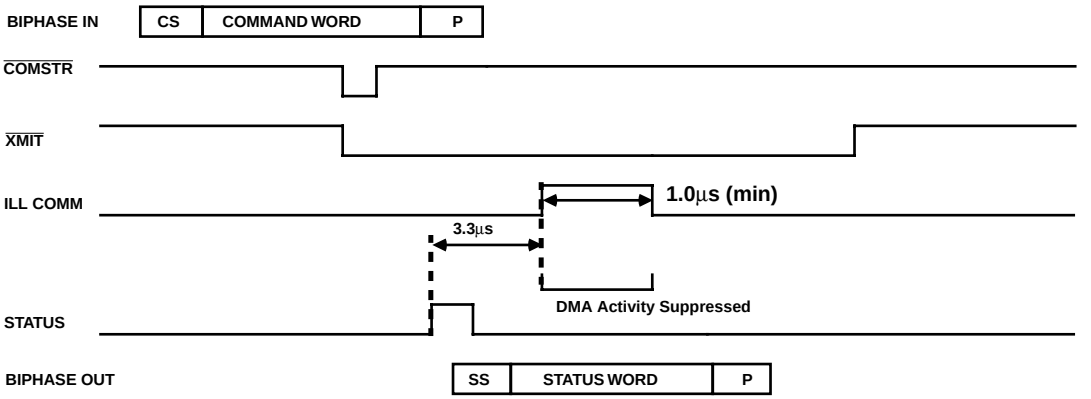
The above timing conditions also apply when the host externally decodes an illegal broadcast command. The host must remove the illegal command condition so that the next command is not falsely decoded as illegal. These requirements are easily met if the $\overline{\text{COMSTR}}$ output is used to qualify the ILL COMM input to the RTI.



Note:

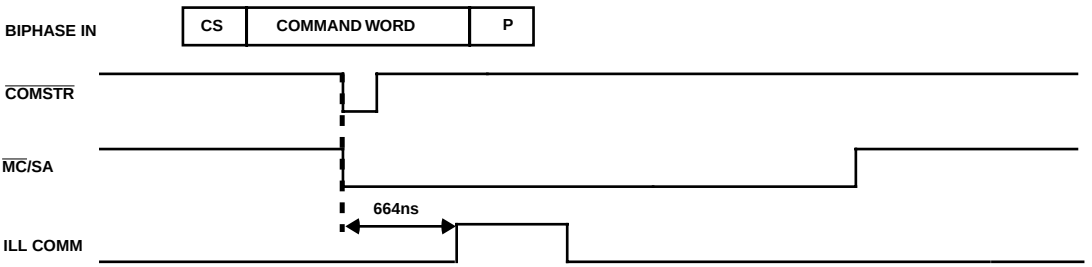
1. Illegal command condition; status word Message Error bit set to logic one, RTI MESERR pin set to a logic one, RTI Status Register Message Error bit set to logic one.

Figure 6a. Illegal Receive Command Decoding



Note:
1. Illegal command condition; status word Message Error bit set to logic one, RTI MES ERR pin set to a logic one, RTI Status Register Message Error bit set to logic one.

Figure 6b. Illegal Transmit Command Decoding



Note:
1. To illegalize mode codes 2, 4, 5, 6, 7, or 18 assert ILL COMM within 664ns of COMSTR's transition to logic zero. Asserting the ILL COMM within 664ns inhibits the mode code function.

Figure 6c. Mode Code Command Decoding

2.0 MEMORY MAP EXAMPLE

The RTI is capable of addressing 2048 x 16 of external memory for message storage. The 2K memory space is divided into two 1K pages and subdivided into 32 blocks of 32 x 16:

Page 1 (Receive): 32 blocks for receive messages (32 x 16)

Page 2 (Transmit): 32 blocks for transmit messages (32 x 16)

Address Decode

The RTI derives addresses (i.e., data pointers) for external memory directly from the 11 least significant bits of the command word. The address data pointer corresponds to ADDR OUT (10:0) during RTI memory accesses.

T/$\overline{R}$ = ADDR OUT (10)
SUBADDRESS/MODE = ADDR OUT (9:5) WORD COUNT/MODE CODE = ADDR OUT (4:0)

The T/$\overline{R}$ bit of the command word becomes the most significant bit of the data pointer; the T/$\overline{R}$ bit serves to divide the RAM into transmit and receive pages of 1K each. The 5-bit subaddress/mode field is used to select 1 of 32 possible message storage blocks within the transmit or receive message page. The 5-bit word count/mode code field acts as a data pointer to select one of 32 locations within the message storage block. Multiple word messages are stored from top to bottom within the message storage block.

For mode commands, the address data pointer always contains 00000 in the $\overline{MC}$/SA field, regardless of whether 00000 or 11111 was received. Forcing the mode code field to 00000 reserves the first message storage block on both pages (receive and transmit) for mode code messages that require data. The 5-bit mode code specifies which of the 32 locations within the message storage block to access.

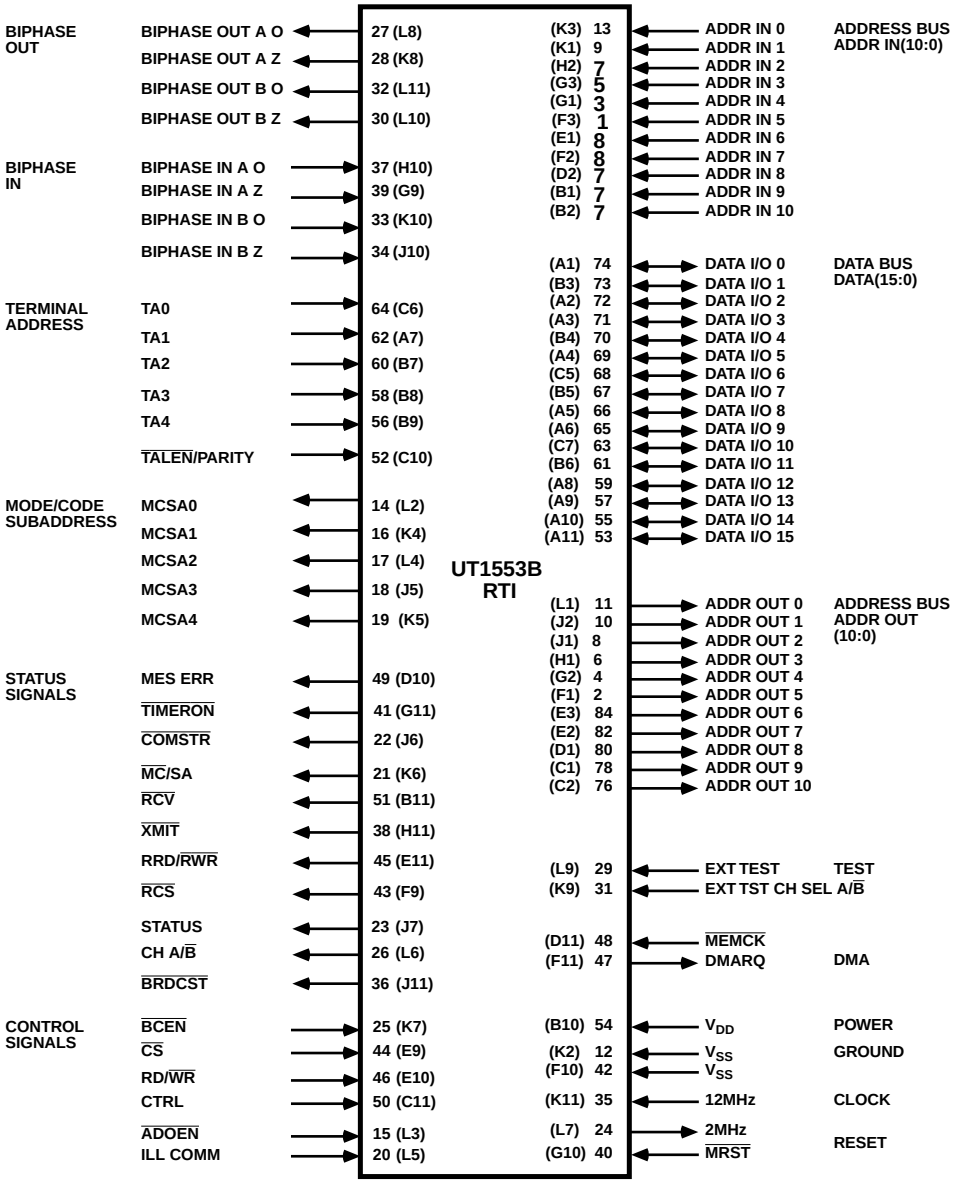
For “wrap-around” applications (transmission of data previously received), force the RTI to store and receive messages on one memory page. To accomplish one-page operation do not use the T/$\overline{R}$ output pin. Eliminating the T/$\overline{R}$ limits the RTI access to only one page and the RTI will not differentiate between receive and transmit pages.

Table 3. RTI Memory Map

1: Receive Memory Map			2: Transmit Memory map		
Block #	**Operation**	**Address Field (hex)**	**Block #**	**Operation**	**Address Field (hex)**
1	Mode Code [1]	000 to 01F	1	Mode Code [1]	400 to 41F
2	Subaddress 1	020 to 03F	2	Subaddress 1	420 to 43F
3	Subaddress 2	040 to 05F	3	Subaddress 2	440 to 45F
4	Subaddress 3	060 to 07F	4	Subaddress 3	460 to 47F
5	Subaddress 4	080 to 09F	5	Subaddress 4	480 to 49F
6	Subaddress 5	0A0 to 0BF	6	Subaddress 5	4A0 to 4BF
7	Subaddress 6	0C0 to 0DF	7	Subaddress 6	4C0 to 4DF
8	Subaddress 7	0E0 to 0FF	8	Subaddress 7	4E0 to 4FF
9	Subaddress 8	100 to 11F	9	Subaddress 8	500 to 51F
10	Subaddress 9	120 to 13F	10	Subaddress 9	520 to 53F
11	Subaddress 10	140 to 15F	11	Subaddress 10	540 to 55F
12	Subaddress 11	160 to 17F	12	Subaddress 11	560 to 57F
13	Subaddress 12	180 to 19F	13	Subaddress 12	580 to 59F
14	Subaddress 13	1A0 to 1BF	14	Subaddress 13	5A0 to 5BF
15	Subaddress 14	1C0 to 1DF	15	Subaddress 14	5C0 to 5DF
16	Subaddress 15	1E0 to 1FF	16	Subaddress 15	5E0 to 5FF
17	Subaddress 16	200 to 21F	17	Subaddress 16	600 to 61F
18	Subaddress 17	220 to 23F	18	Subaddress 17	620 to 63F
19	Subaddress 18	240 to 25F	19	Subaddress 18	640 to 65F
20	Subaddress 19	260 to 27F	20	Subaddress 19	660 to 67F
21	Subaddress 20	280 to 29F	21	Subaddress 20	680 to 69F
22	Subaddress 21	2A0 to 2BF	22	Subaddress 21	6A0 to 6BF
23	Subaddress 22	2C0 to 2DF	23	Subaddress 22	6C0 to 6DF
24	Subaddress 23	2E0 to 2FF	24	Subaddress 23	6E0 to 6FF
25	Subaddress 24	300 to 31F	25	Subaddress 24	700 to 71F
26	Subaddress 25	320 to 33F	26	Subaddress 25	720 to 73F
27	Subaddress 26	340 to 35F	27	Subaddress 26	740 to 75F
28	Subaddress 27	360 to 37F	28	Subaddress 27	760 to 77F
29	Subaddress 28	380 to 39F	29	Subaddress 28	780 to 79F
30	Subaddress 29	3A0 to 3BF	30	Subaddress 29	7A0 to 7BF
31	Subaddress 30	3C0 to 3DF	31	Subaddress 30	7C0 to 7DF
32	Unused	3E0 to 3FF	32	Unused	7E0 to 7FF

Notes:
1. Receive mode codes with data:
   - Synchronize with data
   - Selected Transmitter Shutdown (Illegal)
   - Override Selected Transmitter Shutdown (Illegal)
2. Transmit mode codes with data:
   - Transmit Vector Word
   - Transmit Bit Word

3.0 PIN IDENTIFICATION AND DESCRIPTION



Note:
Pingrid array numbers are in parentheses. LCC pin numbers are not in parentheses.

Figure 7. UT1553B RTI Pin Description

Legend for TYPE and ACTIVE fields:

TI = TTL input
TUI = TTL input (pull-up)
TDI = TTL input (pull-down)
TO = TTL output
TTO = Three-state TTL output
TTB = Three-state TTL bidirectional

[ ] - Values in parentheses indicate the initialized state of output pin.

DATA BUS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
DATA I/O 15	53	A11	TTB	--	Bit 15 (MSB) of the bidirectional Data bus.
DATA I/O 14	55	A10	TTB	--	Bit 14 of the bidirectional Data bus.
DATA I/O 13	57	A9	TTB	--	Bit 13 of the bidirectional Data bus.
DATA I/O 12	59	A8	TTB	--	Bit 12 of the bidirectional Data bus.
DATA I/O 11	61	B6	TTB	--	Bit 11 of the bidirectional Data bus.
DATA I/O 10	63	C7	TTB	--	Bit 10 of the bidirectional Data bus.
DATA I/O 9	65	A6	TTB	--	Bit 9 of the bidirectional Data bus.
DATA I/O 8	66	A5	TTB	--	Bit 8 of the bidirectional Data bus.
DATA I/O 7	67	B5	TTB	--	Bit 7 of the bidirectional Data bus.
DATA I/O 6	68	C5	TTB	--	Bit 6 of the bidirectional Data bus.
DATA I/O 5	69	A4	TTB	--	Bit 5 of the bidirectional Data bus.
DATA I/O 4	70	B4	TTB	--	Bit 4 of the bidirectional Data bus.
DATA I/O 3	71	A3	TTB	--	Bit 3 of the bidirectional Data bus.
DATA I/O 2	72	A2	TTB	--	Bit 2 of the bidirectional Data bus.
DATA I/O 1	73	B3	TTB	--	Bit 1 of the bidirectional Data bus.
DATA I/O 0	74	A1	TTB	--	Bit 0 (LSB) of the bidirectional Data bus.

INPUT ADDRESS BUS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
ADDR IN 10	75	B2	TI	--	Bit 10 (MSB) of the Address Input bus.
ADDR IN 9	77	B1	TI	--	Bit 9 of the Address Input bus.
ADDR IN 8	79	D2	TI	--	Bit 8 of the Address Input bus.
ADDR IN 7	81	F2	TI	--	Bit 7 of the Address Input bus.
ADDR IN 6	83	E1	TI	--	Bit 6 of the Address Input bus.
ADDR IN 5	1	F3	TI	--	Bit 5 of the Address Input bus.
ADDR IN 4	3	G1	TI	--	Bit 4 of the Address Input bus.
ADDR IN 3	5	G3	TI	--	Bit 3 of the Address Input bus.
ADDR IN 2	7	H2	TI	--	Bit 2 of the Address Input bus.
ADDR IN 1	9	K1	TI	--	Bit 1 of the Address Input bus.
ADDR IN 0	13	K3	TI	--	Bit 0 (LSB) of the Address Input bus.

OUTPUT ADDRESS BUS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
ADDR OUT 10	76	C2	TTO	--	Bit 10 (MSB) of the Address Output bus.
ADDR OUT 9	78	C1	TTO	--	Bit 9 of the Address Output bus.
ADDR OUT 8	80	D1	TTO	--	Bit 8 of the Address Output bus.
ADDR OUT 7	82	E2	TTO	--	Bit 7 of the Address Output bus.
ADDR OUT 6	84	E3	TTO	--	Bit 6 of the Address Output bus.
ADDR OUT 5	2	F1	TTO	--	Bit 5 of the Address Output bus.
ADDR OUT 4	4	G2	TTO	--	Bit 4 of the Address Output bus.
ADDR OUT 3	6	H1	TTO	--	Bit 3 of the Address Output bus.
ADDR OUT 2	8	J1	TTO	--	Bit 2 of the Address Output bus.
ADDR OUT 1	10	J2	TTO	--	Bit 1 of the Address Output bus.
ADDR OUT 0	11	L1	TTO	--	Bit 0 (LSB) of the Address Output bus.

REMOTE TERMINAL ADDRESS INPUTS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
TA4	56	B9	TUI	--	Remote Terminal Address bit 4 (MSB).
TA3	58	B8	TUI	--	Remote Terminal Address bit 3.
TA2	60	B7	TUI	--	Remote Terminal Address bit 2.
TA1	62	A7	TUI	--	Remote Terminal Address bit 1.
TA0	C6	64	TUI	--	Remote Terminal Address bit 0.
$\overline{\text{TALEN}}$/PARITY	52	C10	TUI	--	Remote Terminal Address Latch Enable/ Remote Terminal Parity Input. Function of input is defined by he state of pin EXT TEST and EXT TST CH SEL A/$\overline{\text{B}}$. For EXT TEST = 0, EXT TST CH SEL A/$\overline{\text{B}}$ = 1, $\overline{\text{TALEN}}$/PARITY must provide odd parity for the Remote Terminal Address. For all other states of EXT TEST and EXT TST CH SEL A/$\overline{\text{B}}$ (i.e., 00, 10, 11) $\overline{\text{TALEN}}$/PARITY functions as an active low address strobe.

;

MODE CODE/SUBADDRESS OUTPUTS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
$\overline{MC}$/SA	21	K6	TO	--	Mode Code/Subaddress Indicator. If $\overline{MC}$/SA is low, it indicates that the most recent command word is a mode code command. If $\overline{MC}$/SA is high, it indicates that the most recent command word is for a subaddress. This output indicates whether the mode code/subaddress outputs (i.e., MCSA(4:0)) contain mode code or sub-address information.
MCSA4 19	K5	TO	--		Mode Code/Subaddress 4. If $\overline{MC}$/SA is low, this pin represents the most significant bit of the the most recent command word (the MSB of the mode code). If $\overline{MC}$/SA is high, this pin represents the MSB of the subaddress.
MCSA3 18	J5	TO	--		Mode Code/Subaddress 3.
MCSA2 17	L4	TO	--		Mode Code/Subaddress 2.
MCSA1 16	K4	TO	--		Mode Code/Subaddress 1.
MCSA0 14	L2	TO	--		Mode Code/Subaddress 0. If $\overline{MC}$/SA is low, this pin represents the least significant bit of the the most recent command word. If $\overline{MC}$/SA is high, this pin represents the LSB of the sub-address

BIPHASE INPUTS

NAME	PIN NUMBER				DESCRIPTION
	LCC	PGA			
BIPHASE IN A Z	39	G9	TI	--	Receiver - Channel A, Zero Input. Idle low Manchester input from the 1553 bus transceiver.
BIPHASE IN A O	37	H10	TI	--	Receiver - Channel A, One Input. This input is thecomplement of BIPHASE IN A Z.
BIPHASE IN B Z	34	J10	TI	--	Receiver - Channel B, Zero Input. Idle low Manchester input from the 1553 bus transceiver.
BIPHASE IN B O	33	K10	TI	--	Receiver - Channel B, One Input. This input is the complement of BIPHASE IN B Z.

BIPHASE OUTPUTS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
BIPHASE OUT A Z	28	K8	TO	--	Transmitter - Channel A, Zero Output. This Manchester-encoded data output is connected to the 1553 bus transmitter input. The output is idle low.
BIPHASE OUT A O	27	L8	TO	--	Transmitter - Channel A, One Output. This output is the complement of BIPHASE OUT A Z. The output is idle low.
BIPHASE OUT B Z	30	L10	TO	--	Transmitter - Channel B, Zero Output. This Manchester-encoded data output is connected to the 1553 bus transmitter. The output is idle low.
BIPHASE OUT B O	32	L11	TO	--	Transmitter - Channel B, One Output. This output is the complement of BIPHASE OUT B Z. The output is idle low.

MASTER RESET AND CLOCK

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
$\overline{\text{MRST}}$	40	G10	TUI	AL	Master Reset. Initializes all internal functions of the RTI. $\overline{\text{MRST}}$ must be asserted 500 nanoseconds before normal RTI operation. (500ns minimum).
12MHz	35	K11	TI	--	12MHz Input Clock. This is the RTI system clock that requires an accuracy greater than 0.01% with a duty cycle from 50% ±10%.
2MHz	24	L7	TO	--	2MHz Clock Output. This is a 2MHz output generated by the 12MHz input clock. This clock is stopped when $\overline{\text{MRST}}$ is low.

POWER AND GROUND

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
V_{DD}	54	B10	PWR	--	+5V_{DC}. Power supply must be +5V_{DC} ±10%.
V_{SS}	12 42	K2 F10	GND GND	-- --	Ground reference. Zero V_{DC} logic ground.

CONTROL PINS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
$\overline{CS}$	44	E9	TI	AL	Chip Select. Active low input for host access of transparent memory or the RTI internal registers. In the transparent memory configuration $\overline{CS}$ is propagated through the RTI to the $\overline{RCS}$ output.
$\overline{CTRL}$	50	C11	TI	AL	Control. The host processor uses the active low $\overline{CTRL}$ input signal in conjunction with $\overline{CS}$ and RD/$\overline{WR}$ to access the RTI internal registers. $\overline{CTRL}$ is also used in the software assignment of the terminal address and programmed reset.
$\overline{ADOEN}$	15	L3	TI	AL	Address Output Enable. When $\overline{ADOEN}$ is low the Address Out bus (ADDR OUT (15:0)) is active. If $\overline{ADOEN}$ = 1 the Address Out bus is high impedance.
RD/$\overline{WR}$	46	E10	TI	--	Read/Write. The host processor uses a high level on this input in conjunction with $\overline{CS}$ and $\overline{CTRL}$ to read the RTI internal registers. A low level on this input is used in conjunction with $\overline{CS}$ and $\overline{CTRL}$ to write to internal RTI registers. In the transparent memory configuration RD/$\overline{WR}$ is propagated through the RTI to the RRD/$\overline{RWR}$ output.
$\overline{BCEN}$	25	K7	TUI	AL	Broadcast Enable. Active low input enables broadcast commands.
ILL COMM	20	L5	TDI	AH	Illegal Command. The host processor uses the ILL COMM input to inform the RTI that the present command is illegal. ILL COMM is used in conjunction with MCSA(4:0) and $\overline{MC}$/SA to define system dependent illegal commands.

STATUS OUTPUTS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
$\overline{RCS}$	43	F9	TO	AL	RAM Chip Select. Active low output used to enable memory for access.
RRD/$\overline{RWR}$	45	E11	TO	--	RAM Read/Write. High output enables memory read, low output enables memory write, used in conjunction with $\overline{RCS}$). Normally high output.
$\overline{COMSTR}$	22	J6	TO	AL	Command Strobe. $\overline{COMSTR}$ is an active low output of 500ns duration identifying receipt of a valid command.
$\overline{TIMERON}$	41	G11	TO	AL	Fail-safe Timer. The $\overline{TIMERON}$ output pulses low for 730ms when the RTI begins transmitting (i.e., rising edge of STATUS) to provide a fail-safe timer meeting the requirements of MIL-STD-1553B. This pulse is reset when $\overline{COMSTR}$ goes low or during Master Reset. in the external self-test mode $\overline{TIMERON}$ does not recognize $\overline{COMSTR}$ and resets after 730ms.
MES ERR	49	D10	TO	AH	Message Error. The active high MES ERR output signals that the Message Error bit in the Status Register has been set due to receipt of an invalid command or an error during message sequence. MES ERR will reset to logic zero on receipt of next valid command.
CH A/$\overline{B}$	26	L6	TO	--	Channel A/$\overline{B}$. Output identifying the channel on which the most recent valid command was received. Channel A = 1, Channel B = 0.
$\overline{XMIT}$	38	H11	TO	AL	Transmit. Active low output identifies a transmit command message transfer by the RTI is in progress.
$\overline{RCV}$	51	B11	TO	AL	Receive. Active low output identifies a receive command message transfer by the RTI is in progress.
$\overline{BRDCST}$	36	J11	TO	AL	Broadcast. $\overline{BRDCST}$ is an active low output that identifies receipt of a valid broadcast command.
STATUS	23	J7	TO	AH	Status. Active high output pulse indicating that the RTI is in the process of transmitting a status word.

BUS ARBITRATION

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
DMARQ	47	F11	TO	AH	Direct Memory Access Request. Active high output requesting RTI access to memory.
$\overline{\text{MEMCK}}$	48	D11	TI	AL	Memory Clock (DMA Grant). Active low input signaling the RTI that a memory access is granted. Internal to the RTI, receipt of $\overline{\text{MEMCK}}$ generates RAM chip select and RAM read/write signals.
EXT TST	29	L9	TDI	--	External Self-test Enable. Multi-function input pin. In self-test mode forcing this pin high allows the monitoring of self-test activity at the bus stub. When the RTI is not in self-test this pin defines the function of $\overline{\text{TALEN}}$/PARITY.
EXT TST CH SEL A/$\overline{\text{B}}$	31	K9	TUI	--	External Self-test Channel Select. A/$\overline{\text{B}}$ Multi-function input pin. In self-test mode forcing this pin high selects the channel on which the self-test is performed (Channel A = 1, Channel B = 0). When the RTI is not in self-test this pin defines the function of $\overline{\text{TALEN}}$/PARITY.

4.0 OPERATING CONDITIONS

ABSOLUTE MAXIMUM RATINGS [1]
(referenced to VSS)

SYMBOL	PARAMETER	LIMITS	UNIT
V_{DD}	DC supply voltage	-0.3 to +7.0	V
V_{IO}	Voltage on any pin	-0.3 to V_{DD}+0.3	V
I_I	DC input current	±10	mA
T_{STG}	Storage temperature	-65 to +150	°C
P_D	Maximum power dissipation	300	mW
T_J	Maximum junction temperature	+175	°C
Θ_{JC}	Thermal resistance, junction-to-case	20	°C/W

Note:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

SYMBOL	PARAMETER	LIMITS	UNIT
V_{DD}	DC supply voltage	4.5 to 5.5	V
V_{IN}	DC input voltage	0 to V_{DD}	V
T_C	Temperature range	-55 to +125	°C
F_O	Operating frequency	12 ± .01%	MHz

5.0 DC ELECTRICAL CHARACTERISTICS

(VDD = 5.0V ± 10%; -55°C < TC < +125°C)

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
V_{IL}	Low-level input voltage			0.8	V
V_{IH}	High-level input voltage		2.0		V
I_{IN}	Input leakage current TTL inputs Inputs with pull-down resistors Inputs with pull-up resistors	 $V_{IN} = V_{DD}$ or V_{SS} $V_{IN} = V_{DD}$ $V_{IN} = V_{SS}$	 -10 110 -2750	 10 2750 -110	 µA µA µA
V_{OL}	Low-level output voltage	I_{OL} = 4mA		0.4	V
V_{OH}	High-level output voltage	I_{OH} = -400µA	2.4		V
I_{OZ}	Three-state output leakage current	$V_O = V_{DD}$ or V_{SS}	-10	+10	µA
I_{OS}	Short-circuit output current [1, 2]	V_{DD} = 5.5V, $V_O = V_{DD}$ V_{DD} = 5.5V, V_O = 0V	 -90	90	mA mA
C_{IN}	Input capacitance [3]	*f* = 1MHz @ 0V		10	pF
C_{OUT}	Output capacitance [3]	*f* = 1MHz @ 0V		15	pF
C_{IO}	Bidirect I/O capacitance [3]	*f* = 1MHz @ 0V		25	pF
I_{DD}	Average operating current [1, 4]	*f* = 12MHz, CL = 50pF		50	mA
QI_{DD}	Quiescent current	Note 5		1.5	mA

Notes:

1. Supplied as a design limit but not guaranteed or tested.
2. Not more than one output may be shorted at a time for a maximum duration of one second.
3. Measured only for initial qualification, and after process or design changes that could affect input/output capacitance.
4. Includes current through input pull-ups. Instantaneous surge currents on the order of 1 ampere can occur during output switching. Voltage supply should be adequately sized and decoupled to handle a large surge current.
5. All inputs with internal pull-ups or pull-downs should be left open circuit. All other inputs tied high or low.

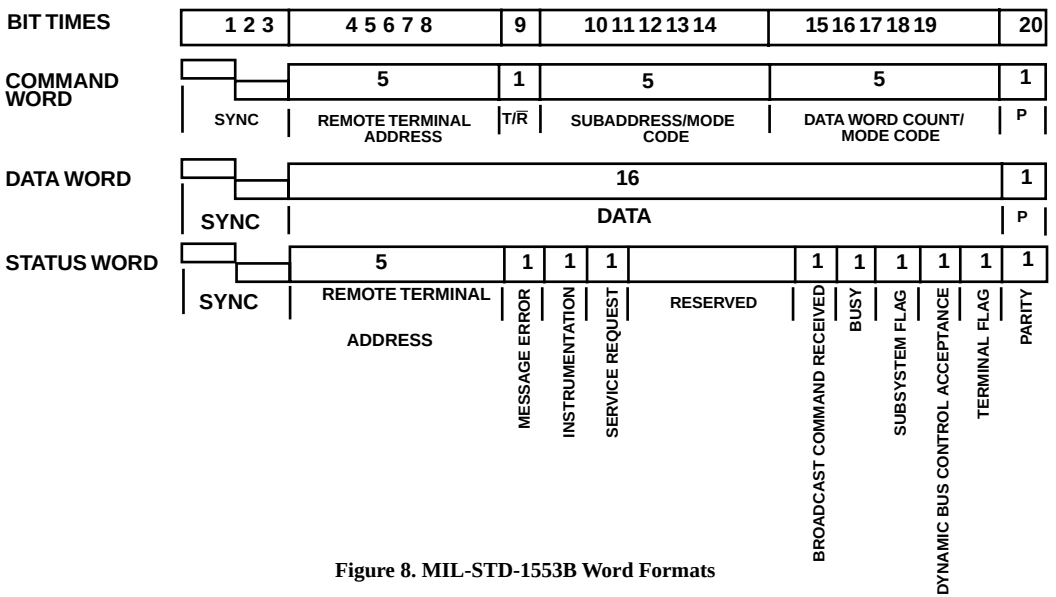
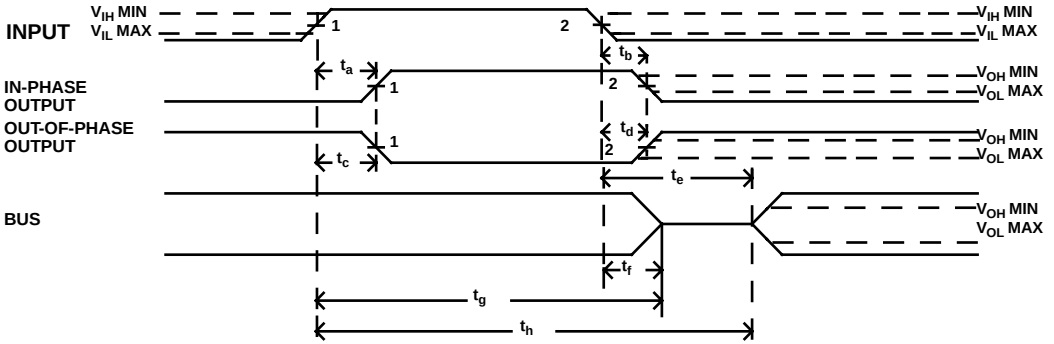


Figure 8. MIL-STD-1553B Word Formats

6.0 AC ELECTRICAL CHARACTERISTICS [3, 4]

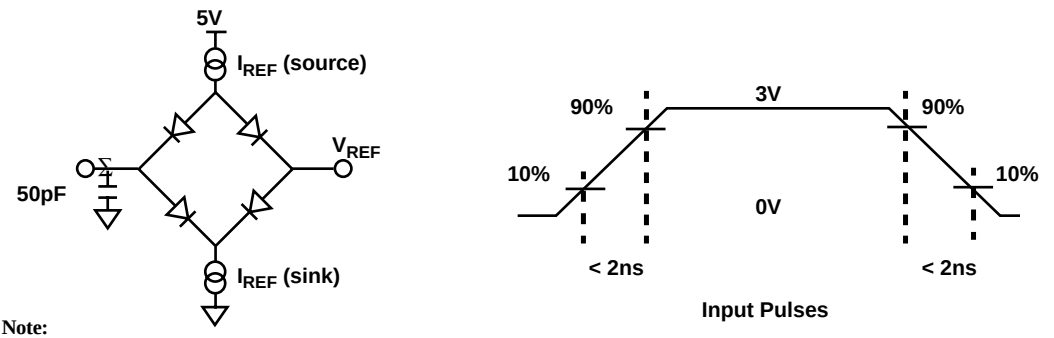
(Over recommended operating conditions)



SYMBOL	PARAMETER
t_a	INPUT↑ to response↑
t_b	INPUT↓ to response↓
t_c	INPUT↑ to response↓
t_d	INPUT↓ to response↑
t_e	INPUT↓ to data valid
t_f	INPUT↓ to high Z
t_g	INPUT↑ to high Z
t_h	INPUT↑ to data valid

Notes:
1. Timing measurements made at (V_{IH} MIN + V_{IL} MAX)/2.
2. Timing measurements made at (V_{OL} MAX + V_{OH} MIN)/2.
3. Based on 50pF load.

Figure 9a. Typical Timing Measurements



Note:
30pF including scope probe and test socket

Figure 9b. AC Test Loads and Input Waveforms

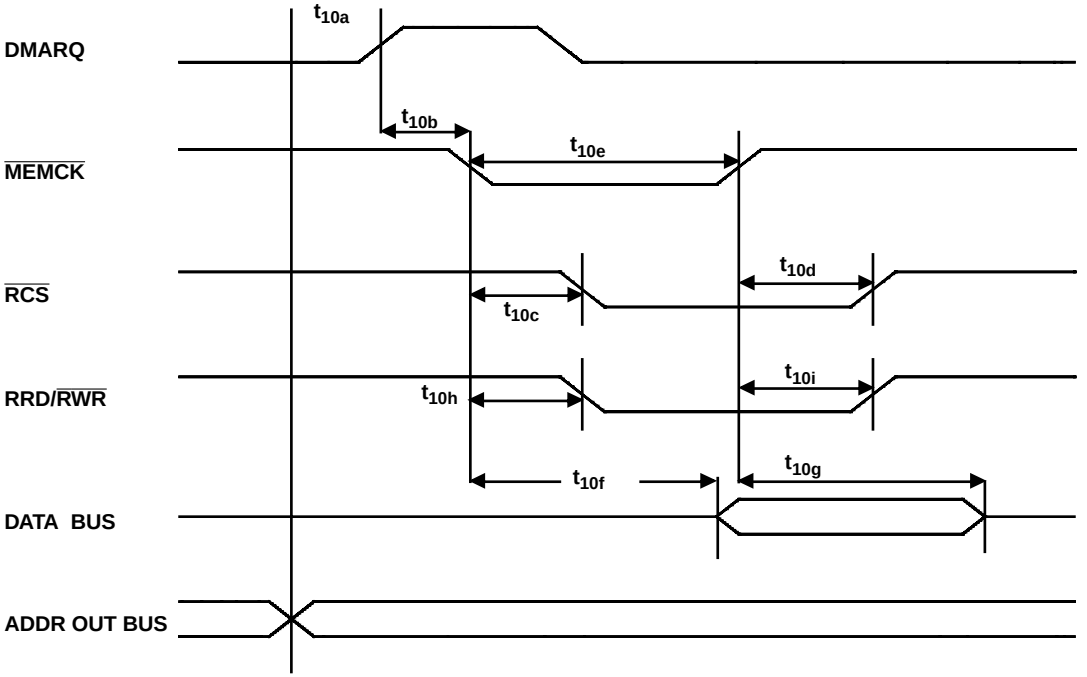


Figure 10. RTI Memory Write

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
t_{10a}	ADDR OUT valid to DMARQ active [3]	883	992	ns
t_{10b}	DMARQ active to $\overline{\text{MEMCK}}$ active [2, 3]	0	-	ns
t_{10c}	$\overline{\text{MEMCK}}$ active to $\overline{\text{RCS}}$ active [4]	-	67	ns
t_{10d}	$\overline{\text{MEMCK}}$ inactive to $\overline{\text{RCS}}$ inactive [4]	-	61	ns
t_{10e}	$\overline{\text{MEMCK}}$ pulse width [1, 2, 4]	83	-	ns
t_{10f}	$\overline{\text{MEMCK}}$ active to DATA bus valid [4]	-	115	ns
t_{10g}	$\overline{\text{MEMCK}}$ inactive to DATA bus high impedance [3]	5	101	ns
t_{10h}	$\overline{\text{MEMCK}}$ active to RRD/$\overline{\text{RWR}}$ active	-	61	ns
t_{10i}	$\overline{\text{MEMCK}}$ inactive to RRD/$\overline{\text{RWR}}$ inactive	-	58	ns

Notes:
1. Allows a 20ns data valid set-up time before $\overline{\text{RCS}}$ and RRD/$\overline{\text{RWR}}$ go high.
2. The sum $t_b + t_e$ must not exceed 18.8ms.
3. Supplied as a design limit, but not guaranteed or tested.
4. Guaranteed by test.

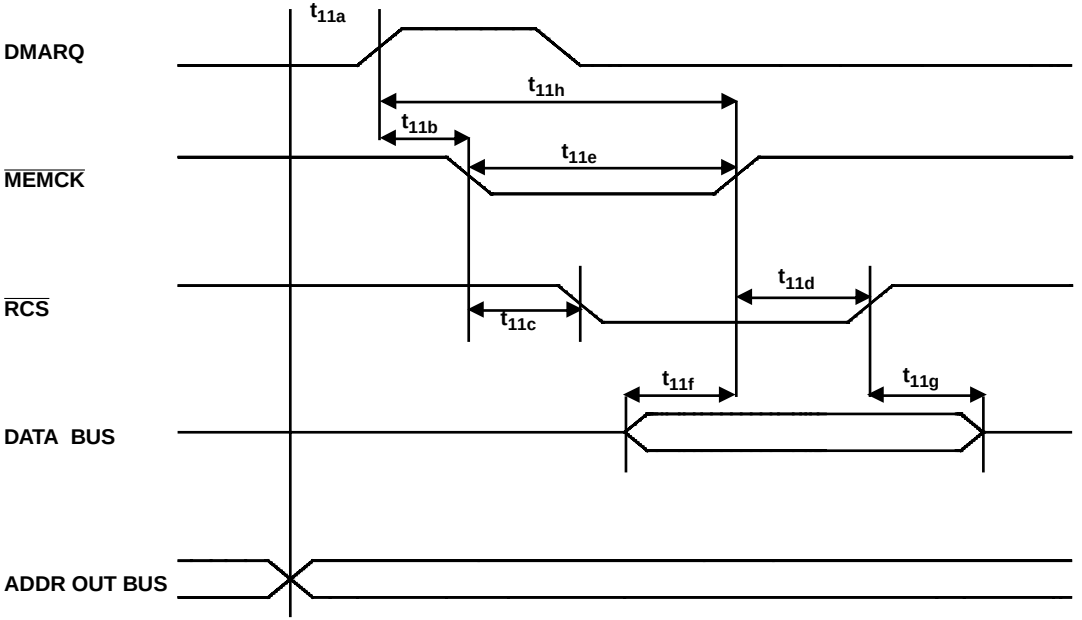


Figure 11. RTI Memory Read

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
t_{11a}	ADDR OUT valid to DMARQ active [3]	883	992	ns
t_{11b}	DMARQ active to $\overline{\text{MEMCK}}$ active [3]	0	14.9	µs
t_{11c}	$\overline{\text{MEMCK}}$ active to $\overline{\text{RCS}}$ active [4]	-	67	ns
t_{11d}	$\overline{\text{MEMCK}}$ inactive to $\overline{\text{RCS}}$ inactive [4]	-	61	ns
t_{11e}	$\overline{\text{MEMCK}}$ pulse width [1, 2, 4]	50	-	ns
t_{11f}	Input DATA valid to $\overline{\text{MEMCK}}$ inactive [4]	45	-	ns
t_{11g}	Input DATA valid after $\overline{\text{RCS}}$ inactive [4]	5	-	ns
t_{11h}	DMARQ active to $\overline{\text{MEMCK}}$ inactive [4]	-	18.3	µs

Notes:
1. Allows a 20ns data valid set-up time before $\overline{\text{RCS}}$ and RRD/$\overline{\text{RWR}}$ go high.
2. The sum $t_b + t_e$ must not exceed 18.8ms.
3. Supplied as a design limit, but not guaranteed or tested.
4. Guaranteed by test.

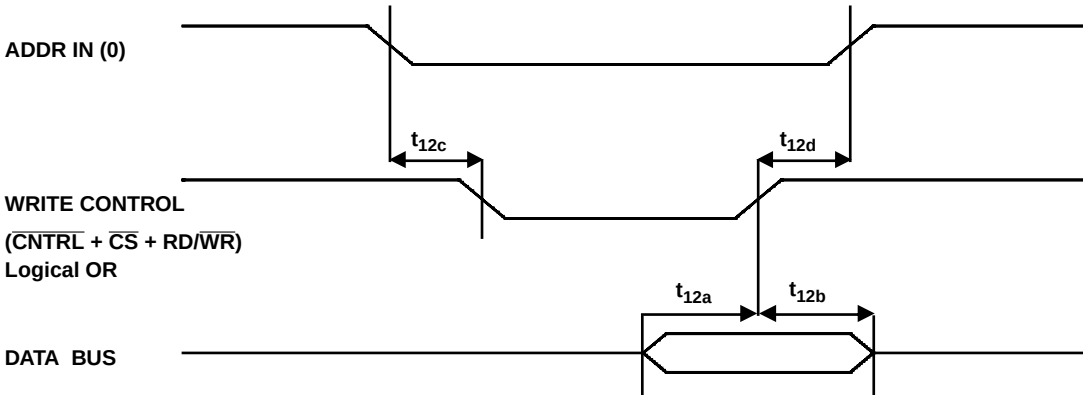


Figure 12. Control Register Write Timing

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
t_{12a}	Input DATA valid before WRITE CONTROL inactive (set-up time) [3]	20	-	ns
t_{12b}	Input DATA valid after WRITE CONTROL inactive (hold-time) [3]	25	-	ns
t_{12c}	ADDR IN valid before WRITE CONTROL asserts [1, 3]	20	-	ns
t_{12d}	ADDR IN valid after WRITE CONTROL negates [2, 3]	20	-	ns

Notes:
1. Set-up time required to prevent inadvertent software reset.
2. Hold-time required to prevent inadvertent software reset.
3. Guaranteed by test.

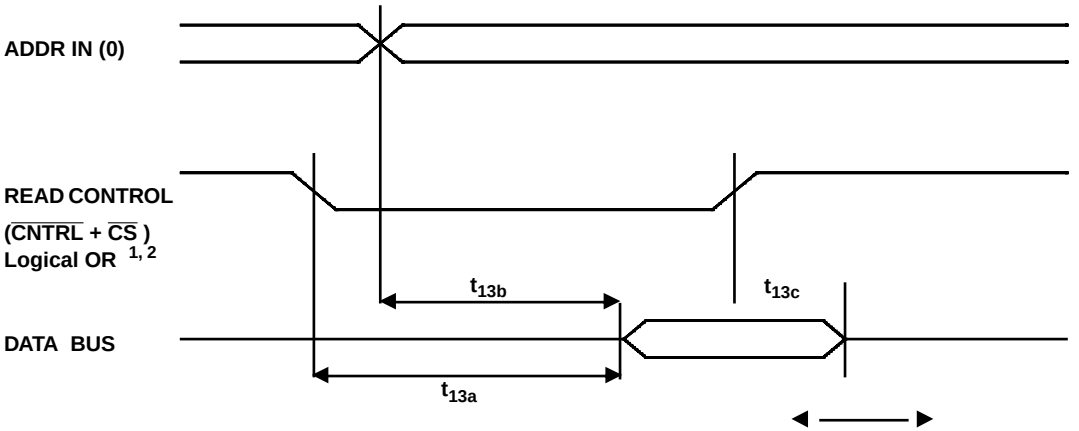


Figure 13. System and Last Command Register Read Timing

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
t_{13a}	DATA bus valid after READ CONTROL valid whilve ADDR IN (0) = 0 or 1	-	132	ns
t_{13b}	DATA bus valid after ADDR IN (0) = 0 or 1 while READ CONTROL = 0	-	70	ns
t_{13c}	READ CONTROL negation to DATA bus high impedance [3]	-	101	ns

Notes:
1. ADDR IN (0) = 0 System Register read.
2. ADDR IN (0) = 1 Last Command Register read.
3. Supplied as a design limit but not guaranteed or tested.

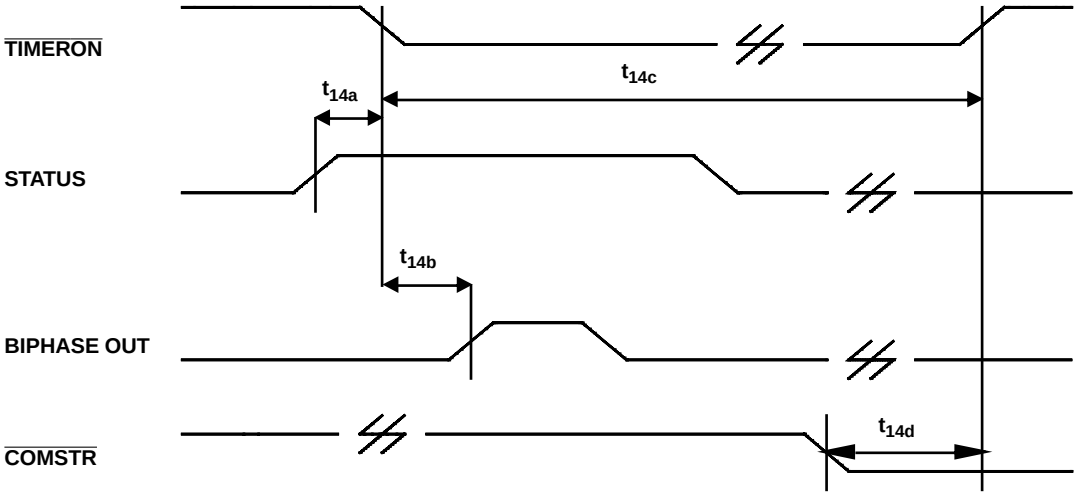


Figure 14. RT Fail-Safe Timer Signal Relationships

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
t_{14a}	STATUS active to $\overline{\text{TIMERON}}$ active [1]	4	31	ns
t_{14b}	$\overline{\text{TIMERON}}$ active to first BIPHASE OUT transition [1]	1.2	-	ms
t_{14c}	$\overline{\text{TIMERON}}$ low pulse width [1]	-	732	ms
t_{14d}	$\overline{\text{COMSTR}}$ active to $\overline{\text{TIMERON}}$ reset [1]	-	31	ns

Note:
1. Supplied as a design limit, but not guaranteed or tested.

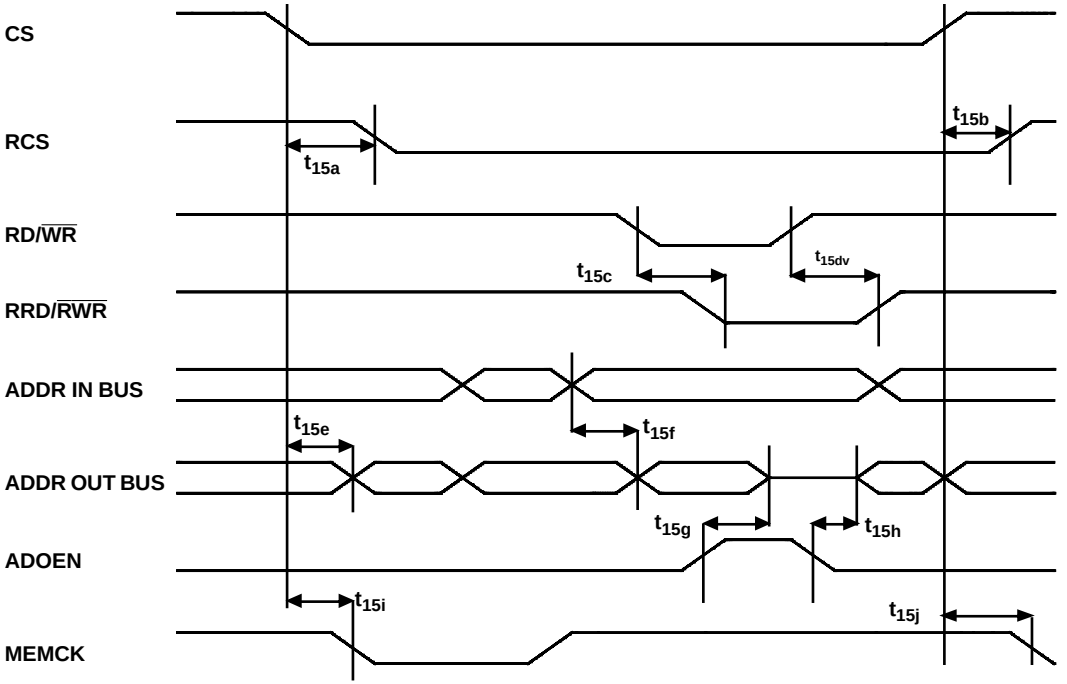


Figure 15. RTI Propagation Delays

SYM-	PARAMETER	MINIMUM	MAXIMUM	UNITS
t_{15a}	$\overline{CS}$ active to $\overline{RCS}$ active [2]	-	48	ns
t_{15b}	$\overline{CS}$ negation to $\overline{RCS}$ negation [2]	-	40	ns
t_{15c}	RD/$\overline{WR}$ active to RRD/$\overline{RWR}$ active [2]	-	45	ns
t_{15d}	RD/$\overline{WR}$ negation to RRD/$\overline{RWR}$ negation [2]	-	35	ns
t_{15e}	$\overline{CS}$ active to ADDR OUT valid [2]	6	52	ns
t_{15f}	ADDR IN valid to ADDR OUT valid [2]	-	44	ns
t_{15g}	$\overline{ADOEN}$ negation to ADDR OUT high impedance [1]	-	42	ns
t_{15h}	$\overline{ADOEN}$ active to ADDR OUT active [2]	6	50	ns
t_{15i}	$\overline{CS}$ active to $\overline{MEMCK}$ active (MEMCK not recognized) [1]	13	-	ns
t_{15j}	$\overline{CS}$ negation to $\overline{MEMCK}$ active (MEMCK recognized) [1]	10	-	ns

Note:
1. Supplied as a design limit, but not guaranteed or tested.
2. Guaranteed by test.

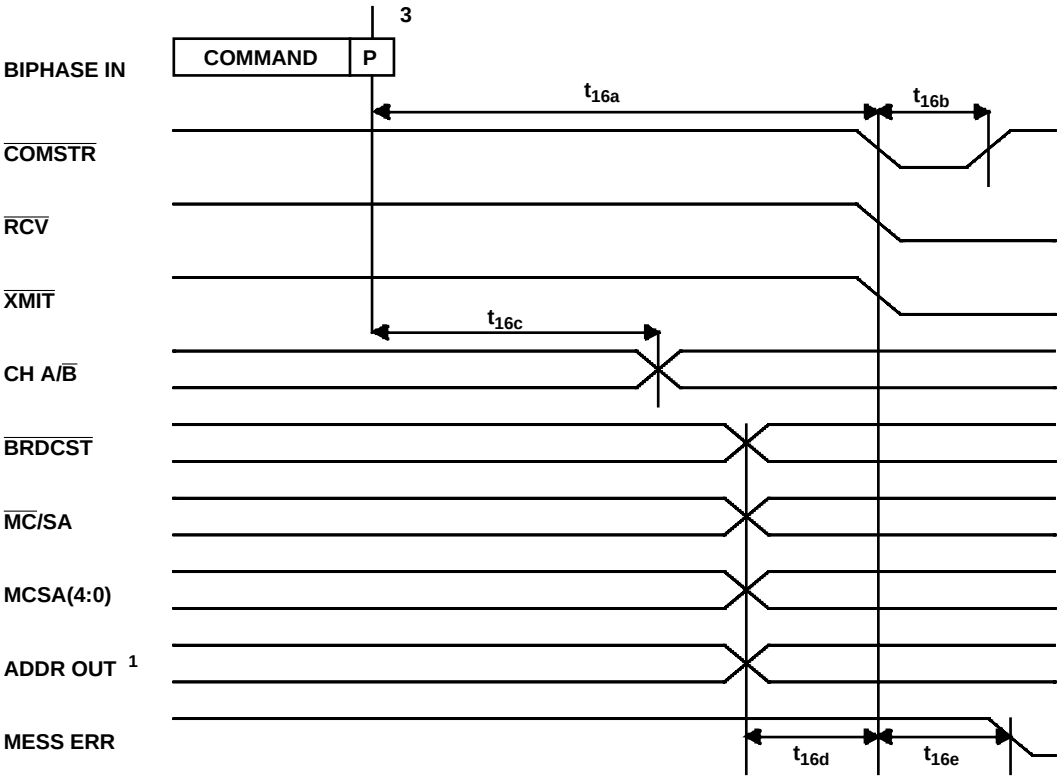


Figure 16. Command Word Validation

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
t_{16a}	Command word parity to $\overline{\text{COMSTR}}$ and RCV or XMIT active [4]	3.58	3.67	µs
t_{16b}	$\overline{\text{COMSTR}}$ pulse width [4]	499	502	ns
t_{16c}	Command word parity to CH A/$\overline{\text{B}}$ valid [4]	2.58	2.66	µs
t_{16d}	Status output signals valid to $\overline{\text{COMSTR}}$ active [2, 4]	430	-	ns
t_{16e}	MES ERR reset after $\overline{\text{COMSTR}}$ active [4]	745	750	ns

Notes:
1. $\overline{\text{ADOEN}}$ is asserted (i.e., logic low).
2. Status signals include $\overline{\text{BRDCST}}$, $\overline{\text{MC}}$/SA, MCSA(4:0), and ADDR OUT.
3. Measured from mid-bit parity crossing.
4. Supplied as a design limit, but not guaranteed or tested.

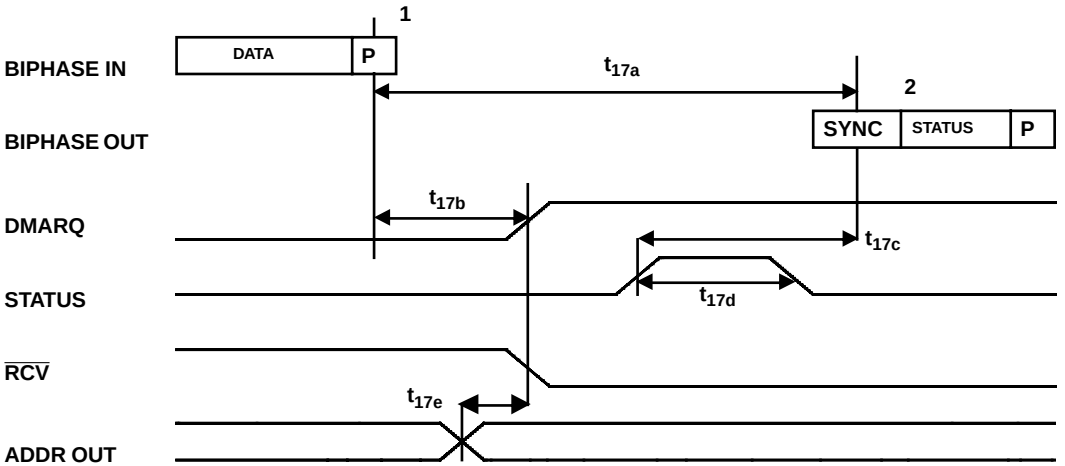


Figure 17. Receive Command Message Processing

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
t_{17a}	Data word parity bit to status word response [1,3]	8.80	9.37	µs
t_{17b}	Data word parity bit to DMARQ active [2,3]	3.58	3.68	µs
t_{17c}	STATUS active to BIPHASE OUT active [3]	1.24	1.25	µs
t_{17d}	STATUS pulse width [3]	4.48	4.98	µs
t_{17e}	ADDR OUT valid before DMARQ (H) [3]	0.90	-	µs

Notes:
1. Measured from last data word mid-bit parity crossing.
2. Measured from transmitted status word sync field mid-bit crossing.
3. Supplied as a design limit, but not guaranteed or tested.

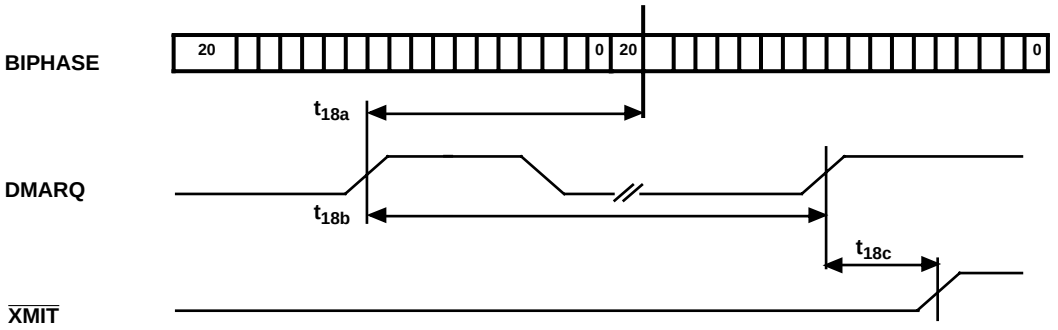


Figure 18. Transmitted Data Timing

SYM-	PARAMETER	MINIMUM	MAXIMUM	UNITS
* t_{18a}	DMARQ active to sync field of transmitted data word	17.15	17.18	µs
* t_{18b}	DMARQ active to DMARQ active	-	19.2	µs
* t_{18c}	$\overline{\text{XMIT}}$ negation after last DMARQ active	460	500	µs

Note:
* Supplied as a design limit but not guaranteed or tested.

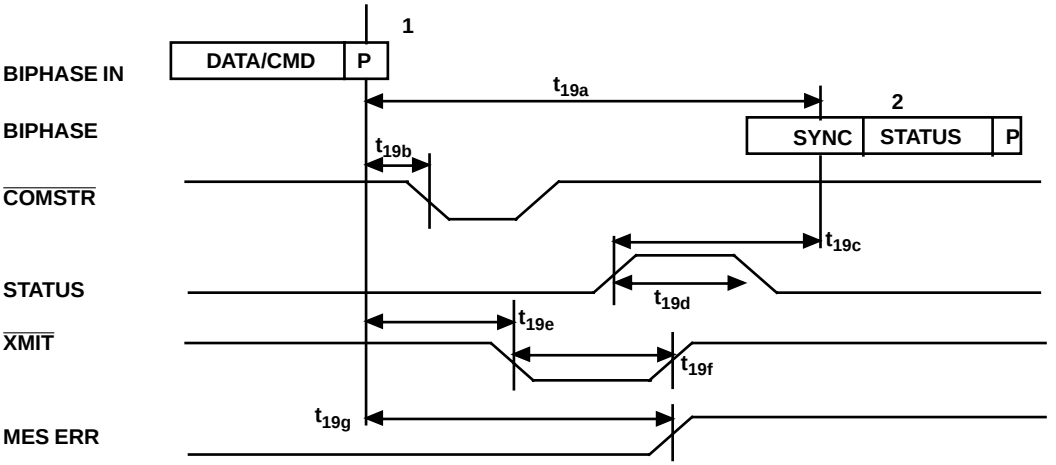


Figure 19. Mode Command Message Processing

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
* t_{19a}	Response time BIPHASE IN to BIPHASE OUT [2]	3.58	3.67	µs
* t_{19b}	Command word parity bit to $\overline{\text{COMSTR}}$ assertion [1]	8.80	9.37	µs
* t_{19c}	STATUS active to BIPHASE OUT active	1.24	1.25	µs
* t_{19d}	STATUS pulse width	4.48	4.98	µs
* t_{19e}	Command word parity bit to $\overline{\text{XMIT}}$ assertion	3.58	3.67	µs
* t_{19f}	$\overline{\text{XMIT}}$ pulse width for mode code reception	1.00	-	µs
* t_{19g}	Command word parity bit to MES ERR assertion	6.57	6.68	µs

Notes:
1. Measured from data or command word mid-bit parity crossing.
2. Measured from transmitted status word sync field mid-bit crossing.
* Supplied as a design limit but not guaranteed or tested.

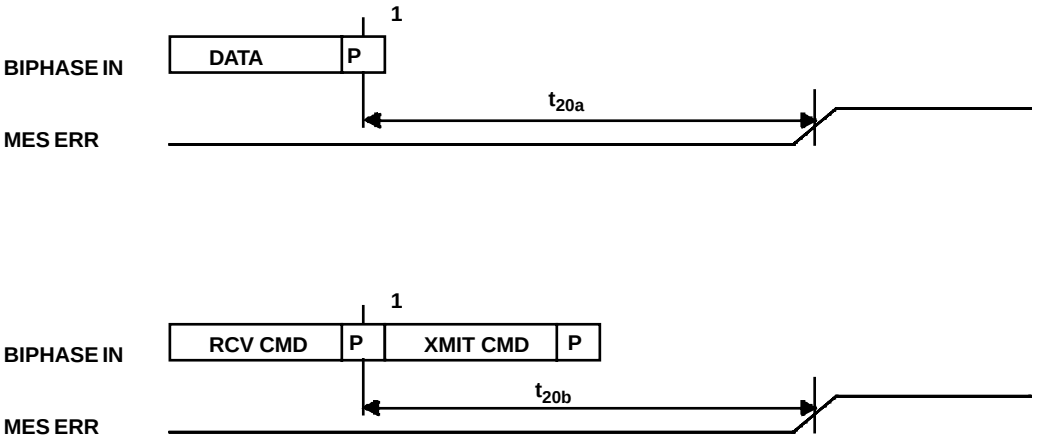


Figure 20. Message Error

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
* t_{20a}	Data word parity bit to MES ERR assertion [1]	23.50	23.63	µs
* t_{20b}	Command word parity bit to MES ERR assertion RT to RT transfer [2]	55.4	55.5	µs

Notes:
1. Measured from last data word mid-bit parity crossing.
2. No response from transmitter.

* Supplied as a design limit but not guaranteed or tested.

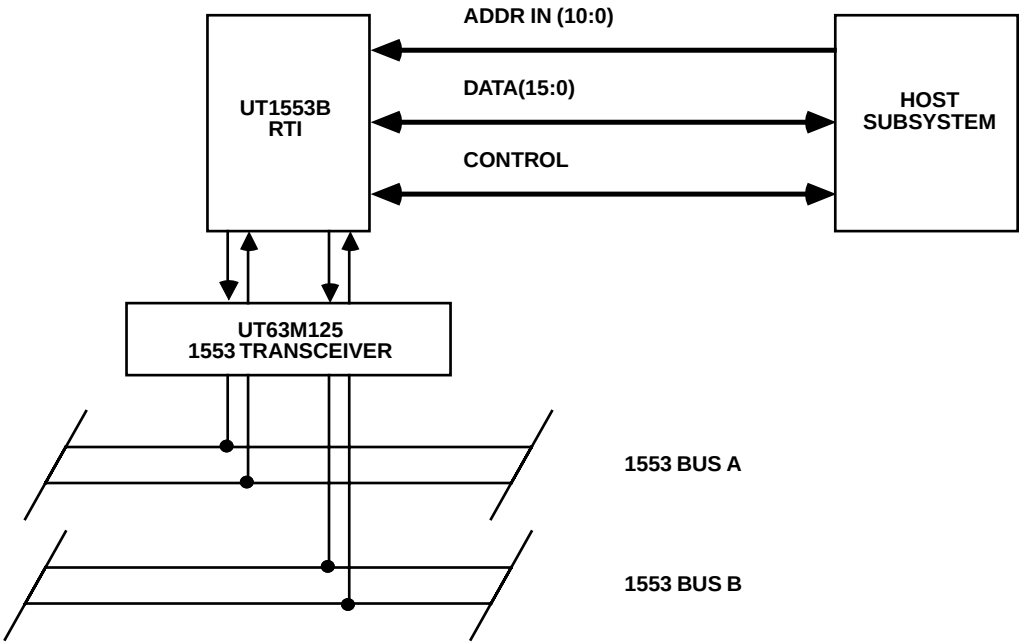


Figure 21. RTI General System Diagram (Idle low interface)

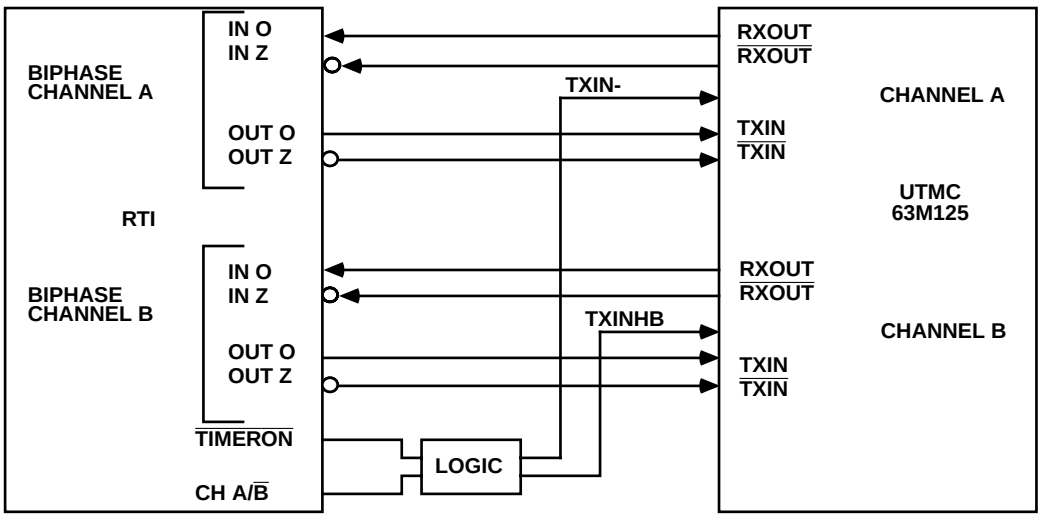


Figure 22. RTI Transceiver Interface Diagram

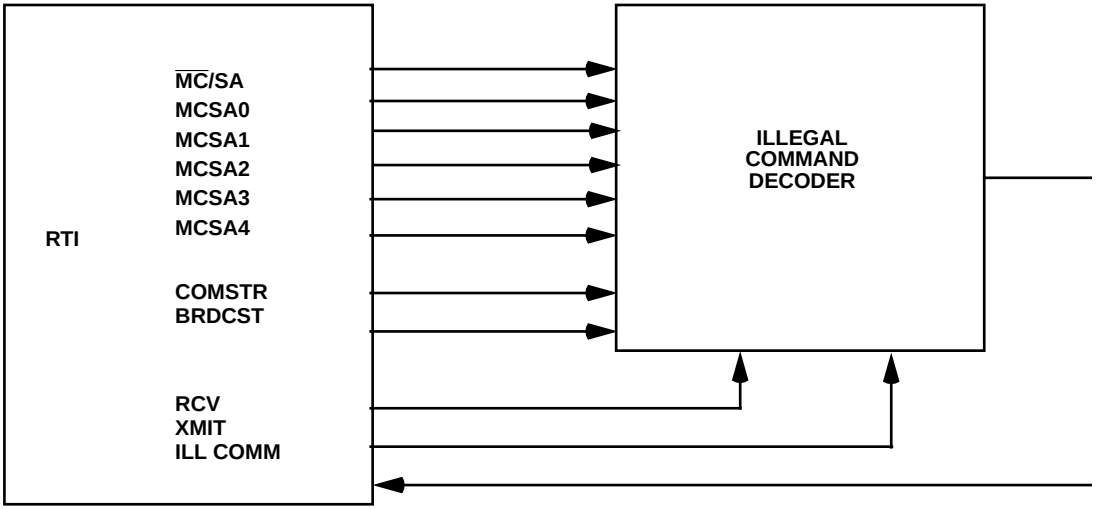


Figure 23. Mode Code/Subaddress Illegalization Circuit

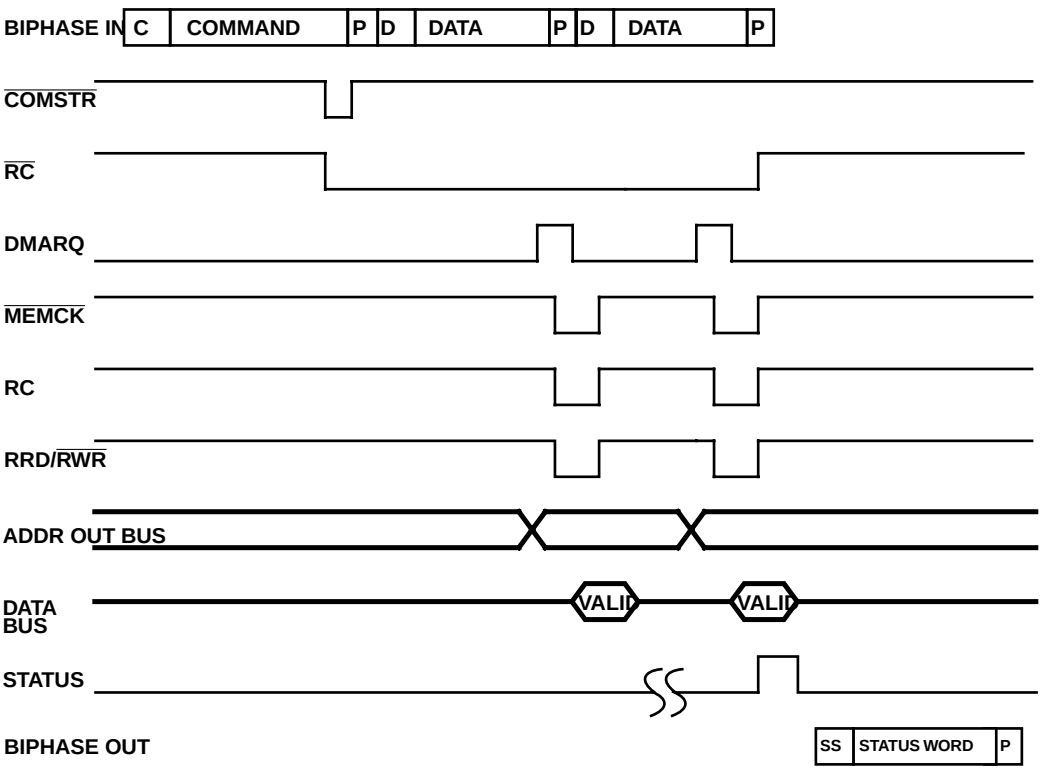


Figure 24. Receive Command with Two Data Words

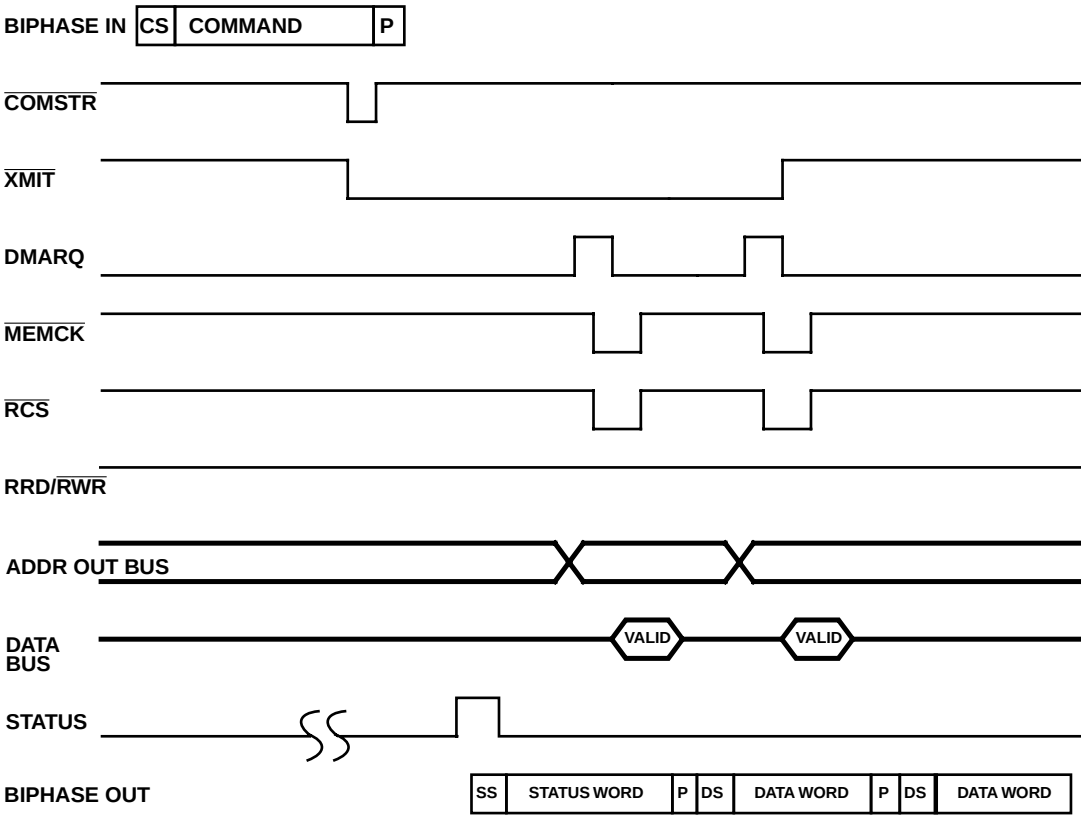
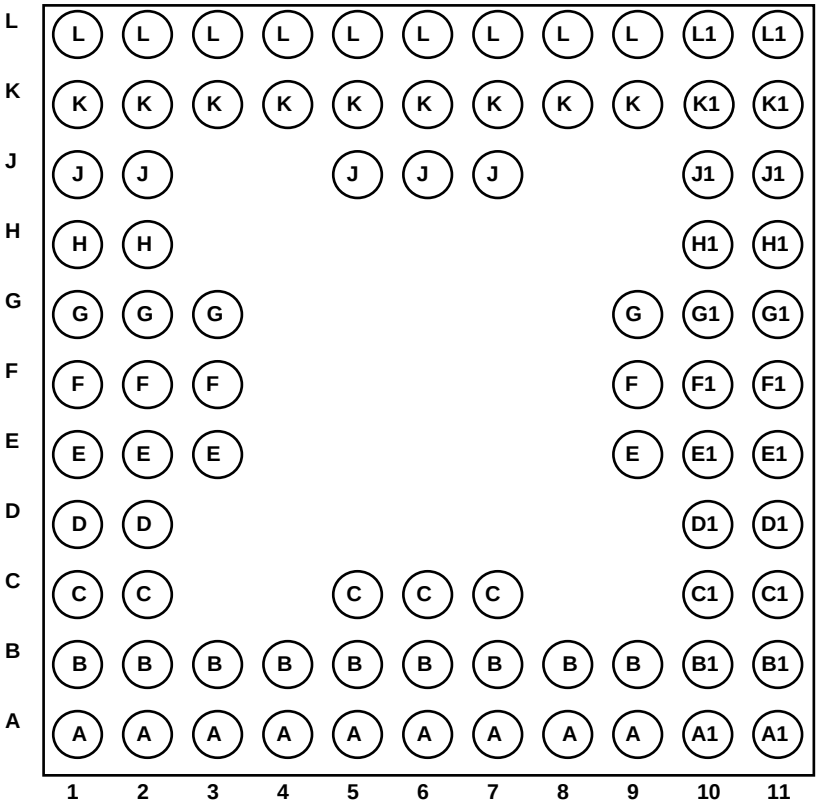


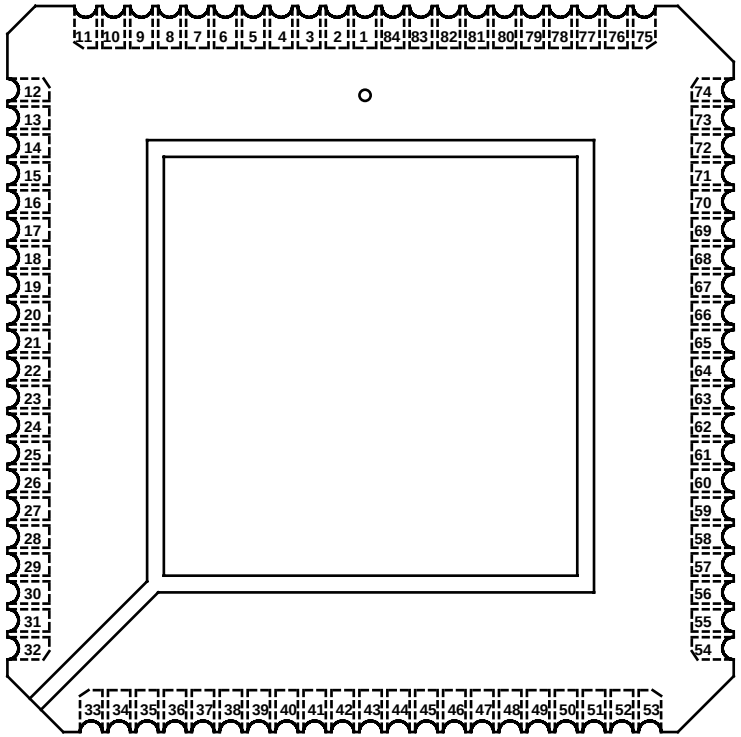
Figure 25. Transmit Command with Two Data Words

PACKAGE OUTLINE DRAWINGS



A1	DATA I/O 0	C1	ADDR OUT 9	F1	ADDR OUT 5	J1	ADDR OUT 2	L1	ADDR OUT 0
A2	DATA I/O 2	C2	ADDR OUT 10	F2	ADDR IN 7	J2	ADDR OUT 1	L2	MCSA 0
A3	DATA I/O 3	C5	DATA I/O 6	F3	ADDR IN 5	J5	MCSA 3	L3	ADOEN
A4	DATA I/O 5	C6	TA 0	F9	RCS	J6	COMSTR	L4	MCSA 2
A5	DATA I/O 8	C7	DATA I/O 10	F10	V_{SS}	J7	STATUS	L5	ILL COMM
A6	DATA I/O 9	C10	TALEN/PARITY	F11	DMARQ	J10	BIPHASE IN B Z	L6	CH A/B
A7	TA 1	C11	CTRL			J11	BRDCST	L7	2MHz
A8	DATA I/O 12			G1	ADDR IN 4			L8	BIPHASE OUT A
A9	DATA I/O 13	D1	ADDR OUT 8	G2	ADDR OUT 4	K1	ADDR IN 1	L9	EXT TEST
A10	DATA I/O 14	D2	ADDR IN 8	G3	ADDR IN 3	K2	V_{SS}	L10	BIPHASE OUT B
A11	DATA I/O 15	D10	MES ERR	G9	BIPHASE IN A Z	K3	ADDR IN 0	L11	BIPHASE OUT B
		D11	MEMCK	G10	MRST	K4	MCSA 1		
B1	ADDR IN 9			G11	TIMERON	K5	MCSA 4		
B2	ADDR IN 10	E1	ADDR IN 6			K6	MC/SA		
B3	DATA I/O 1	E2	ADDR OUT 7	H1	ADDR OUT 3	K7	BCEN		
B4	DATA I/O 4	E3	ADDR OUT 6	H2	ADDR IN 2	K8	BIPHASE OUT A Z		
B5	DATA I/O 7	E9	CS	H10	BIPHASE IN A O	K9	EXT TST CH SEI A/B		
B6	DATA I/O 11	E10	RD/WR	H11	XMIT	K10	BIPHASE IN B O		
B7	TA 2	E11	RRD/RWR			K11	12MHz		
B8	TA 3								
B9	TA 4								
B10	V_{DD}								
B11	RCV								

Figure 26a. UT1553B RTI Pingrid Array Configuration
(Bottom View)



1	ADDR IN 5	19	MCSA 4	37	BIPHASE IN A O	55	DATA I/O 14	73	DATA I/O 1
2	ADDR OUT 5	20	ILL COMM	38	$\overline{\text{XMIT}}$	56	TA4	74	DATA I/O 0
3	ADDR IN 4	21	MC/SA	39	BIPHASE IN A Z	57	DATA I/O 13	75	ADDR IN 10
4	ADDR OUT 4	22	COMSTR	40	$\overline{\text{MRST}}$	58	TA3	76	ADDR OUT 10
5	ADDR IN 3	23	STATUS	41	$\overline{\text{TIMERON}}$	59	DATA I/O 12	77	ADDR IN 9
6	ADDR OUT 3	24	2MHz	42	V_{SS}	60	TA2	78	ADDR OUT 9
7	ADDR IN 2	25	BCEN	43	$\overline{\text{RCS}}$	61	DATA I/O 11	79	ADDR IN 8
8	ADDR OUT 2	26	CH A/B	44	$\overline{\text{CS}}$	62	TA1	80	ADDR OUT 8
9	ADDR IN 1	27	BIPHASE OUT A O	45	RRD/$\overline{\text{RWR}}$	63	DATA I/O 10	81	ADDR IN 7
10	ADDR OUT 1	28	BIPHASE OUT A Z	46	RD/$\overline{\text{WR}}$	64	TA0	82	ADDR OUT 7
11	ADDR OUT 0	29	EXT TEST	47	$\overline{\text{DMARQ}}$	65	DATA I/O 9	83	ADDR IN 6
12	V_{SS}	30	BIPHASE OUT B Z	48	$\overline{\text{MEMCK}}$	66	DATA I/O 8	84	ADDR OUT 6
13	ADDR IN 0	31	EXT TST CH SEL A/B	49	$\overline{\text{MES ERR}}$	67	DATA I/O 7		
14	MCSA0	32	BIPHASE OUT B O	50	$\overline{\text{CTRL}}$	68	DATA I/O 6		
15	ADOEN	33	BIPHASE IN B O	51	$\overline{\text{RCV}}$	69	DATA I/O 5		
16	MCSA1	34	BIPHASE IN B Z	52	TALEN/PARITY	70	DATA I/O 4		
17	MCSA2	35	$\overline{\text{12MHz}}$	53	DATA I/O 15	71	DATA I/O 3		
18	MCSA3	36	$\overline{\text{BRDCST}}$	54	V_{DD}	72	DATA I/O 2		

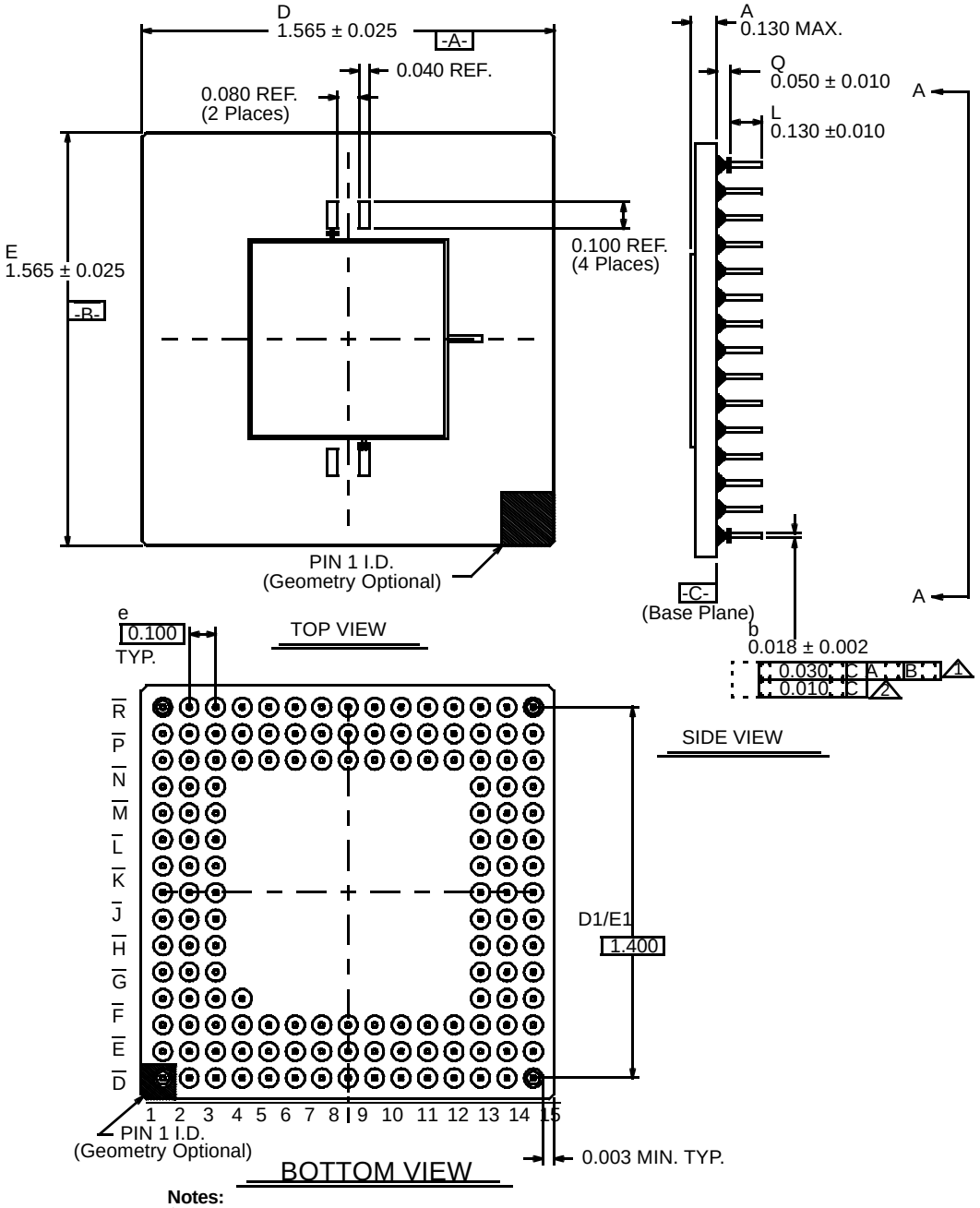
Figure 26b. UT1553B RTI Chip Carrier Configuration
(Top View)

Package Selection Guide

	Product							
	RTI	RTMP	RTR	BCRT	BCRTM	BCRTMP	RTS	XCVR
24-pin DIP (single cavity)								X
36-pin DIP (dual cavity)								X
68-pin PGA			X				X	
84-pin PGA	X	X		X	X[1]			
144-pin PGA						X		
84-lead LCC		X		X	X[1]			
36-lead FP (dual cavity) (50-mil ctr)								X
84-lead FP				X	X			
132-lead FP				X		X		

NOTE:

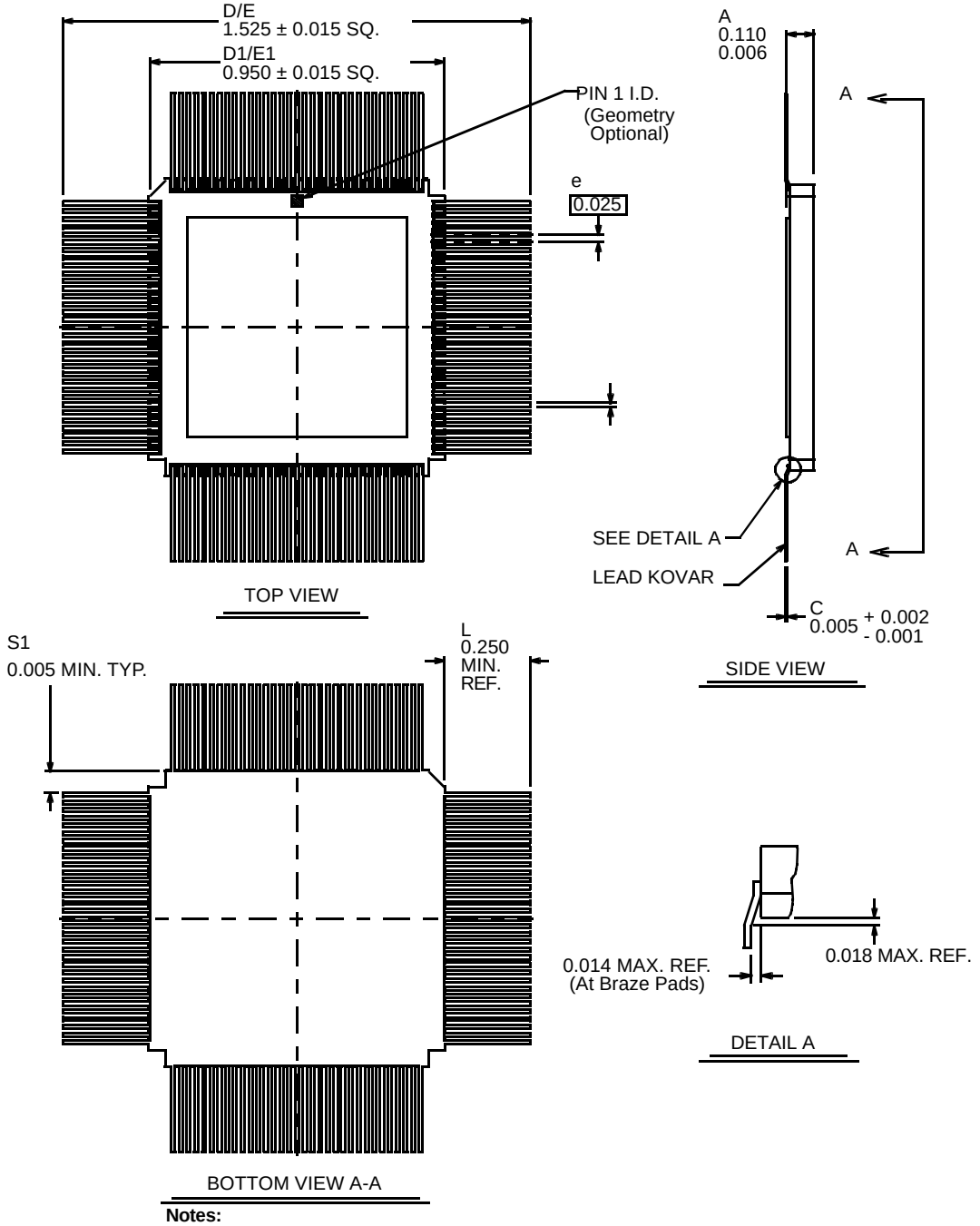
1. 84LCC package is not available radiation-hardened.



Notes:

1. True position applies to pins at base plane (datum C).
2. True position applies at pin tips.
3. All package finishes are per MIL-M-38510.
4. Letter designations are for cross-reference to MIL-M-38510.

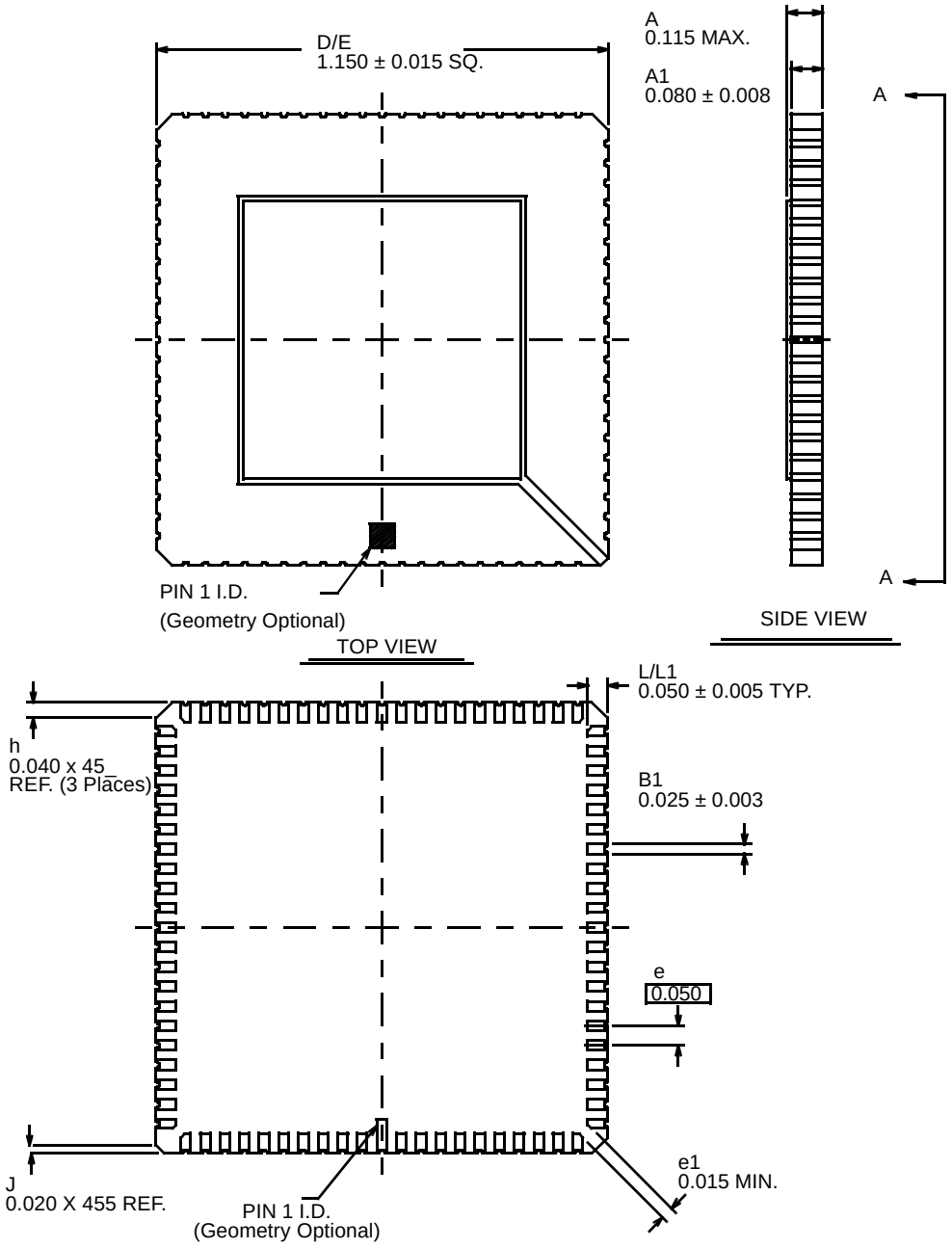
144-Pin Pingrid Array



Notes:

1. All package finishes are per MIL-M-38510.
2. Letter designations are for cross-reference to MIL-M-38510.

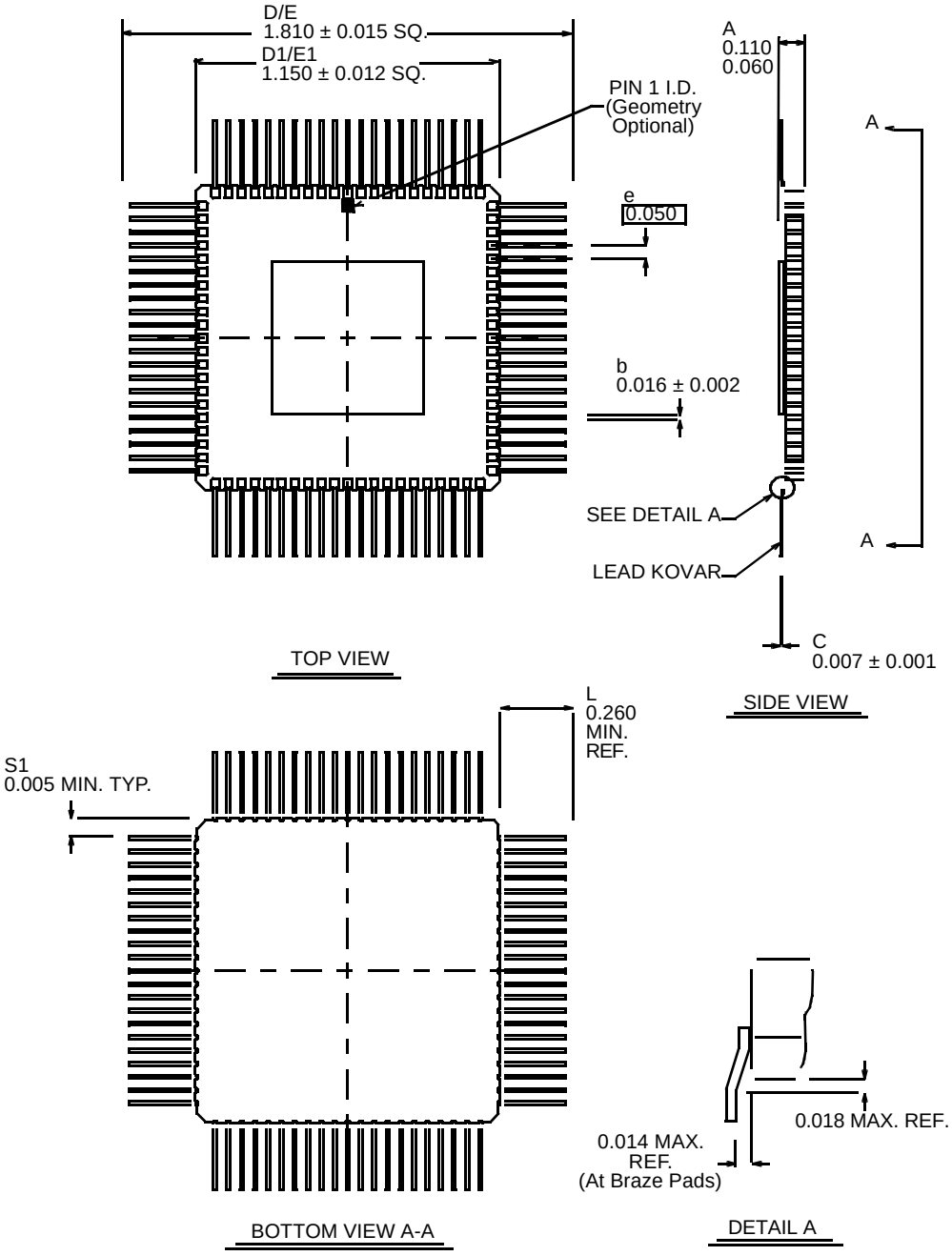
132-Lead Flatpack (25-MIL Lead Spacing)



Notes:

1. All package finishes are per MIL-M-38510.
2. Letter designations are for cross-reference to MIL-M-38510.

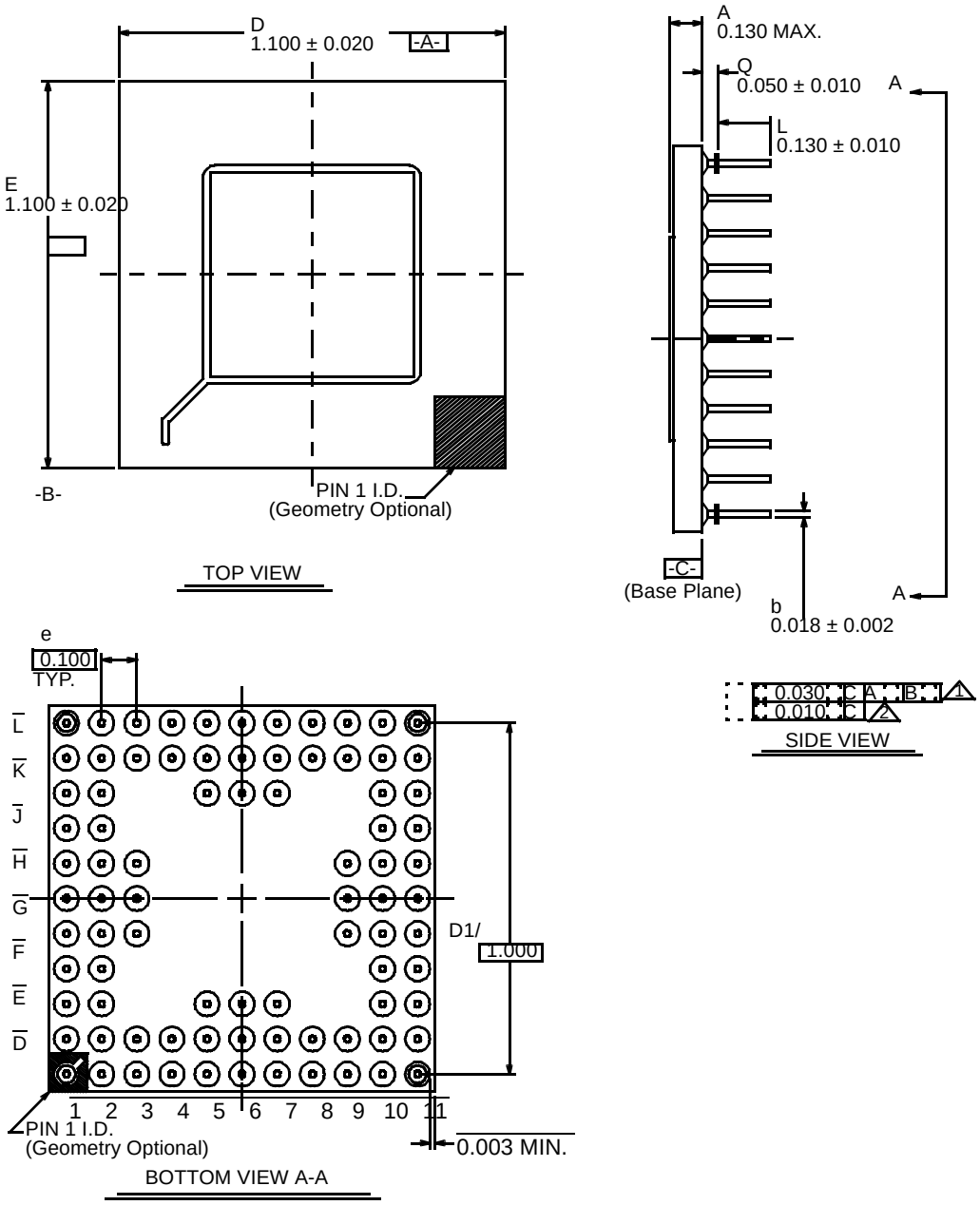
84-LCC



Notes:

1. All package finishes are per MIL-M-38510.
2. Letter designations are for cross-reference to MIL-M-38510.

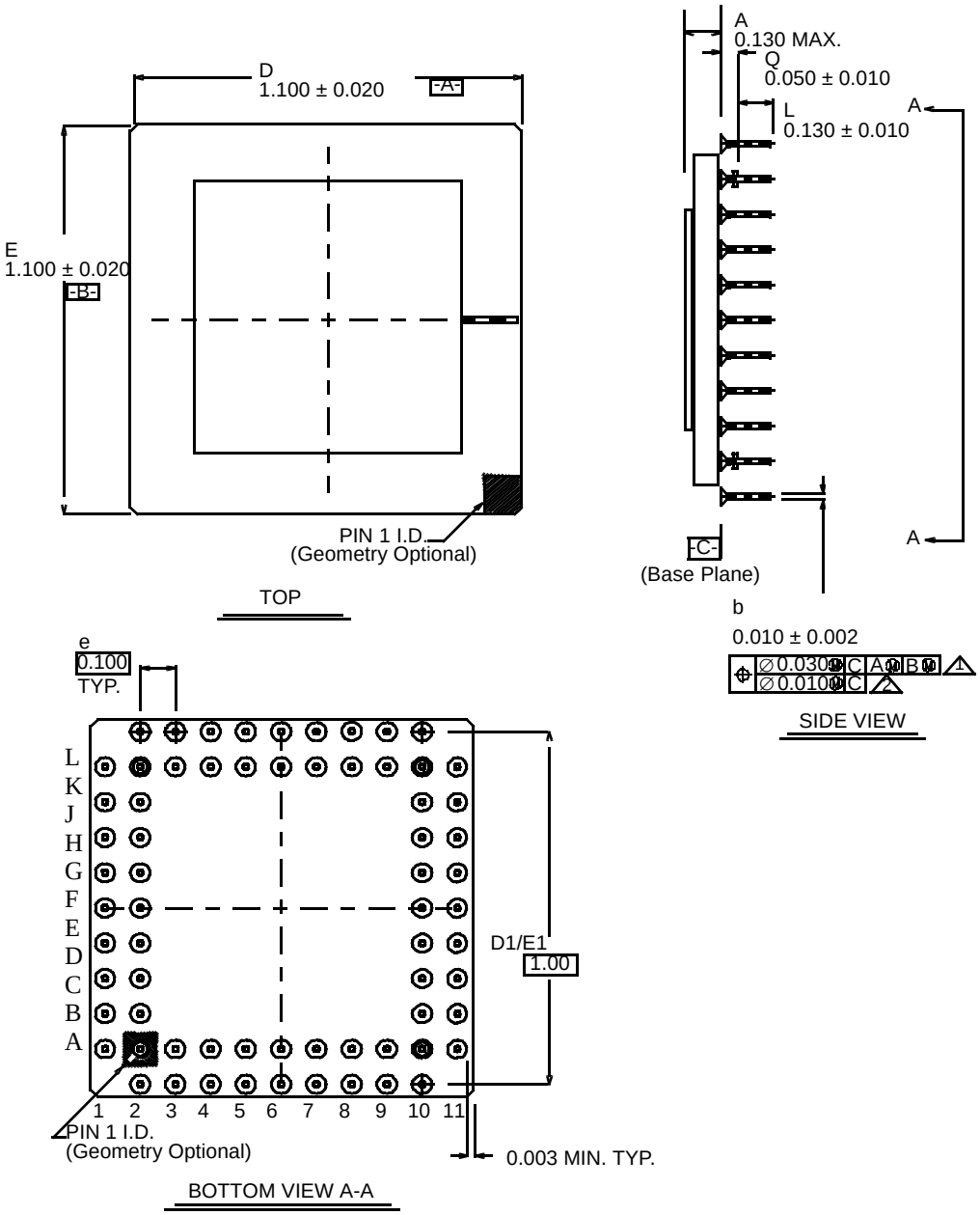
84-Lead Flatpack (50-MIL Lead Spacing)



Notes:

1. True position applies to pins at base plane (datum C).
2. True position applies at pin tips.
3. All packages finishes are per MIL-M-38510.
4. Letter designations are for cross-reference to MIL-M-38510.

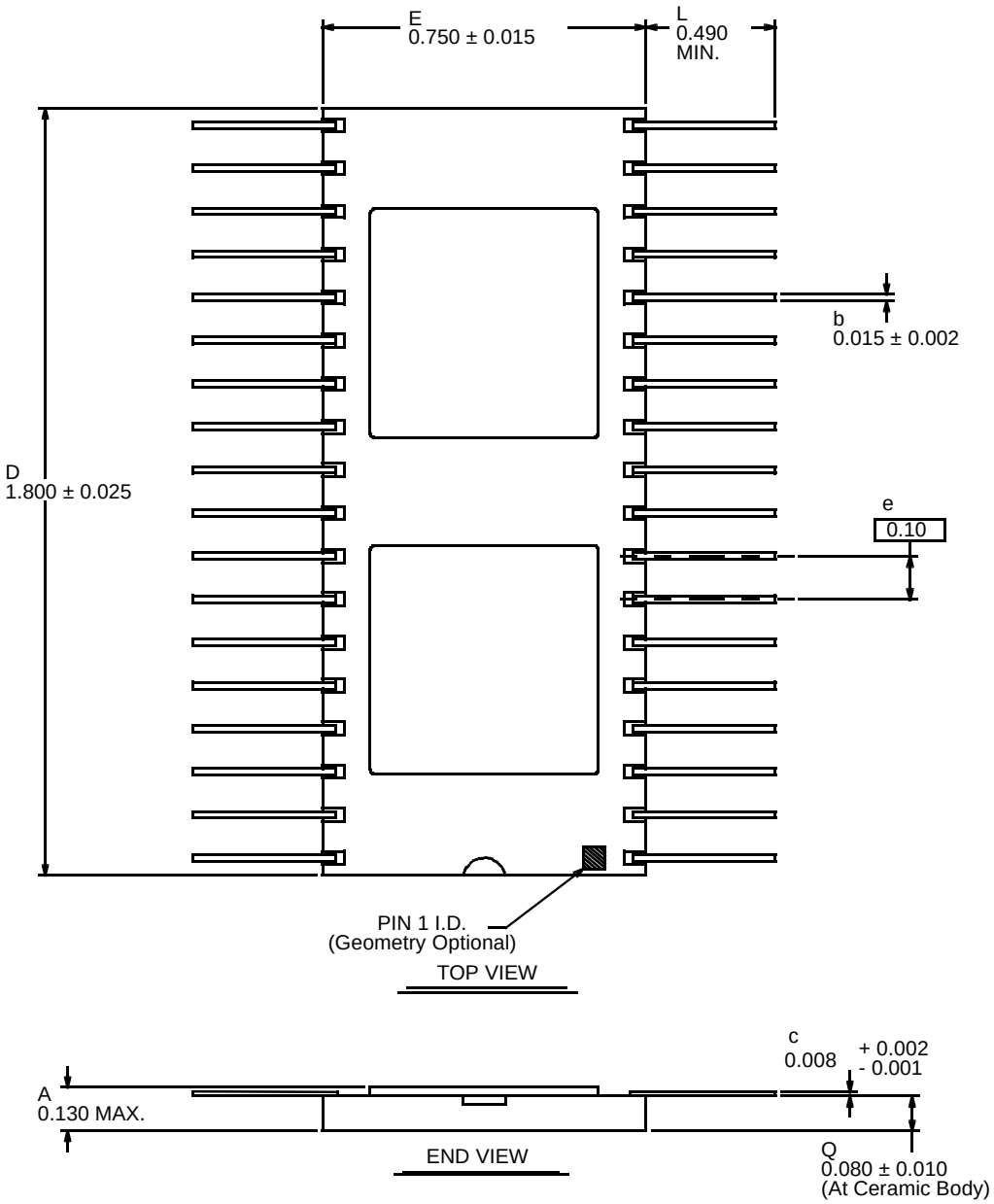
84-Pin Pingrid Array



Notes:

1. True position applies to pins at base plane (datum C).
2. True position applies at pin tips.
3. All packages finishes are per MIL-M-38510.
4. Letter designations are for cross-reference to MIL-M-38510.

68-Pin Pingrid Array



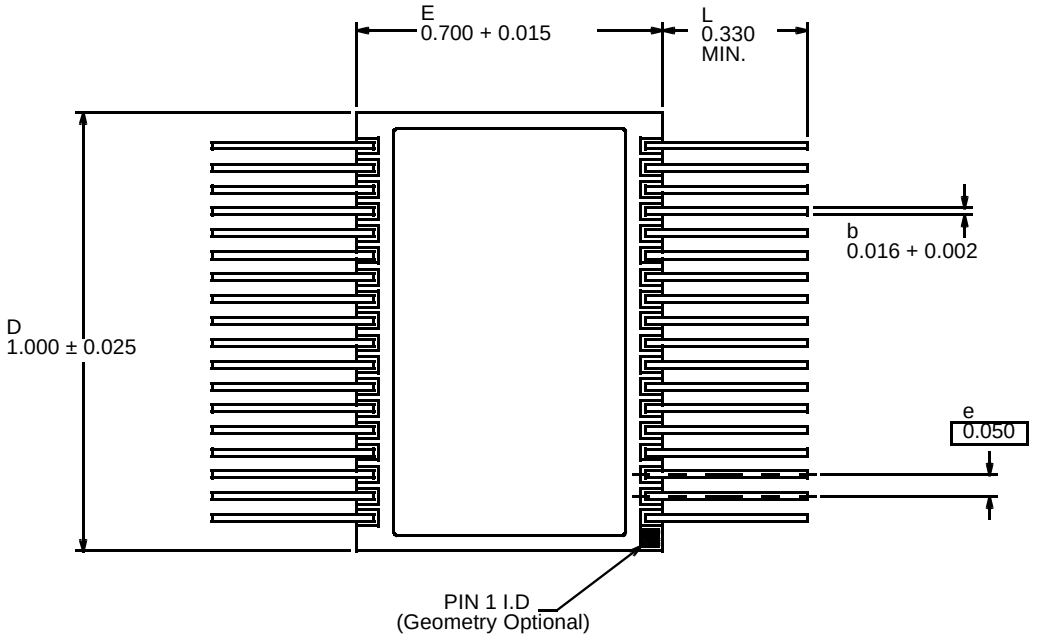
Notes:

1 All package finishes are per MIL-M-38510.

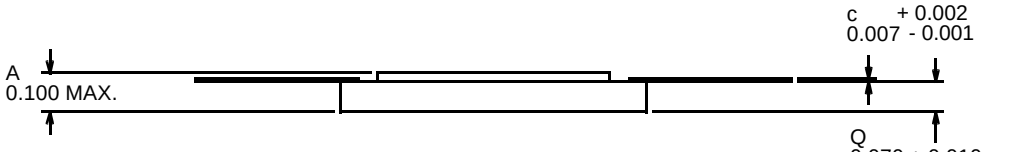
2. It is recommended that package ceramic be mounted to a heat removal rail located on the printed circuit board. A thermally conductive material such as MERECO XLN-589 or equivalent should be used.

3. Letter designations are for cross-reference to MIL-M-38510.

36-Lead Flatpack, Dual Cavity (100-MIL Lead Spacing)



TOP

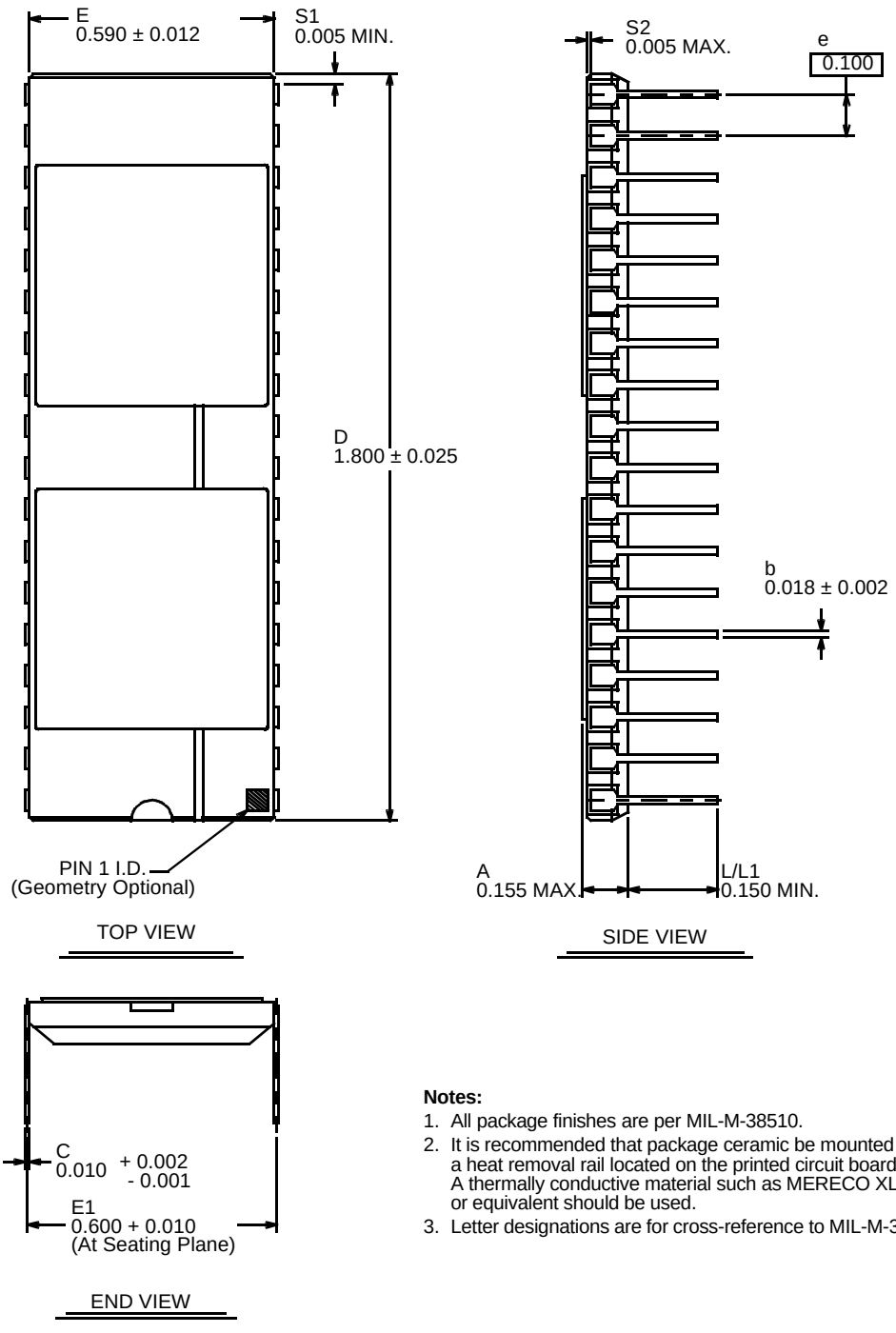


END

Notes:

1. All package finishes are per MIL-M-38510.
2. It is recommended that package ceramic be mounted to a heat removal rail located on the printed circuit board. A thermally conductive material such as MERECO XLN-589 or equivalent should be used.
3. Letter designations are for cross-reference to MIL-M-38510.

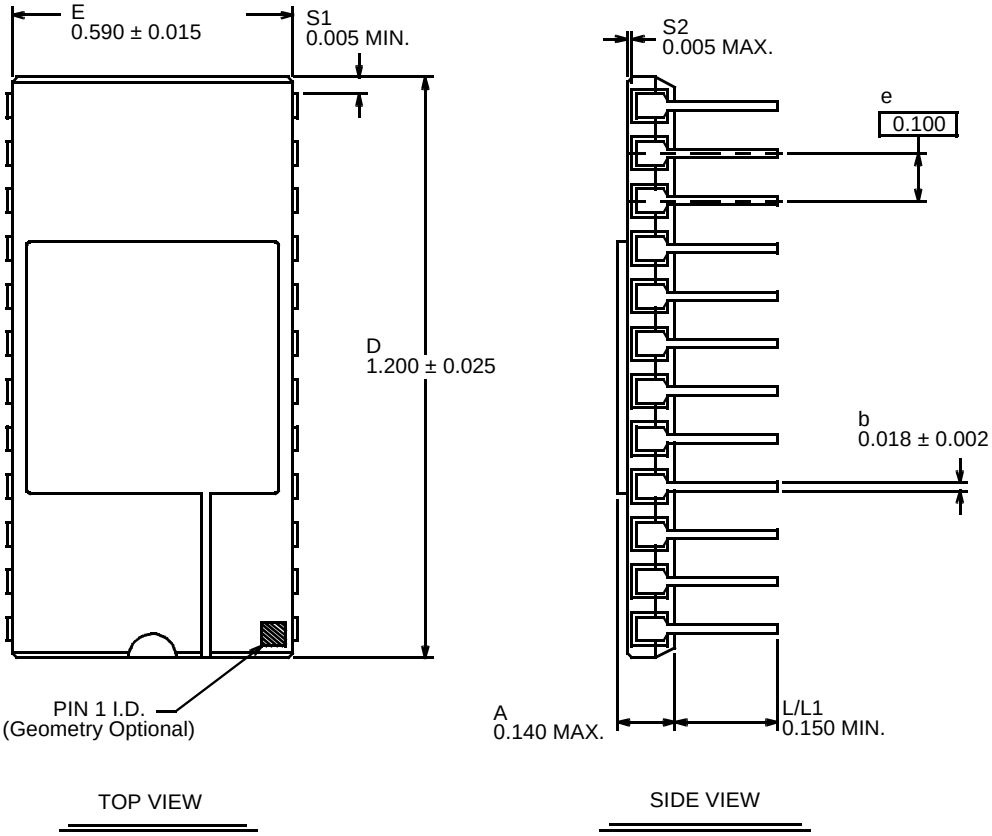
36-Lead Flatpack, Dual Cavity (50-MIL Lead Spacing)



Notes:

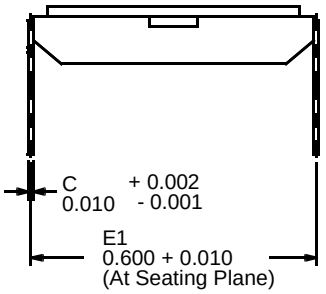
1. All package finishes are per MIL-M-38510.
2. It is recommended that package ceramic be mounted to a heat removal rail located on the printed circuit board. A thermally conductive material such as MERECO XLN-589 or equivalent should be used.
3. Letter designations are for cross-reference to MIL-M-38510.

36-Lead Side-Brazed DIP, Dual Cavity



TOP VIEW

SIDE VIEW



END VIEW

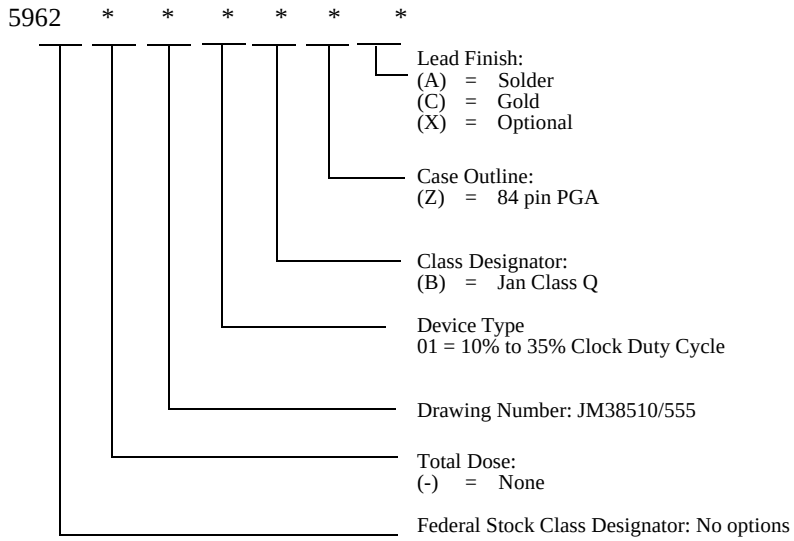
Notes:

1. All package finishes are per MIL-M-38510.
2. It is recommended that package ceramic be mounted to a heat removal rail located on the printed circuit board. A thermally conductive material such as MERECO XLN-589 or equivalent should be used.
3. Letter designations are for cross-reference to MIL-M-38510.

24-Lead Side-Brazed DIP, Single Cavity

ORDERING INFORMATION

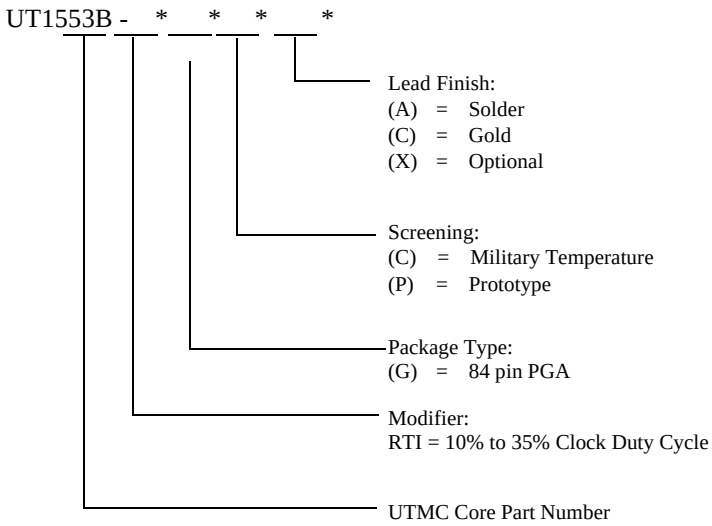
UT1553B RTI Remote Terminal Interface:



Notes:

1. Lead finish (A, C, or X) must be specified.
2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).

UT1553B RTI Remote Terminal Interface



Notes:

1. Lead finish (A, C, or X) must be specified.
2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Mil Temp range flow per UTMC's manufacturing flows document. Devices are tested at -55°C, room temperature, and 125°C.
4. Prototpe flow per UTMC's document manufacturing flows and are tested at 25°C only. Lead finish is GOLD only.
5. Prototypes and reduced high-reliability devices are only available with 40% to 60% clock duty cycle.