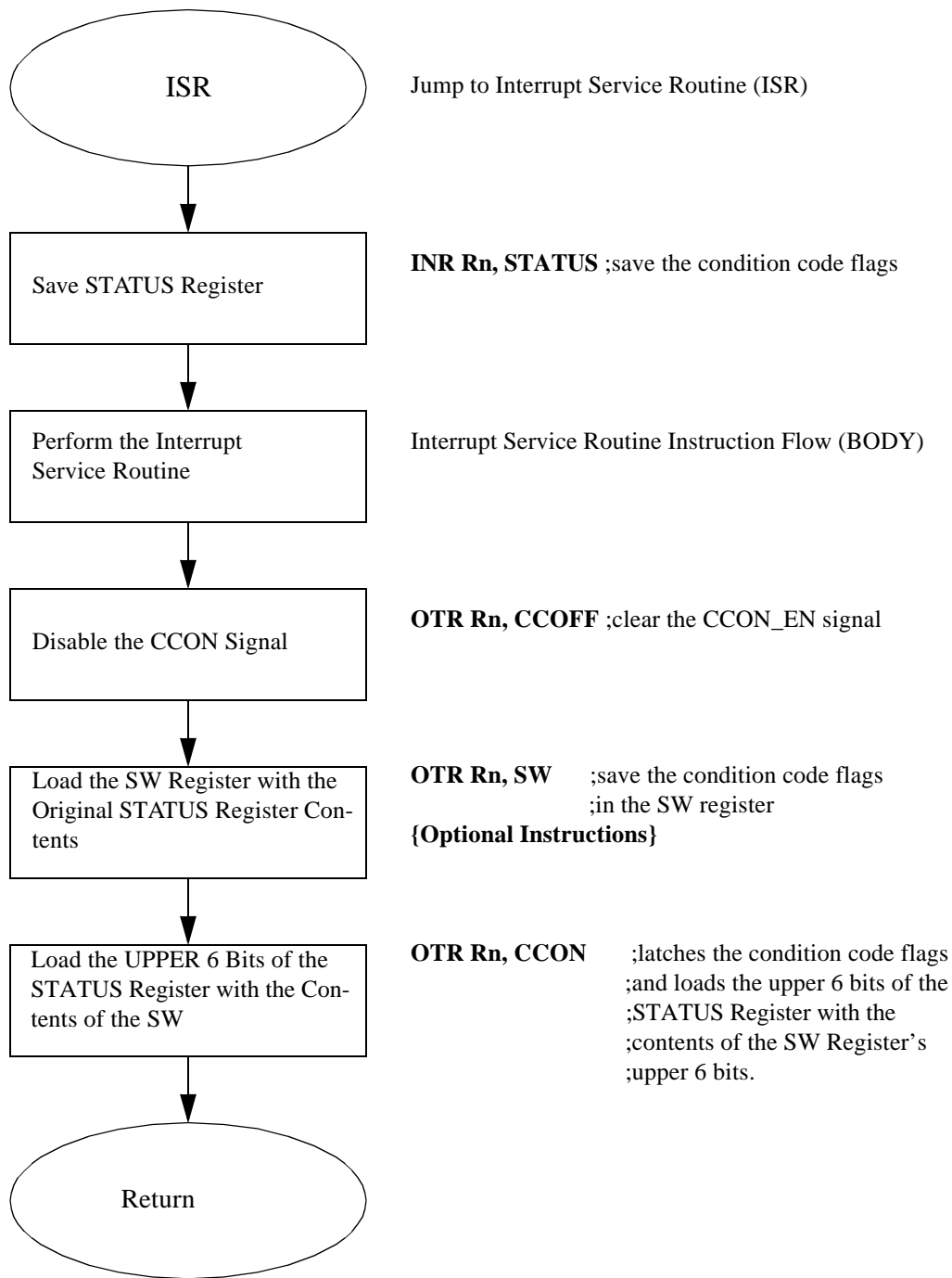# UTMC Product Advisory

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UT1750AR RISC Microcontroller CCON Operation

Introduction:

The UTMC Engineering Notebook Document Number UT1750AR-7 on Status Register Writes dated January 24, 1990 discusses a method for manually updating the contents of the system STATUS Register. The UT1750AR instruction set architecture does not directly support the loading of the status register with data from a general purpose register. A work-around to this limitation, as defined by the engineering notebook, suggests the programmer use the OTR CCON instruction to load the STATUS Register's upper 6 bits (i.e. condition code flags). This suggestion implies the OTR Rn, CCON instruction **immediately follows** an OTR Rn, SW instruction. The UT1750AR uses the CCON signal to enable the clock phase CK1 to latch the contents of the upper 4 SW bits into the upper 4 STATUS bits. The upper 4 bits on the STATUS word are latched during the high period of CK1 and are held when CK1 transitions from high to low. Additionally, the CCON signal is used to enable clocking of the C, P, Z, and N condition code flags from the STATUS register into the SW register on the falling edge of CK1. Consequently, a write to the SW using an OTR Rn, SW instruction updates the SW with the contents of Rn. The next instruction causes the previous contents of the STATUS register to overwrite the condition codes in the SW register. If the next instruction is an OTR Rn, CCON it allows the contents of the SW to update the STATUS register before they are fed back into the SW on the falling edge of CK1. The ability to restore condition code flags is important for proper operation of interrupt service routines. Most software applications allow an interrupt to occur between the time the UT1750AR executes an instruction which modifies the condition codes, and the time the condition code flags are used to evaluate a branch instruction. Once in the interrupt service routine, there exists a strong possibility the pre-ISR condition codes will be modified within the interrupt service routine, and to return to the user's main program will require the original condition codes be restored.

Solution:

If the software guarantees anytime the condition codes are modified by an OTR Rn, SW instruction, the next instruction executed will always be an OTR Rn, CCON. The user can be confident the condition codes are restored properly. If, however, there exists the possibility the OTR Rn, SW and OTR Rn, CCON instructions may not occur contiguously, the user uses an OTR Rn, CCOFF instruction before manually updating the SW with an OTR Rn, SW instruction. The OTR Rn, CCOFF instruction is used to disable the clocking of the STATUS word's condition codes into the SW's condition code latches. The following flow chart describes the proper programming flow guarantees the user's condition codes will be restored whether the OTR Rn, SW and OTR Rn, CCON instruction occur consecutively.

```
        ┌─────────────┐
        │     ISR     │          Jump to Interrupt Service Routine (ISR)
        └─────────────┘
               │
               ▼
   ┌──────────────────────┐
   │ Save STATUS Register │      **INR Rn, STATUS** ;save the condition code flags
   └──────────────────────┘
               │
               ▼
   ┌──────────────────────┐
   │ Perform the Interrupt│      Interrupt Service Routine Instruction Flow (BODY)
   │ Service Routine      │
   └──────────────────────┘
               │
               ▼
   ┌──────────────────────┐
   │ Disable the CCON     │      **OTR Rn, CCOFF** ;clear the CCON_EN signal
   │ Signal               │
   └──────────────────────┘
               │
               ▼
   ┌──────────────────────┐
   │ Load the SW Register │      **OTR Rn, SW**      ;save the condition code flags
   │ with the Original    │                         ;in the SW register
   │ STATUS Register Con- │      **{Optional Instructions}**
   │ tents                │
   └──────────────────────┘
               │
               ▼
   ┌──────────────────────┐
   │ Load the UPPER 6 Bits│      **OTR Rn, CCON**     ;latches the condition code flags
   │ of the STATUS        │                          ;and loads the upper 6 bits of the
   │ Register with the    │                          ;STATUS Register with the
   │ Contents of the SW   │                          ;contents of the SW Register's
   └──────────────────────┘                          ;upper 6 bits.
               │
               ▼
        ┌─────────────┐
        │   Return    │
        └─────────────┘
```

Per the above diagram, the user reads the STATUS Register at the beginning of the interrupt service routine to prevent corruption. After completing the interrupt service routine, the user restores the status register before returning to the main program. Remember that after the **OTR Rn, CCON** command is executed, the condition code flags can be modified by certain instruction executions.