

# 0.35 $\mu\text{m}$ CMOS Gate Array CMOS-9HD Family



Second-generation highly integrated 0.35  $\mu\text{m}$  CMOS gate array  
Considerable cost reduction

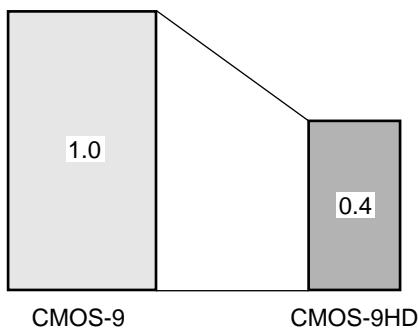
New  
Products

# FEATURES

The CMOS-9HD Family is a channel-less type gate array that uses the 0.35- $\mu\text{m}$  leading-edge process and realizes 960,000 usable gates. This family is adaptable for both high-speed and low-power consumption systems. Currently supporting a 3.3-V supply voltage, it is expected that the future lineup will be able to support a supply voltage of 2.5 V.

## High Integration/Low Power Consumption

- Maximum of 960,000 usable gates integrated
- Improved cell structure, higher density
- Lower power consumption (a further 30% reduction from CMOS-9)



◀ Cell size comparison (1 cell)

CMOS-9: NEC's conventional 0.35- $\mu\text{m}$  gate array

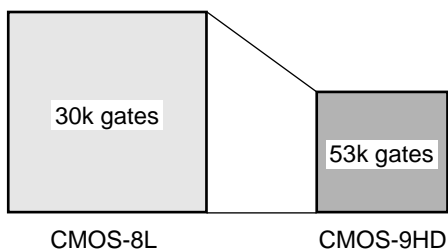
## In Pursuit of Lower Cost

- Enhanced cost competitiveness through chip-size shrinkage
- Fewer gate masters leading to further cost reduction

(Example) Comparison with CMOS-8L

Although the 30k-gate CMOS-8L and the 53k-gate CMOS-9HD are similar in terms of price, because the cell density is higher in the CMOS-9HD, for an area of 30k integrated gates or more, the CMOS-9HD is the more cost-competitive choice.

Note that the applicable-package pin-count range differs depending on the chip size, even if the gate scale is identical.



◀ Chip size comparison

CMOS-8L: NEC's conventional 0.5- $\mu\text{m}$  gate array

## Ultra High-Speed Operation

- $t_{PD} = 131$  ps (2-input NAND, fanout = 1, standard wiring length)
- $t_{PD} = 107$  ps (2-input NAND (power gate), fanout = 1, standard wiring length)
- $t_{PD} = 229$  ps (input buffer, fanout = 1, standard wiring length)
- $t_{PD} = 222$  ps (input buffer, standard load)
- $t_{PD} = 1396$  ps (output buffer,  $C_L = 50$  pF)

## Provision of Function Block Enabling High Speed/High Integration

- Including high speed and low power, compatible with CMOS-8L Family
- Scan path block
- Driver for clock tree synthesis
- Asynchronous single-port RAM (45 types)
- Asynchronous dual-port RAM (45 types)
- Asynchronous compiled single-port RAM
- Synchronous/asynchronous compiled dual-port RAM

## Abundance of Peripheral Blocks

- |   |  |
|---|--|
| • LVTTTL/TTL 5-V withstand voltage interface buffer | • Low-noise buffer   |
| • LVTTTL interface buffer with fail safe function   | • Buffers with on-chip pull-up resistors (5 k $\Omega$ , 50 k $\Omega$ ) |
| • High drive capacity buffer ( $I_{OL} = 24$ mA)    | • Buffers with on-chip pull-down resistors (50 k $\Omega$ )              |
| • PCI   | • Digital PLL (33 to 80 MHz)   |
| • GTL+  | • Digital PLL (multiple)   |

## Power Consumption

- 0.524  $\mu$ W/MHz/cell (Internal gates,  $V_{DD} = 3.3$  V)

## Support of Variety of Pin Count Packages

- 100- to 304-pin plastic QFP (fine-pitch)
- 160-pin, 208-pin plastic QFP (fine-pitch, with heat spreader)
- 48- to 120-pin plastic TQFP
- 144-pin plastic LQFP
- 225- to 352-pin plastic BGA
- 108- to 304-pin plastic FBGA
- 256- to 696-pin tape BGA (with heat spreader)

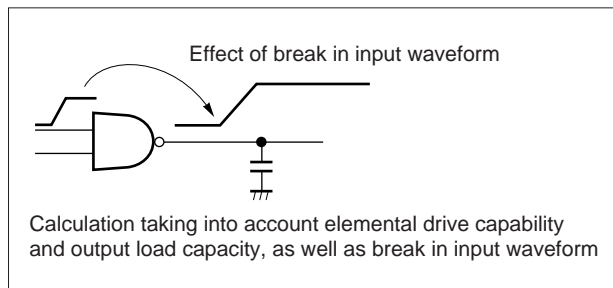
## Precision Delay Estimation

### <Wiring length calculation>

- Can be calculated using a floorplan
- Floorplan-calculated wiring length can be used in logic synthesis and design rule check programs

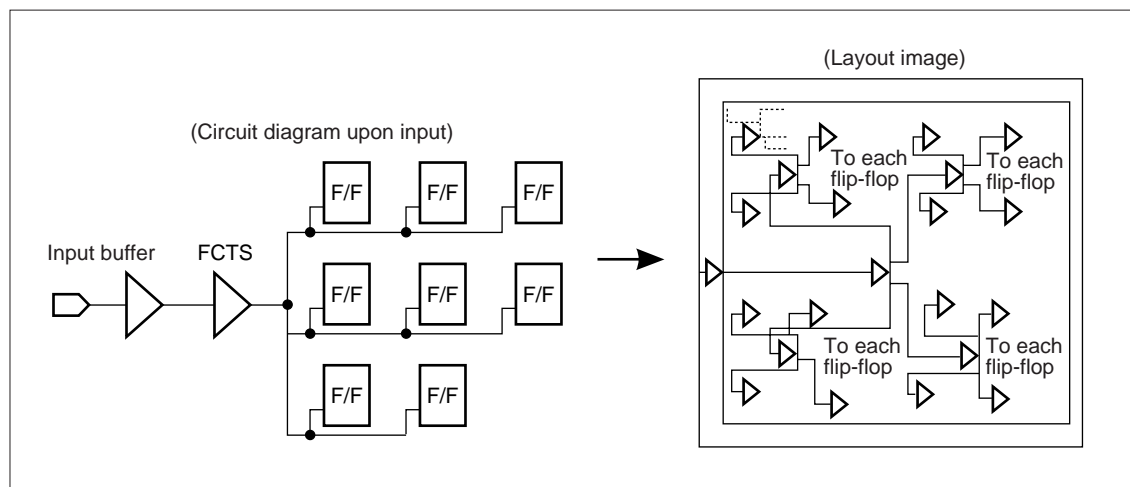
### <Delay calculation>

- Takes into account the break in the block's input waveform



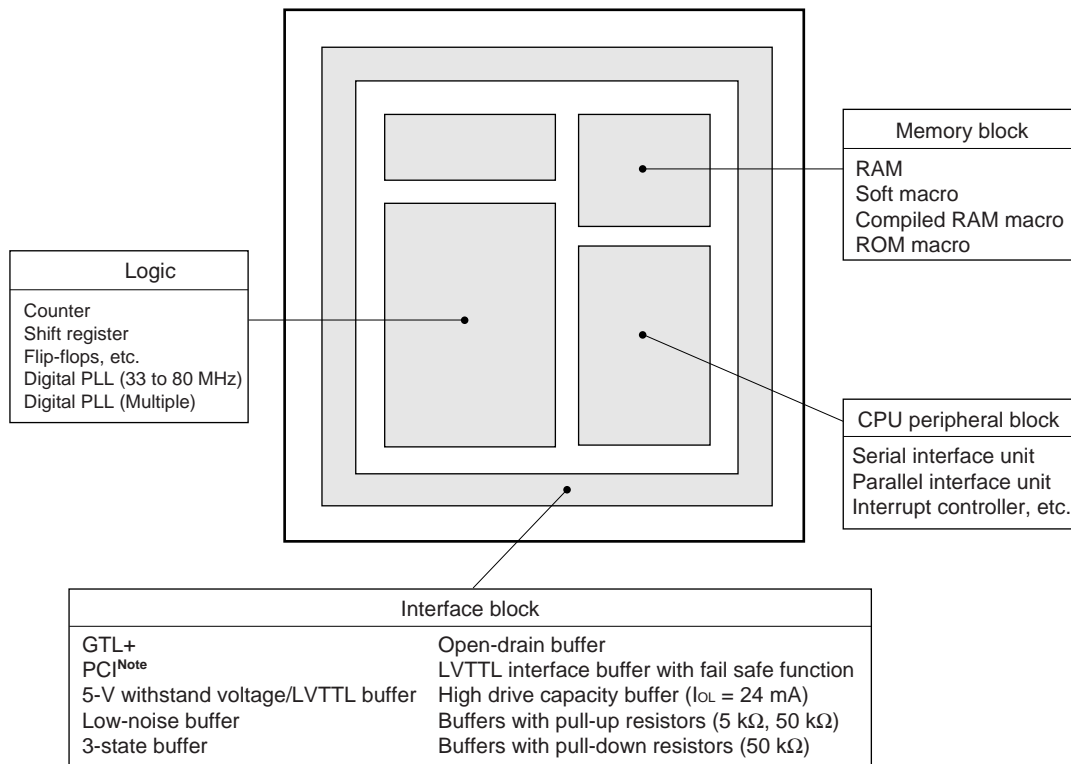
## Clock Tree Synthesis

- Clock tree automatically synthesized during layout to minimize clock skew
- Up to 10000 flip-flops can be connected



## Multifarious Function Block Mounting Capability

The function blocks ensure functional compatibility with conventional products and facilitate transfer or appropriation of existing design data.



**Note** Standard interface recommended by Intel Corp. (PCI = Peripheral Component Interconnect)

## Applications (Supported Fields)

All fields from large-scale high-speed processing systems to small and medium scale general applications are covered.

- Multimedia market
  - PC, AV, moving picture processing, 3D, etc.
- Communications market
  - High-speed communication, cellular terminals, etc.
- OA, industrial, and other applications.

# PRODUCT OUTLINE

## List of Product Types

### 3-layer wiring

| Part Number                | μPD65943 | μPD65944 | μPD65945 | μPD65946 | μPD65948 | μPD65949 | μPD65951 | μPD65954 | μPD65956 | μPD65958 |
|----------------------------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| Number of signals          | 156      | 180      | 200      | 252      | 308      | 364      | 416      | 496      | 572      | 692      |
| Number of pads             | 172      | 196      | 216      | 268      | 324      | 380      | 436      | 516      | 588      | 708      |
| Number of integrated gates | 75740    | 100602   | 128338   | 202630   | 312684   | 437136   | 585390   | 835664   | 1096452  | 1615646  |
| Number of usable gates     | 53018    | 70421    | 89836    | 141841   | 218879   | 262281   | 321964   | 459615   | 603048   | 807823   |

**Remark** The actual number of usable signal lines depends on the package and the number of power supply and GND pins used.

### 4-layer wiring

| Part Number                | μPD65961 | μPD65964 | μPD65966 | μPD65968 | μPD65969 | μPD65970 | μPD65971 |
|----------------------------|----------|----------|----------|----------|----------|----------|----------|
| Number of signals          | –        | –        | –        | –        | –        | –        | –        |
| Number of pads             | 436      | 516      | 588      | 708      | 764      | 820      | 876      |
| Number of integrated gates | 585390   | 835664   | 1096452  | 1615646  | 1904700  | 2196592  | 2509284  |
| Number of usable gates     | 380503   | 54318    | 712693   | 969387   | 1142820  | 1317955  | 1505570  |

**Remark** The actual number of usable signal lines depends on the package and the number of power supply and GND pins used.

## List of Packages

### 3-layer wiring

(1/2)

| Package                                  | Pins | μPD65943 | μPD65944 | μPD65945 | μPD65946 | μPD65948 |
|--|------|----------|----------|----------|----------|----------|
| Plastic QFP (fine-pitch)                 | 100  | ✓        | ✓        | ✓        | ✓        | ✓        |
|  | 120  | —        | —        | —        | ✓        | —        |
|  | 144  | ✓        | ✓        | ✓        | ✓        | ✓        |
|  | 160  | ✓        | ✓        | ✓        | ✓        | ✓        |
|  | 176  | —        | ✓        | ✓        |          |          |
|  | 208  | —        | —        | ✓        | ✓        | ✓        |
|  | 240  | —        | —        | —        | ✓        | ✓        |
|  | 304  | —        | —        | —        | —        | ✓        |
| Plastic QFP (fine-pitch) <sup>Note</sup> | 160  | —        | —        | —        | —        | —        |
|  | 208  | —        | —        | —        | —        | —        |
| Plastic TQFP                             | 48   |          | —        | —        | —        | —        |
|  | 64   |          | —        | —        | —        | —        |
|  | 80   | ✓        |          |          |          | —        |
|  | 100  | ✓        | —        | —        | —        | ✓        |
|  | 120  |          | —        | —        | ✓        |          |
| Plastic LQFP                             | 144  | —        | —        | —        | —        | ✓        |
| Plastic BGA                              | 225  | —        | —        | —        |          |          |
|  | 256  | —        | —        | —        | —        | ✓        |
|  | 272  | —        | —        | —        | —        |          |
|  | 313  | —        | —        | —        | —        | —        |
|  | 352  | —        | —        | —        | —        | —        |
| Plastic FBGA                             | 108  |          |          |          |          |          |
|  | 144  |          |          |          |          |          |
|  | 160  |          |          |          |          |          |
|  | 176  | —        | ✓        | ✓        |          |          |
|  | 208  | —        | —        | —        | —        | —        |
|  | 240  | —        | —        | —        | —        | —        |
|  | 304  | —        | —        | —        | —        | —        |
| Plastic BGA (advanced)                   | 672  | —        | —        | —        | —        | —        |
| Tape BGA <sup>Note</sup>                 | 256  | —        | —        | —        | ✓        | ✓        |
|  | 352  | —        | —        | —        | —        | —        |
|  | 420  | —        | —        | —        | —        | —        |
|  | 500  | —        | —        | —        | —        | —        |
|  | 576  | —        | —        | —        | —        | —        |
|  | 696  | —        | —        | —        | —        | —        |

**Note** With heat spreader

**Remark** ✓: Supported, —: Not supported, Blank: Under consideration

## List of Packages

### 3-layer wiring

(2/2)

| Package                                  | Pins | μPD65949 | μPD65951 | μPD65954 | μPD65956 | μPD65958 |
|--|------|----------|----------|----------|----------|----------|
| Plastic QFP (fine-pitch)                 | 100  | ✓        | ✓        | ✓        | —        | —        |
|  | 120  | —        | —        | —        | —        | —        |
|  | 144  | ✓        | ✓        | —        | —        | —        |
|  | 160  | ✓        | ✓        | ✓        | ✓        | —        |
|  | 176  |          |          |          |          | —        |
|  | 208  | ✓        | ✓        | ✓        | ✓        | ✓        |
|  | 240  | ✓        | ✓        | ✓        | ✓        | ✓        |
|  | 304  | —        | ✓        | ✓        | ✓        | ✓        |
| Plastic QFP (fine-pitch) <sup>Note</sup> | 160  |          |          |          |          |          |
|  | 208  |          |          |          |          |          |
| Plastic TQFP                             | 48   | —        | —        | —        | —        | —        |
|  | 64   | —        | —        | —        | —        | —        |
|  | 80   | —        | —        | —        | —        | —        |
|  | 100  | ✓        | —        | —        | —        | —        |
|  | 120  |          | —        | —        | —        | —        |
| Plastic LQFP                             | 144  |          | —        | —        | —        | —        |
| Plastic BGA                              | 225  |          |          |          |          | —        |
|  | 256  | ✓        | ✓        |          |          | —        |
|  | 272  | ✓        | ✓        |          | —        | —        |
|  | 313  | ✓        | ✓        |          |          |          |
|  | 352  | ✓        | ✓        |          |          | ✓        |
| Plastic FBGA                             | 108  | —        | —        | —        | —        | —        |
|  | 144  |          |          | —        | —        | —        |
|  | 160  |          |          | —        | —        | —        |
|  | 176  |          |          |          |          | —        |
|  | 208  | ✓        |          |          |          | —        |
|  | 240  | —        |          |          |          |          |
|  | 304  | —        | —        | —        |          |          |
| Plastic BGA (advanced)                   | 672  | —        | —        | —        | —        | ✓        |
| Tape BGA <sup>Note</sup>                 | 256  | ✓        | ✓        |          | —        | —        |
|  | 352  | ✓        | ✓        | ✓        | ✓        | —        |
|  | 420  | —        | ✓        | ✓        | ✓        | ✓        |
|  | 500  | —        | —        | ✓        | ✓        | ✓        |
|  | 576  | —        | —        | —        | ✓        | ✓        |
|  | 696  | —        | —        | —        | —        | ✓        |

**Note** With heat spreader

**Remark** ✓: Supported, —: Not supported, Blank: Under consideration

## List of Packages

### 4-layer wiring

(1/2)

| Package                                  | Pins | $\mu$ PD65961 | $\mu$ PD65964 | $\mu$ PD65966 | $\mu$ PD65968 | $\mu$ PD65969 |
|--|------|---------------|---------------|---------------|---------------|---------------|
| Plastic QFP (fine-pitch) <sup>Note</sup> | 160  | —             | —             | —             | —             | —             |
|  | 208  |               |               |               |               |               |
| Tape BGA <sup>Note</sup>                 | 256  | —             | —             | —             | —             | —             |
|  | 352  |               |               |               |               | —             |
|  | 420  |               |               |               |               |               |
|  | 500  | —             |               |               |               |               |
|  | 576  | —             | —             |               |               |               |
|  | 696  | —             | —             |               |               |               |
| Plastic BGA (advanced)                   | 672  | —             | —             | —             |               |               |

**Note** With heat spreader

**Remark** — : Not supported, Blank : Under consideration

### 4-layer wiring

(2/2)

| Package                                  | Pins | $\mu$ PD65970 | $\mu$ PD65971 |
|--|------|---------------|---------------|
| Plastic QFP (fine-pitch) <sup>Note</sup> | 160  | —             | —             |
|  | 208  |               |               |
| Tape BGA <sup>Note</sup>                 | 256  | —             | —             |
|  | 352  |               |               |
|  | 420  |               |               |
|  | 500  |               |               |
|  | 576  |               |               |
|  | 696  |               |               |
| Plastic BGA (advanced)                   | 672  |               |               |

**Note** With heat spreader

**Remark** — : Not supported, Blank : Under consideration

# ELECTRICAL SPECIFICATIONS

## Absolute Maximum Ratings

| Parameter   | Symbol    | Conditions                      | Ratings                | Unit |
|---|-----------|---------------------------------|------------------------|------|
| Supply voltage                                    | $V_{DD}$  |                                 | −0.5 to +4.6           | V    |
| Input voltage                                     |           |                                 |                        |      |
| LVTTL interface buffer                            | $V_I$     | $V_I < V_{DD} + 0.5 \text{ V}$  | −0.5 to +4.6           | V    |
| LVTTL interface buffer<br>with fail safe function | $V_I$     | $V_I < V_{DD} + 0.5 \text{ V}$  | −0.5 to +4.6           | V    |
| TTL 5-V withstand voltage interface buffer        | $V_I$     | $V_I < V_{DD} + 3.0 \text{ V}$  | −0.5 to +6.6           | V    |
| Output voltage                                    |           |                                 |                        |      |
| LVTTL output buffer                               | $V_O$     | $V_O < V_{DD} + 0.5 \text{ V}$  | −0.5 to +4.6           | V    |
| TTL 5-V output buffer                             | $V_O$     | $V_O < V_{DD} + 3.0 \text{ V}$  | −0.5 to +6.6           | V    |
| 5-V output buffer for CMOS                        | $V_O$     | $V_O < V_{DD} + 3.0 \text{ V}$  | −0.5 to +6.6           | V    |
| Input/output voltage                              | $V_I/V_O$ | Normal I/O pin                  | −0.5 to $V_{DD} + 0.5$ | V    |
| Output current <sup>Note</sup>                    | $I_O$     | $I_{OL} = 1 \text{ mA (FV0A)}$  | 3                      | mA   |
|   |           | $I_{OL} = 2 \text{ mA (FV0B)}$  | 7                      | mA   |
|   |           | $I_{OL} = 3 \text{ mA (FO09)}$  | 10                     | mA   |
|   |           | $I_{OL} = 6 \text{ mA (FO04)}$  | 20                     | mA   |
|   |           | $I_{OL} = 9 \text{ mA (FO01)}$  | 30                     | mA   |
|   |           | $I_{OL} = 12 \text{ mA (FO02)}$ | 40                     | mA   |
|   |           | $I_{OL} = 18 \text{ mA (FO03)}$ | 60                     | mA   |
|   |           | $I_{OL} = 24 \text{ mA (FO06)}$ | 75                     | mA   |
| Operating ambient temperature                     | $T_A$     |                                 | −40 to +85             | °C   |
| Storage temperature                               | $T_{stg}$ |                                 | −65 to +150            | °C   |

**Note** Output current: Indicates the maximum value of the current that is allowed to flow directly through this output pin.

**Remark** With the exception of the buffer with fail safe function, be sure to input voltage to the I/O pins only after the supply voltage has been fixed.

## Recommended Operating Range

| Parameter                | Symbol   | Conditions                          | MIN. | TYP. | MAX.     | Unit |
|--------------------------|----------|-------------------------------------|------|------|----------|------|
| Supply voltage           | $V_{DD}$ | LVTTTL interface                    | 3.00 | 3.30 | 3.60     | V    |
| High-level input voltage | $V_{IH}$ |                                     | 2.0  |      | $V_{DD}$ | V    |
| Low-level input voltage  | $V_{IL}$ |                                     | 0    |      | 0.8      | V    |
| Positive trigger voltage | $V_P$    |                                     | 1.4  |      | 2.4      | V    |
| Negative trigger voltage | $V_N$    |                                     | 0.8  |      | 1.6      | V    |
| Hysteresis voltage       | $V_H$    |                                     | 0.3  |      | 1.5      | V    |
| High-level input voltage | $V_{IH}$ | TTL 5-V withstand voltage interface | 2.0  |      | 5.5      | V    |
| Low-level input voltage  | $V_{IL}$ |                                     | 0    |      | 0.8      | V    |
| Positive trigger voltage | $V_P$    |                                     | 1.4  |      | 2.4      | V    |
| Negative trigger voltage | $V_N$    |                                     | 0.8  |      | 1.6      | V    |
| Hysteresis voltage       | $V_H$    |                                     | 0.3  |      | 1.5      | V    |
| Input rise time          | $t_{ri}$ | Normal input                        | 0    |      | 200      | ns   |
| Input fall time          | $t_{fi}$ |                                     | 0    |      | 200      | ns   |
| Input rise time          | $t_{ri}$ | Schmitt input                       | 0    |      | 10       | ms   |
| Input fall time          | $t_{fi}$ |                                     | 0    |      | 10       | ms   |

## DC Characteristics (V<sub>DD</sub> = 3.3 V ±0.3 V)

(1/3)

| Parameter   | Symbol          | Conditions   | MIN. | TYP. | MAX.  | Unit |
|---|-----------------|--|------|------|-------|------|
| Static current consumption <sup>Note 1</sup>                      |                 |  |      |      |       |      |
| μPD65943, μPD65944,<br>μPD65945, μPD65946,<br>μPD65948, μPD65949, | I <sub>DD</sub> | V <sub>I</sub> = V <sub>DD</sub> or GND                                    |      | 2.0  | 300   | μA   |
| μPD65951, μPD65954,<br>μPD65956                                   | I <sub>DD</sub> | V <sub>I</sub> = V <sub>DD</sub> or GND                                    |      | 0    | 400   | μA   |
| μPD65958  | I <sub>DD</sub> | V <sub>I</sub> = V <sub>DD</sub> or GND                                    |      | 4.0  | 800   | μA   |
| Off-state output current <sup>Note 2</sup>                        |                 |  |      |      |       |      |
| LVTTL output  | I <sub>OZ</sub> | V <sub>O</sub> = V <sub>DD</sub> or GND                                    |      |      | ±10   | μA   |
| TTL 5-V withstand voltage output                                  | I <sub>OZ</sub> | V <sub>O</sub> = V <sub>DD</sub> or GND                                    |      |      | ±10   | μA   |
| 5-V withstand voltage for CMOS                                    | I <sub>OZ</sub> | V <sub>O</sub> = V <sub>DD</sub> or GND                                    |      |      | ±10   | μA   |
| Output current flow <sup>Note 3</sup><br>5-V output for CMOS      | I <sub>R</sub>  | V <sub>PU</sub> = 5.5 V, R <sub>PU</sub> = 2 kΩ,<br>V <sub>O</sub> = 3.0 V |      |      | 0.1   | μA   |
| Output short-circuit current <sup>Note 4</sup>                    | I <sub>OS</sub> | V <sub>O</sub> = GND   |      |      | −250  | mA   |
| Input leakage current   |                 |  |      |      |       |      |
| Normal input  | I <sub>I</sub>  | V <sub>I</sub> = V <sub>DD</sub> or GND                                    |      |      | ±1.0  | μA   |
| With pull-up resistor (50 kΩ)                                     | I <sub>I</sub>  | V <sub>I</sub> = GND   | −28  | −83  | −190  | μA   |
| With pull-up resistor (5 kΩ)                                      | I <sub>I</sub>  | V <sub>I</sub> = GND   | −280 | −700 | −1900 | μA   |
| With pull-down resistor (50 kΩ)                                   | I <sub>I</sub>  | V <sub>I</sub> = V <sub>DD</sub>   | 28   | 83   | 190   | μA   |
| Pull-up resistor 50 kΩ  | R <sub>PU</sub> |  | 18.9 | 39.8 | 107.1 | kΩ   |
| Pull-up resistor 5 kΩ   | R <sub>PU</sub> |  | 1.9  | 4.7  | 10.7  | kΩ   |
| Pull-down resistor 50 kΩ  | R <sub>PD</sub> |  | 18.9 | 39.8 | 107.1 | kΩ   |

**Notes 1.** When using I/O blocks (etc.) with pull-up/pull-down resistors incorporated, the static current consumption increases.

**2.** Because there is a bias toward the 5-V protection circuit in the TTL 5-V withstand voltage and 5-V withstand voltage for CMOS 3-state or I/O buffers, the output-off state current increases slightly.

**3.** When the LSI supply current is pulled up to a higher voltage in the CMOS output buffer, a current that flows from the output pin to inside the LSI is generated.

**4.** The output short-circuit time is less than 1 second and for 1 LSI pin only.

**Remarks 1.** The + and − symbols attached to the current values in the table indicate the direction of the current. The symbol is + when the current is flowing into the device, and − when flowing out of the device.

**2.** Blanks in the table indicate that the values are undergoing evaluation.

## DC Characteristics (V<sub>DD</sub> = 3.3 V ±0.3 V)

(2/3)

| Parameter                | Symbol          | Conditions   | MIN.  | TYP. | MAX. | Unit |
|--------------------------|-----------------|--|-------|------|------|------|
| Low-level output current |                 |  |       |      |      |      |
| 3 mA buffer (FO09)       | I <sub>OL</sub> | LVTTL output type<br>V <sub>OL</sub> = 0.4 V                             | 3.00  |      |      | mA   |
| 6 mA buffer (FO04)       | I <sub>OL</sub> |  | 6.00  |      |      | mA   |
| 9 mA buffer (FO01)       | I <sub>OL</sub> |  | 9.00  |      |      | mA   |
| 12 mA buffer (FO02)      | I <sub>OL</sub> |  | 12.00 |      |      | mA   |
| 18 mA buffer (FO03)      | I <sub>OL</sub> |  | 18.00 |      |      | mA   |
| 24 mA buffer (FO06)      | I <sub>OL</sub> |  | 24.00 |      |      | mA   |
| 1 mA buffer (FV0A)       | I <sub>OL</sub> | TTL 5-V withstand voltage<br>output type<br>V <sub>OL</sub> = 0.4 V      | 1.00  |      |      | mA   |
| 2 mA buffer (FV0B)       | I <sub>OL</sub> |  | 2.00  |      |      | mA   |
| 3 mA buffer (FV09)       | I <sub>OL</sub> |  | 3.00  |      |      | mA   |
| 6 mA buffer (FV04)       | I <sub>OL</sub> |  | 6.00  |      |      | mA   |
| 9 mA buffer (FV01)       | I <sub>OL</sub> |  | 9.00  |      |      | mA   |
| 12 mA buffer (FV02)      | I <sub>OL</sub> |  | 12.00 |      |      | mA   |
| 18 mA buffer (FV03)      | I <sub>OL</sub> |  | 18.00 |      |      | mA   |
| 24 mA buffer (FV06)      | I <sub>OL</sub> |  | 24.00 |      |      | mA   |
| 3 mA buffer (FY09)       | I <sub>OL</sub> | 5-V withstand voltage output<br>for CMOS type<br>V <sub>OL</sub> = 0.4 V | 3.00  |      |      | mA   |
| 6 mA buffer (FY04)       | I <sub>OL</sub> |  | 6.00  |      |      | mA   |
| 9 mA buffer (FY01)       | I <sub>OL</sub> |  | 9.00  |      |      | mA   |
| 12 mA buffer (FY02)      | I <sub>OL</sub> |  | 12.00 |      |      | mA   |
| 18 mA buffer (FY03)      | I <sub>OL</sub> |  | 18.00 |      |      | mA   |
| 24 mA buffer (FY06)      | I <sub>OL</sub> |  | 24.00 |      |      | mA   |

## DC Characteristics ( $V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$ )

(3/3)

| Parameter                                       | Symbol          | Conditions  | MIN.                  | TYP. | MAX. | Unit |
|---|-----------------|---|-----------------------|------|------|------|
| High-level output current                       |                 |   |                       |      |      |      |
| 3 mA buffer (FO09)                              | I <sub>OH</sub> | LVTTTL output type<br>V <sub>OH</sub> = 2.4 V                       | −3.00                 |      |      | mA   |
| 6 mA buffer (FO04)                              | I <sub>OH</sub> |   | −6.00                 |      |      | mA   |
| 9 mA buffer (FO01)                              | I <sub>OH</sub> |   | −9.00                 |      |      | mA   |
| 12 mA buffer (FO02)                             | I <sub>OH</sub> |   | −12.00                |      |      | mA   |
| 18 mA buffer (FO03)                             | I <sub>OH</sub> |   | −18.00                |      |      | mA   |
| 24 mA buffer (FO06)                             | I <sub>OH</sub> |   | −24.00                |      |      | mA   |
| 1 mA buffer (FV0A)                              | I <sub>OH</sub> | TTL 5-V withstand voltage<br>output type<br>V <sub>OH</sub> = 2.4 V | −1.00                 |      |      | mA   |
| 2 mA buffer (FV0B)                              | I <sub>OH</sub> |   | −1.00                 |      |      | mA   |
| 3 mA buffer (FV09)                              | I <sub>OH</sub> |   | −3.00                 |      |      | mA   |
| 6 mA buffer (FV04)                              | I <sub>OH</sub> |   | −3.00                 |      |      | mA   |
| 9 mA buffer (FV01)                              | I <sub>OH</sub> |   | −3.00                 |      |      | mA   |
| 12 mA buffer (FV02)                             | I <sub>OH</sub> |   | −3.00                 |      |      | mA   |
| 18 mA buffer (FV03)                             | I <sub>OH</sub> |   | −6.00                 |      |      | mA   |
| 24 mA buffer (FV06)                             | I <sub>OH</sub> |   | −6.00                 |      |      | mA   |
| Low-level output voltage                        |                 |   |                       |      |      |      |
| LVTTTL output type                              | V <sub>OL</sub> | I <sub>OL</sub> = 0 mA  |                       |      | 0.1  | V    |
| LVTTTL output type (with 5 kΩ pull-up resistor) | V <sub>OL</sub> | I <sub>OL</sub> = 0 mA  |                       |      | 0.2  | V    |
| TTL 5-V withstand voltage output type           | V <sub>OL</sub> | I <sub>OL</sub> = 0 mA  |                       |      | 0.1  | V    |
| 5-V withstand voltage output for CMOS type      | V <sub>OL</sub> | I <sub>OL</sub> = 0 mA  |                       |      | 0.1  | V    |
| High-level output voltage                       |                 |   |                       |      |      |      |
| LVTTTL output type                              | V <sub>OH</sub> | I <sub>OH</sub> = 0 mA  | V <sub>DD</sub> − 0.1 |      |      | V    |
| TTL 5-V withstand voltage output type           | V <sub>OH</sub> | I <sub>OH</sub> = 0 mA  | V <sub>DD</sub> − 0.2 |      |      | V    |

## AC Characteristics

The values in the table below refer to when the supply voltage of the internal gate array block is 3.3 V.

| Parameter              | Symbol           | Conditions                                 | MIN.                               | TYP. | MAX. | Unit |
|------------------------|------------------|--|------------------------------------|------|------|------|
| Toggle frequency       | $f_{\text{tog}}$ | Internal toggle F/F (fanout = 2)           | 670                                |      |      | MHz  |
| Propagation delay time | $t_{\text{PD}}$  | Internal gates                             | Fanout = 1, wiring length 0 mm     | 94   |      | ps   |
|                        |                  |  | Fanout = 1, standard wiring length | 131  |      | ps   |
|                        |                  |  | Standard load                      | 108  |      | ps   |
|                        |                  | Internal gates, power gates, 2NAND         | Fanout = 1, standard wiring length | 107  |      | ps   |
|                        |                  |  | Standard load                      | 94   |      | ps   |
|                        |                  | Input buffers                              | Fanout = 1, standard wiring length | 229  |      | ps   |
|                        |                  |  | Standard load                      | 222  |      | ps   |
|                        |                  | Output buffer (FO01) $C_L = 15 \text{ pF}$ |                                    | 1396 |      | ps   |
| Output rise time       | $t_r$            | Output buffer (FO01) $C_L = 15 \text{ pF}$ |                                    | 2391 |      | ps   |
| Output fall time       | $t_f$            | Output buffer (FO01) $C_L = 15 \text{ pF}$ |                                    | 1872 |      | ps   |

**Remark** Standard load: Fanout = 2, wiring length 0 mm

# TEST DESIGN

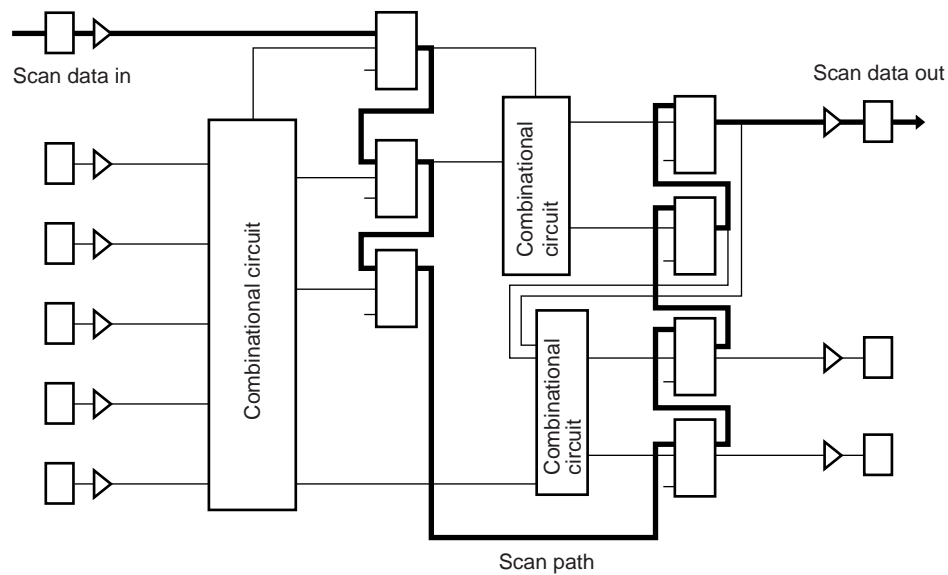
## Scan Path Test

The scan path test is an effective technique in test simplification design. The ATG (Automatic Testpattern Generator) makes it possible to automatically generate a test pattern with high fault coverage.

The features of NEC's scan path test are outlined below.

- Automatic configuration of scan path
- Faults of asynchronous clock detectable
- Check tools for scan path design rule fully provided

Outline of Scan Path Test Method



# DEVELOPMENT TOOLS

## Easy interface with your EWS or PC

Users can choose the following tools to their environment.

**Caution** Some functions may not be supported. Make it sure before use.

### OPENCAD™ V5.3 Configuration Tool

| Function                                | NEC Tool                         | Interface Data                                 | Commercially Available Tool Interface         |
|---|----------------------------------|--|---|
| Function simulator                      | —                                | • Net list<br>PWC/EDIF (2.0.0)/<br>Verilog HDL | ModelSim™ <sup>Note 1</sup> /Verilog-XL™/VCS™ |
| Schematic editor                        | Vdraw™ <sup>Note 1</sup>         |  | —   |
| Logic synthesis                         | —                                |  | Design Compiler™                              |
| Gate-level simulator <sup>Note 2</sup>  | V. sim™ <sup>Note 1</sup>        |  | ModelSim <sup>Note 1</sup> /Verilog-XL/VCS    |
| Formal verifier                         | —                                |  | Formality™                                    |
| STA <sup>Note 2</sup>                   | Tiara <sup>Note 1</sup>          | • Test pattern<br>ALBA/LOGPAT                  | PrimeTime™                                    |
| Fault simulation <sup>Note 3</sup>      | C. FGRADE™                       |  | —   |
| Design for test                         | NEC_SCAN                         |  | Testgen™ <sup>Note 4</sup>                    |
| Floor planner <sup>Note 4</sup>         | ace_floorplan<br>galet_floorplan | • Delay data SDF                               | —   |
| Layout and wiring <sup>Notes 3, 4</sup> | Galet                            |  | Gate Ensemble™<br>Silicon Ensemble™           |

- Notes**
1. Tool supported in the Windows NT™ version
  2. Sign-off tool
  3. Tool not supported in the HP™ version
  4. Individually supported tool

**Remark** Platform : SUN™ (Solaris™)/HP (HP-UX™)/PC-9800 series (Windows NT)/IBM PC/AT™  
(Windows NT)  
GUI : X11R5/Motif™ 1.2/Windows NT

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