Preliminary Data Sheet, Rev. 3
April 2001

Agere USB 2.0 USS2X1W 16-Bit and USS2X1 8-Bit PHY Chips

Introduction

The USS2X1(W) PHY chip provides a serial electrical interface which is compliant with the USB specification revision 2.0. The chip contains sufficient capabilities to allow it to function as a USB 2.0 device when coupled to an intelligent application through its 16-/8-bit interface.

Features

- UTMI/USB 2.0 compliant.
- Operates in both USB 2.0 HS (480 Mbits/s) and USB 1.1 FS (12 Mbits/s) modes.
- Serial-to-parallel and parallel-to-serial conversions.
- All required terminations, including 1.5 kΩ pull-up on DP, are internal to chip.
- Sync field and EOP detection on receive packets.
- Sync field and EOP generation on transmit packets.
- Data and clock recovery from the USB serial stream.
- Bit stuffing/unstuffing; bit stuff error detection.
- Staging register to manage data rate variation due to bit stuffing/unstuffing.
- 16-bit, 30 MHz (8-bit, 60 MHz) parallel interface.
- Ability to switch between full-speed and high-speed terminations and signaling.
- 30 MHz external crystal, plus internal oscillator and PLL used to generate higher-speed internal clocks and CLKOUT output.
- Supports detection of USB reset, suspend, and resume.
- Supports high-speed identification and detection as defined by USB 2.0 specification.
- Supports transmission of resume signaling.
- Supports test modes defined by USB 2.0 specification.
- Supports USB suspend state.
- USS2X1W 64-pin TQFP (16-bit).
- USS2X1 48-pin TQFP (8-bit).

Description

The USS2X1(W) PHY chip may be used in conjunction with an ASIC to provide a two-chip solution for a USB 2.0 device. The chip may also be used in conjunction with FPGAs to prototype a USB 2.0 device. The chip uses a 16-/8-bit parallel interface which is compliant with the *Intel*USB 2.0 Transceiver Macrocell Interface Specification*.

In the transmit direction (to the host), the chip performs parallel-to-serial conversion, plus the required bit stuffing and NRZI encoding. It also generates the required SYNC and EOP fields for outgoing packets. In the receive direction (from the host), the chip performs serial-to-parallel conversion, plus the required bit unstuffing and NRZI decoding. It also detects and strips the SYNC and EOP fields from incoming packets. The receive logic also detects bit stuff error (FS mode only), elasticity buffer underrun or overrun (HS mode only), and byte-alignment errors (either mode).

All device terminations required by the USB 2.0 specification are contained inside the USS2X1(W). This includes the DP/DM 45 Ω termination to ground in HS mode, the DP/DM 45 Ω series termination in FS mode, and the 1.5 kΩ pull-up resistor on DP when in FS mode. The chip also includes appropriate control for the 1.5 kΩ DP pull-up which is needed when switching between FS and HS modes.

The USS2X1(W) supports the high-speed detection sequence defined in the USB 2.0 specification, which is performed after USB reset to determine the highest speed capability of the upstream and downstream entities. The USS2X1(W) has the ability to transmit a chirp K and detect a chirp K/chirp J pattern, as required by the high-speed detection sequence.

The USS2X1(W) supports test modes defined in the USB 2.0 specification which are appropriate for upstream-facing ports: Test_SE0_NAK, Test_J, Test_K, and Test_Packet.

* *Intel* is a registered trademark of Intel Corporation.

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Description (continued)

The USB 2.0 specification requirements for current draw in suspend mode can be met by asserting the SUSPENDN input pin. This turns off internal clocks and the CLKOUT output, and places the internal analog components into low-power mode. When the SUSPENDN input is deasserted, the USS2X1(W) turns on internal clocks, begins asserting the CLKOUT output after internal clocks have stabilized, and returns the internal analog components to their operational state.

Functional Block Diagram

Figure 8 shows the functional block diagram of the USB 2.0 PHY chip. Each block is described below. It is assumed that the control and data interface pins are externally connected to a logic block which performs the next layer of USB processing, such as packet decoding. In this document, the external logic block that performs this function is referred to as the SIE.

Clock Control and PLL

These blocks generate the appropriate internal clocks for the USS2X1(W) and the CLKOUT output signal. An external 30 MHz crystal must be connected to the XI and XO pins to provide a reference clock for these blocks. All data transfer signals are synchronized with the CLKOUT output.

After the deassertion of SUSPENDN, the CLKOUT signal generated by the USS2X1(W) will behave as follows:

- Produce the first CLKOUT transition no later than 5.6 ms after the deassertion of SUSPENDN.
- The CLKOUT signal frequency error will be less than ±10%.
- The CLKOUT signal will fully meet the required accuracy of ±500 ppm, no later than 1.4 ms after the first transition of CLKOUT.

In HS mode, there is one CLK cycle per byte time. The frequency of CLKOUT does not change when the USS2X1(W) is switched between HS and FS modes. In FS mode, there are 5 CLK cycles per FS bit time and 40 CLK cycles per FS byte time. If a received byte contains a stuffed bit, then the byte boundary can be stretched to 45 CLK cycles and two stuffed bits would result in a 50 CLK delay between bytes.

Figure 1 shows the relationship between the CLK and the receive data transfer signals in FS mode. RXActive frames a packet, transitioning only at the beginning and end of a packet. However, transitions of RXValid may take place any time 8 bits of data are available. Figure 1 also shows how RXValid is only asserted for one CLK cycle per byte time even though the data may be presented for the full byte time. The USS2X1(W) will present valid data for the clock cycle while RXValid is asserted.

Figure 2 shows the relationship between CLK and the transmit data transfer signals in FS mode. TXReady is only asserted for one CLK per byte time. This signal acknowledges to the SIE that the data on the DATA input lines has been read by the USS2X1(W) (small arrows above DATA input signal). The SIE must present the next data byte on the DATA input bus after it detects TXReady high on a rising edge of the CLK.

Transitions of TXValid must meet the defined setup and hold times relative to CLK.

The XcvrSelect signal determines whether the HS or FS timing relationship is applied to the data and control signals.

HS CDR

The clock data recovery block recovers the serial 480 Mbits/s data received by the transceiver when in HS mode, as indicated by the XCVRSELECT input.

Elasticity Buffer

As defined in the USB 2.0 specification, this buffer manages any differences between the local clock frequency and the rate at which HS data is received.

The USB specification defines a maximum clock error of ±500 ppm. When the error is calculated over the maximum packet size and when the other system timing margin is taken into consideration, up to ±12 bits of drift can occur. At the start of a packet, the elasticity buffer is filled to a threshold prior to enabling the remainder of the downstream receive logic.

Overflow or underflow conditions detected in the elasticity buffer are reported with the RXError signal.

Transmit Logic

This block is responsible for accepting 16-/8-bit parallel data from the parallel application bus (SIE) interface upon command and serializing it for transmission over the USB 2.0 interface. This module also includes logic for bit stuffing, NRZI encoding, SYNC field, and EOP generation. This block is used for both HS and FS transmit.

Functional Block Diagram (continued)

The transmit logic is controlled in the following manner:

- The SIE asserts TXValid to begin a transmission.
- The SIE negates TXValid to end a transmission.
- After the SIE asserts TXValid, it must assume that the transmission has started when it detects TXReady is asserted.
- The SIE must assume that the USS2X1(W) has consumed a data byte if TXReady and TXValid are asserted.
- The SIE must have valid packet information (PID) asserted on the DATA input bus coincident with the assertion of TXValid. TXReady may be asserted at the same time as TXValid or later.
- TXValid and TXReady are sampled on the rising edge of CLK.
- The transmit logic does **not** automatically generate packet ID (PID) or CRC fields. When transmitting, the SIE is always expected to present a PID field as the first byte of the data stream and, if appropriate, a CRC field as the last byte (bytes) of the data stream.

Figure 2 shows the timing relationship in the FS mode, and Figure 3 shows the timing relationship in the HS mode between TXValid, DATA input, TXReady, and the transmitted data (DP/DM).

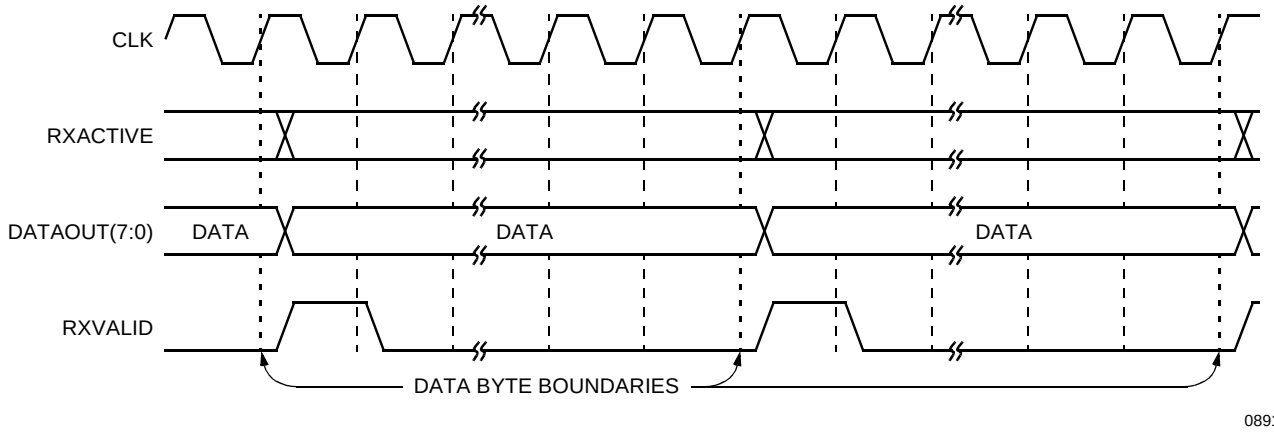


Figure 1. FS CLK Relationship to Receive Data and Control Signals

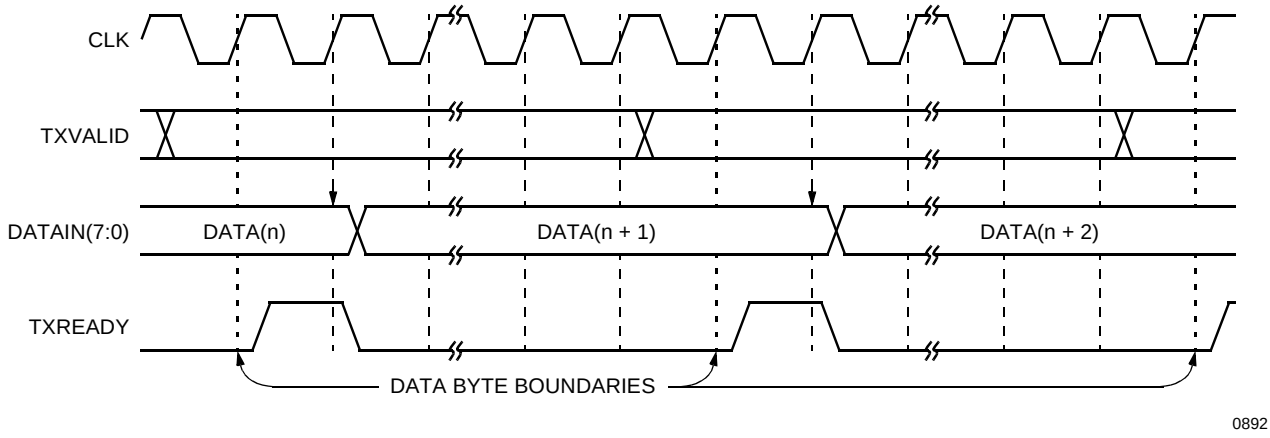


Figure 2. FS CLK Relationship to Transmit Data and Control Signals

Functional Block Diagram (continued)

The SIE negates TXValid to complete a packet. Once negated, the transmit logic will not reassert TXReady until after the EOP has been generated. Note that although the USS2X1(W) transmit logic can be ready to start another packet immediately, the SIE must conform to the minimum interpacket delay identified in the USB 2.0 specification.

In FS mode, if the data transmitter is unable (because of problems such as a buffer underrun condition) to transmit the identical amount of data as was in the original data packet, it must terminate the transaction by generating a bit stuffing violation, followed by an EOP. To accomplish this, the SIE must switch the OpMode to **disable bit stuffing and NRZI encoding** and load zeros into the DATA input lines for at least one byte time before negating TXValid.

In HS mode, if an error condition occurs during transmission, the current transmit stream must be terminated by the transmission of a complemented version of the CRC, followed by an EOP. In this case the SIE will be responsible for presenting the complemented CRC to the DATA input lines before negating TXValid.

In either mode, the negation of TXValid will cause the USS2X1(W) to terminate the packet with the appropriate EOP.

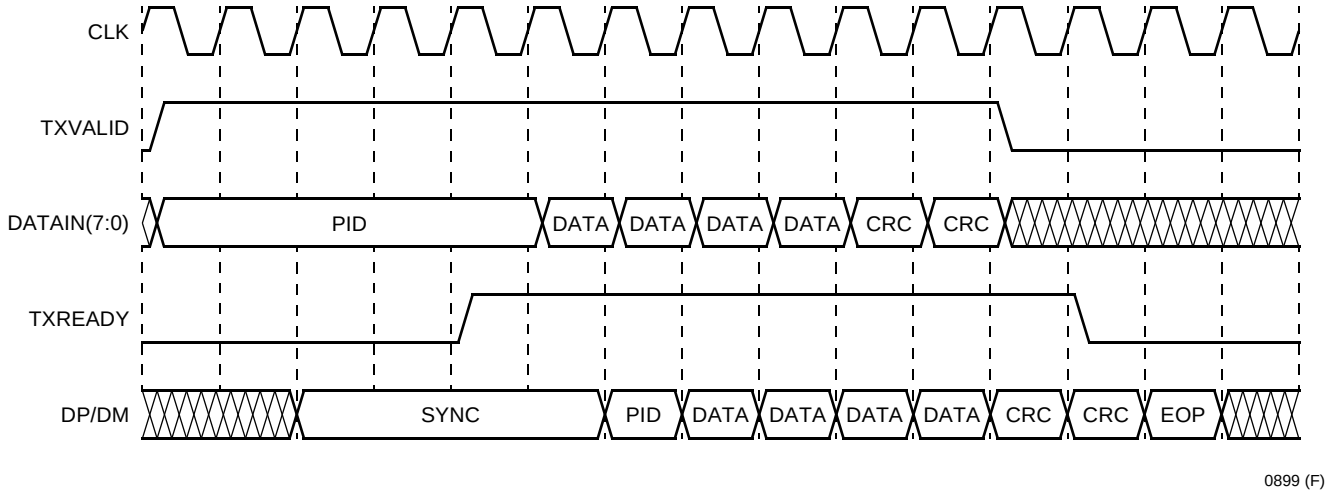


Figure 3. Transmit Timing for a Data Packet

Receive Logic

This block is responsible for deserializing received data recovered by the HS CDR or FS CDR, and providing 16-/8-bit parallel data to the application parallel interface. This module also includes logic for bit unstuffing, NRZI decoding, SYNC field and EOP field detection, and stripping. This block is used for both HS and FS receive.

In FS mode, bit stuff errors assert the RXError signal. In HS mode, bit stuff errors are used to generate the EOP signal so that the RXError signal is not asserted.

The bit rate on USB is constant, however, the bit rate as presented by the USS2X1(W) to the SIE is slightly reduced due to the extraction of inserted 1 bits. Normally, a byte of data is presented on the DATA outputs for every 8 bits received. However, after eight stuffed bits are eliminated from the data stream, a byte time is skipped in the DATA output stream. Figure 4 shows how RXValid is used to skip bytes in the DATA output stream. This example shows the timing in HS mode.

Functional Block Diagram (continued)

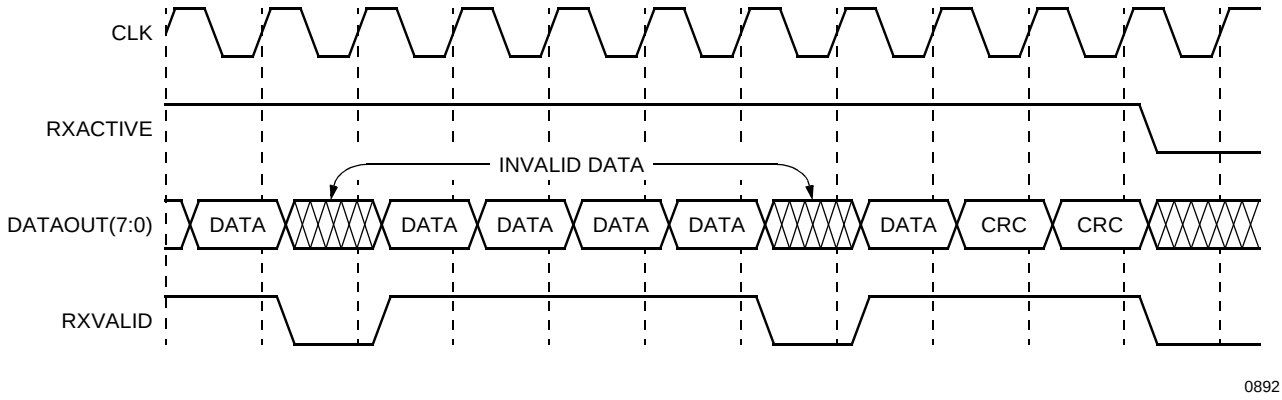


Figure 4. Receive Timing for Data with Unstuffing Bits

The receive logic behavior is controlled/indicated as follows:

- RXActive and RXValid are sampled on the rising edge of CLK.
- The receiver will initially look for SYNC.
- The USS2X1(W) asserts RXActive when SYNC is detected, and will strip the SYNC field.
- The USS2X1(W) negates RXActive when an EOP is detected and will strip the EOP field.
- When RxActive is asserted, RXValid will be asserted if valid data is available on the data outputs.
- RXValid will be negated if valid data is not available on the data outputs. This will occur if 8 stuffed bits have been accumulated.
- The SIE must be ready to consume a data byte if RXActive and RXValid are asserted.
- In FS mode, if a bit stuff error is detected, the receive logic will negate RXActive and RXValid, and return to looking for a SYNC field.

The possible sources of receive errors are as follows:

- Bit stuff error has been detected during an FS receive operation.
- Elasticity buffer overrun.
- Elasticity buffer underun.
- Alignment error, EOP not on a byte boundary.

If a receive error is detected, RXError is asserted. When the last data byte is clocked off the DATA output bus, the SIE must also capture the state of the RXError signal.

Figure 5 shows the timing relationship between the received data (DP/DM), RXValid, RXActive, RXError, and DATA output signals.

Note that the USS2X1(W) does **not** decode packet IDs (PIDs). They are passed to the SIE for decoding.

Note: Figure 5, Figure 6, and Figure 7 are timing examples of the USS2X1(W) when it is in HS mode. When in FS mode, there are approximately 40 CLK cycles every byte time. The receive logic assumes that the SIE captures the data on the DATA output bus if RXActive and RXValid are asserted. In FS mode, RXValid will only be asserted for one CLK per byte time.

Note: The receive section of the USS2X1(W) is disabled when the transmit section is active. The USS2X1(W) does not respond to USB traffic which is transmitting.

Functional Block Diagram (continued)

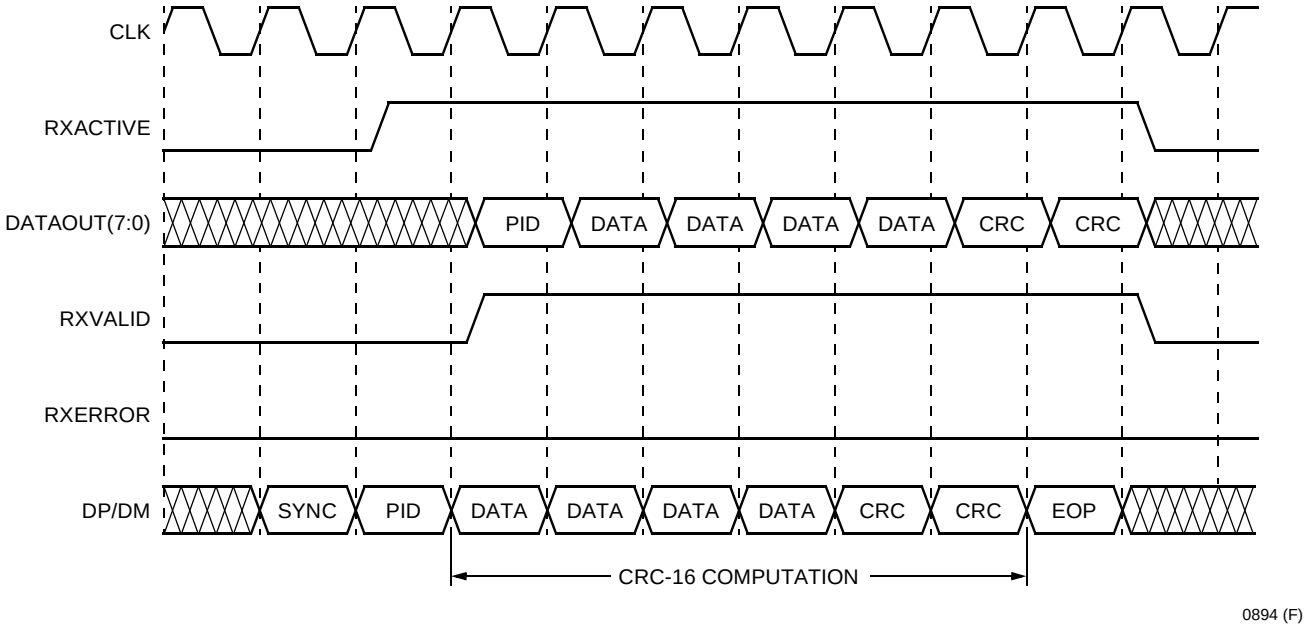


Figure 5. Receive Timing for Data Packet (with CRC-16)

Note: In Figure 5, Figure 6, and Figure 7, the SYNC pattern on DP/DM is shown as one byte long. The SYNC pattern received by a device can vary in length, these figures assume that all but the last 12 bits have been consumed by the hubs between the device and the host controller.

Note: In Figure 5, Figure 6, and Figure 7, the packet displayed on DP/DM is pipelined by the USS2X1(W) and may occur several bit times, or even several byte times earlier, relative to the USS2X1(W) signal transitions (RXActive, DATA output, RXValid, etc.).

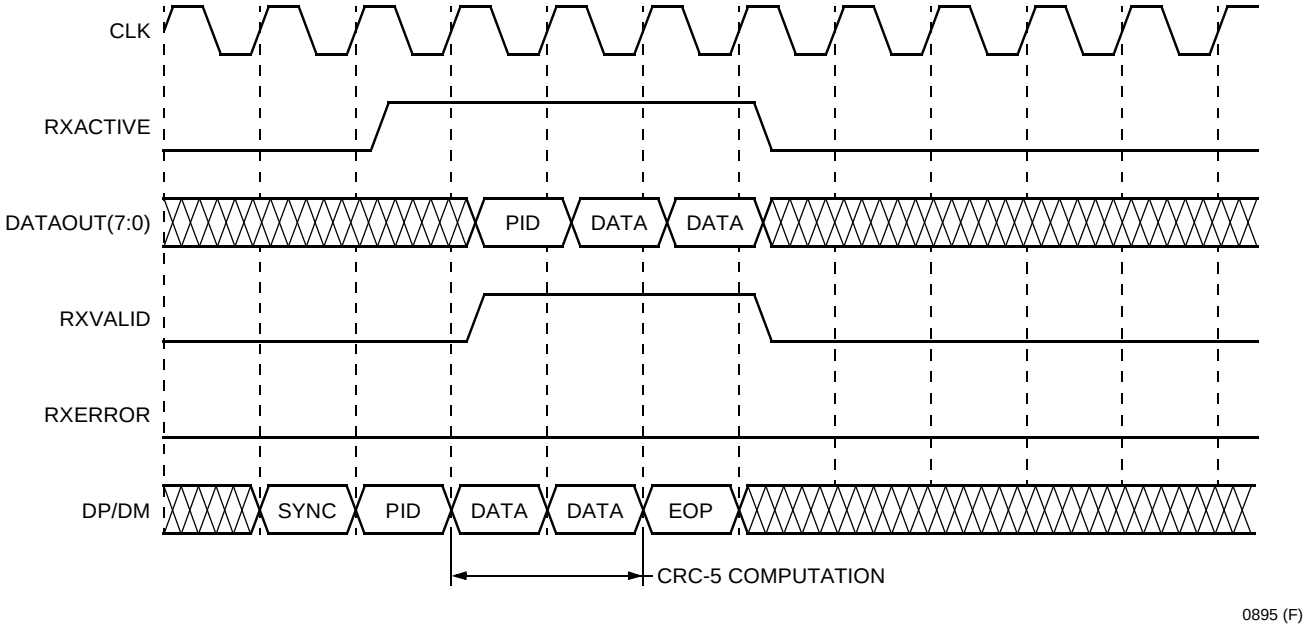


Figure 6. Receive Timing for Setup Packet

Functional Block Diagram (continued)

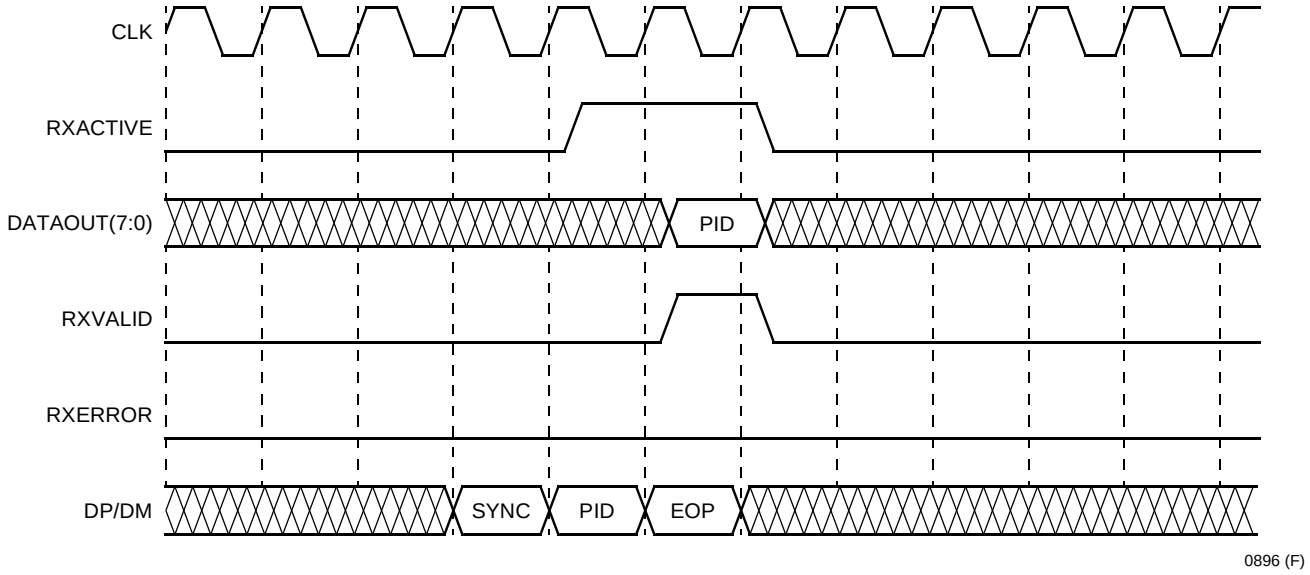


Figure 7. Receive Timing for a Handshake Packet (No CRC)

USB Transceiver

The USB transceiver is capable of transmitting and receiving at the HS or FS bit rates and edge rates, as controlled by the XCVRSELECT input. The transceiver also detects line inactivity (squelch) and the line state in both HS and FS modes. All termination resistors required by the USB 2.0 specification are located internally, and are controlled by the TERMSELECT input.

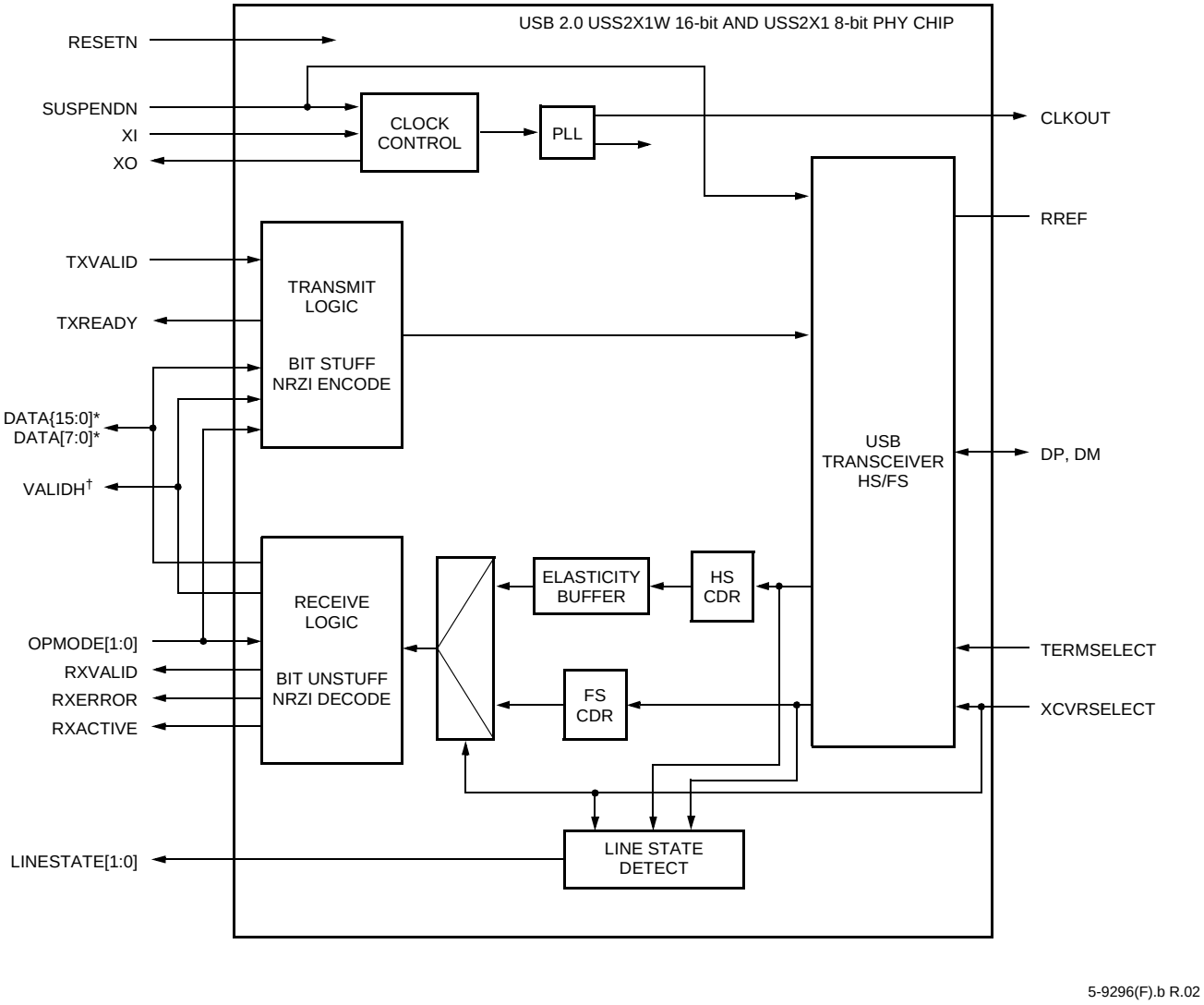
FS CDR

Recovers the serial 12 Mbits/s data received by the transceiver when in FS mode, as indicated by the XCVRSE-LECT input. This block also accounts for any differences between the local clock frequency and the rate at which FS data is received.

Line State Detect

Reports the logic state received from either the HS or FS output of the transceiver.

Functional Block Diagram (continued)



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* DATA[15:0] only exists on the 16-bit PHY chip, and DATA[7:0] only exists on the 8-bit PHY chip.
† VALIDH only exists on the 16-bit PHY chip.

Figure 8. USB 2.0 USS2X1W 16-Bit and USS2X1 8-Bit PHY Chips

Pin Information

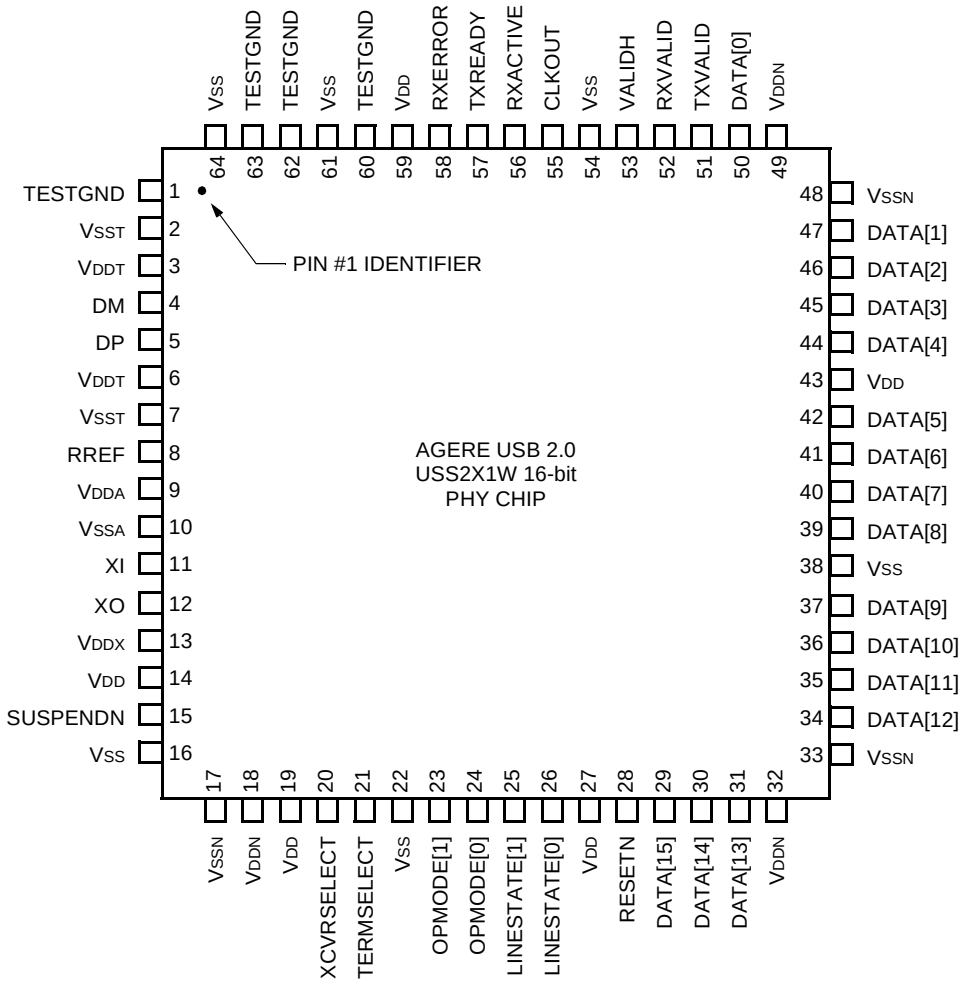

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Figure 9. 64-Pin TQFP Package Pin Assignments

Pin Information (continued)

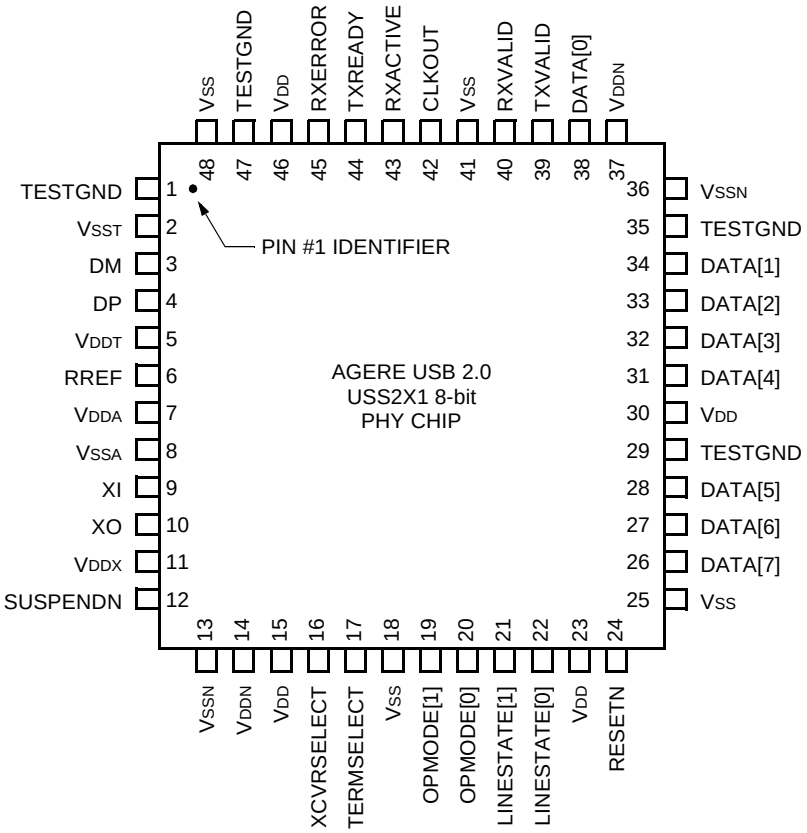

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Figure 10. 48-Pin TQFP Package Pin Assignments

Control Interface Signals

Table 1. Control Interface Signals

Pin Number (64-Pin)	Pin Number (48-Pin)	Name	Direction	Active Level	Description
11	9	XI	Input	NA	**Oscillator Input**. Connect to external 30 MHz crystal.
12	10	XO	Output	NA	**Oscillator Output**. Connect to external 30 MHz crystal.
55	42	CLKOUT	Output	NA	**Clock**. This output is used for clocking receive and transmit parallel data. 60 MHz (8-bit only). 30 MHz (16-bit only).
28	24	RESETN	Input	Low	**Reset**. Hardware reset.
20	16	XCVR-SELECT	Input	NA	**Transceiver Select**. This signal selects between the FS and HS transceivers: 0: HS transceiver enabled. 1: FS transceiver enabled.
21	17	TERM-SELECT	Input	NA	**Termination Select**. This signal selects between the FS and HS terminations: 0: HS termination enabled. 1: FS termination enabled.
15	12	SUSPENDN	Input	Low	**Suspend**. Places the USS2X1(W) in a mode that draws minimal power from supplies. Shuts down all blocks not necessary for suspend/resume operation. While suspended, TERMSELECT must always be in FS mode to ensure that the 1.5 kΩ pull-up on DP remains powered. 0: USS2X1(W) drawing suspend current. 1: USS2X1(W) drawing normal current.
25, 26	21, 22	LINESTATE [1:0]	Output	NA	**Line State**. While the device is suspended and while the device is resuming from a suspended state, these signals are combinatorial, i.e., directly reflect the current state of the DM and DP signals. Otherwise, these signals are synchronized to the CLKOUT output. DM DP Description 0 0 0: SE0 0 1 1: J state 1 0 2: K state 1 1 3: SE1
23, 24	19, 20	OPMODE [1:0]	Input	NA	**Operational Mode**. These signals select between various USS2X1(W) operational modes: OPMODE [1:0] Description 0 0 0: Normal operation 0 1 1: Nondriving all terminations removed 1 0 2: Disable bit stuffing and NRZI encoding 1 1 3: Reserved

USB Interface and Data Input/Output Signals

Table 2. USB Interface Signals

Pin Number (64-Pin)	Pin Number (48-Pin)	Name	Direction	Active Level	Description
5	4	DP	Bidir	NA	**USB Data Pin Data+**.
4	3	DM	Bidir	NA	**USB Data Pin Data–**.
8	6	RREF	NA	NA	**External Reference**. Requires 1% precision 1 kΩ resistor to ground.

Table 3. Data Input/Output Signals (16-Bit Transmit and Receive)

Pin Number (64-Pin)	Name	Direction	Active Level	Description			
29—31, 34—37, 39—42, 44—47, 50	DATA [15:0]*	Bidir	NA	**TXVALID**	**RXVALID**	**VALIDH**	**DATA[15:0]**
				0	0	X	Not in use.
				0	1	0	Data [7:0] output is valid for receive.
				0	1	1	Data [15:0] output is valid for receive.
				1	X	0	Data [7:0] output is valid for transmit.
				1	X	1	Data [15:0] output is valid for transmit.
53	VALIDH*	Bidir	High	If TXVALID = 1, this chip's input, when asserted, it indicates that the entire 16-bit DATA input is to be transmitted over USB. If deasserted, it indicates that only DATA [7:0] is to be transmitted. If TXVALID = 0 and RXVALID = 1, this chip's output, when asserted, it indicates that the entire 16-bit DATA output is valid. If deasserted, it indicates that only DATA [7:0] is valid.			

* Pull-down resistance is 50 kΩ nominal.

Table 4. Data Input/Output Signals (8-Bit Transmit and Receive)

Pin Number (48-Pin)	Name	Direction	Active Level	Description		
26—28, 31—34, 38	DATA [7:0]	Bidir	NA	**TXVALID**	**RXVALID**	**DATA[7:0]**
				0	0	Not in use.
				0	1	Data [7:0] output is valid for receive.
				1	X	Data [7:0] output is valid for transmit.

Data Input Signals

Table 5. Data Input Signals (Transmit)

Pin Number (64-Pin)	Pin Number (48-Pin)	Pin Name	Pin Direction	Active Level	Description
51	39	TXVALID	Input	High	**Transmit Valid**. Indicates that the DATA bus is a valid input. The assertion of TXVALID initiates SYNC on the USB. The negation of TXVALID initiates EOP on the USB.
57	44	TXREADY	Output	High	**Transmit Data Ready**. Indicates that the transmitter requires data. The application must have data available for clocking in to the DATA inputs on the rising edge of CLK. If TXVALID is negated, TXREADY can be ignored by the application.

Table 6. Data Output Signals (Receive)

Pin Number (64-Pin)	Pin Number (48-Pin)	Pin Name	Pin Direction	Active Level	Description
52	40	RXVALID	Output	High	**Receive Data Valid**. Indicates that the DATA bus has valid data. The application is expected to latch the DATA bus on the clock edge.
56	43	RXACTIVE	Output	High	**Receive Active**. Indicates that the receive state machine has detected SYNC and is active. **RXActive** is negated after a bit stuff error or an EOP is detected.
58	45	RXERROR	Output	High	**Receive Error.** 0: Indicates no error. 1: Indicates that a receive error has been detected. Possible sources of errors are as follows: ■ Bit stuff error has been detected during a FS receive operation. ■ Elasticity buffer overrun. ■ Elasticity buffer underrun. ■ Alignment error, EOP not on a byte boundary.

Power/Test Interface Signals

Table 7. Power/Test Signals

Pin Number (64-Pin)	Pin Number (48-Pin)	Pin Name	Pin Direction	Active Level	Description
14, 19, 27, 43, 59	15, 23, 30, 46	V_{DD}	NA	NA	**Chip Power**. V_{DD} = 3.3 V ± 5%
16, 22, 38, 54, 61, 64	18, 25, 41, 48	V_{SS}	NA	NA	**Chip Ground**.
18, 32, 49	14, 37	V_{DDN}	NA	NA	**IO Power**.
17, 33, 48	13, 36	V_{SSN}	NA	NA	**IO Ground**.
10	8	V_{SSA}	NA	NA	**Analog Ground**.
3, 6	5	V_{DDT}	NA	NA	**Transceiver Power**.
2, 7	2	V_{SST}	NA	NA	**Transceiver Ground**.
9	7	V_{DDA}	NA	NA	**Analog Power**.
13	11	V_{DDX}	NA	NA	**Oscillator Power**.
1, 60, 62, 63	1, 29, 35, 47	TESTGND	Input	High	**Test Ground**. Inputs for hardware test modes. Must be connected to ground.

Electrical Characteristics

dc Characteristics

Table 8. dc Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Supply Power Voltage	—	3.135	3.3	3.465	V
Vih	Input High Threshold	—	2.0	—	—	V
Vil	Input Low Threshold	—	—	—	0.8	V
Voh	Output High Voltage	i ≤ –6mA	2.4	—	—	V
Vol	Output Low Voltage	i ≤ 6mA	—	—	0.4	V
Cin	Input Pin Capacitance	—	—	—	2.0	pF
Cbid	Bidi Pin Capacitance	—	—	—	3.0	pF
Cout	Output Pin Capacitance	—	—	—	2.5	pF
P_{totA}	Total Power Active	V_{DD} = 3.3 V, 25 °C	—	—	445	mW
P_{totB}	Total Power Suspend	V_{DD} = 3.3 V, 25 °C	—	—	10	mW

ac Characteristics

Table 9. ac Characteristics

Symbol	Signal	Condition	Min	Typ	Max	Unit	Notes
Tri	All	$0.2V_{DD}$—$0.6V_{DD}$	—	0.8	—	ns	Input rise time.
Tfi	All	$0.6V_{DD}$—$0.2V_{DD}$	—	0.8	—	ns	Input fall time.
Tro	Data	$0.2V_{DD}$—$0.6V_{DD}$, 10 pF	—	—	0.8	ns	Output rise time.
Tro	Others	$0.2V_{DD}$—$0.6V_{DD}$, 10 pF	—	—	0.6	ns	Output rise time.
Tfo	Data	$0.2V_{DD}$—$0.6V_{DD}$, 10 pF	—	—	0.8	ns	Output fall time.
Tfo	Others	$0.6V_{DD}$—$0.2V_{DD}$, 10 pF	—	—	0.6	ns	Output fall time.

Electrical Characteristics (continued)

ac Timing

Table 10. ac Timing (16-Bit)

Symbol	Signal	Condition	Min	Typ	Max	Unit	Notes
Tsu	DATA[15:0]	3.135 V, 125 °C	8	—	—	ns	Setup from signal to CLKOUT.
	TXVALID		10	—	—	ns	
	VALIDH		10	—	—	ns	
	OPMODE[1]		10	—	—	ns	
	OPMODE[0]		11	—	—	ns	
	XCVRSELECT		TBD	—	—	ns	
	TERMSELECT		TBD	—	—	ns	
	SUSPENDN		TBD	—	—	ns	
Thd	DATA[15:0]	3.465V, 125 °C	0	—	—	ns	Hold from signal to CLKOUT.
	TXVALID		0	—	—	ns	
	VALIDH		0	—	—	ns	
	OPMODE[1]		0	—	—	ns	
	OPMODE[0]		0	—	—	ns	
	XCVRSELECT		0	—	—	ns	
	TERMSELECT		0	—	—	ns	
	SUSPENDN		TBD	—	—	ns	
Tpd	DATA[15:0]	10 pF Min: 3.135 V, 125 °C Max: 3.465 V, 0 °C	0	—	21	ns	Prop delay from CLKOUT to signal.
	RXVALID		0	—	20	ns	
	VALIDH		0	—	21	ns	
	RXERROR		0	—	5	ns	
	RXACTIVE		0	—	18	ns	
	LINESTATE[1:0]		0	—	33	ns	
	TXREADY		0	—	27	ns	

Electrical Characteristics (continued)

Table 11. ac Timing (8-Bit)

Symbol	Signal	Condition	Min	Typ	Max	Unit	Notes
Tsu	DATA[15:0]	3.135 V, 125 °C	8	—	—	ns	Setup from signal to CLKOUT.
	TXVALID		10	—	—	ns	
	VALIDH		NA	—	—	ns	
	OPMODE[1]		10	—	—	ns	
	OPMODE[0]		11	—	—	ns	
	XCVRSELECT		TBD	—	—	ns	
	TERMSELECT		TBD	—	—	ns	
	SUSPENDN		TBD	—	—	ns	
Thd	DATA[15:0]	3.465V, 125 °C	0	—	—	ns	Hold from signal to CLKOUT.
	TXVALID		0	—	—	ns	
	VALIDH		NA	—	—	ns	
	OPMODE[1]		0	—	—	ns	
	OPMODE[0]		0	—	—	ns	
	XCVRSELECT		0	—	—	ns	
	TERMSELECT		0	—	—	ns	
	SUSPENDN		TBD	—	—	ns	
Tpd	DATA[15:0]	10 pF Min: 3.135 V, 125 °C Max: 3.465 V, 0 °C	0	—	4	ns	Prop delay from CLKOUT to signal.
	RXVALID		0	—	3	ns	
	VALIDH		NA	—	NA	ns	
	RXERROR		0	—	5	ns	
	RXACTIVE		0	—	3	ns	
	LINESTATE[1:0]		0	—	6	ns	
	TXREADY		0	—	11	ns	

Operational Modes

The OpMode signals are capable of inhibiting normal operation of the transceiver and evoking special test modes. These modes take effect immediately and take precedence over any pending data operations. The transmission data rate when in any OpMode depends on the state of the XcvrSelect input. There are three valid settings for OpMode:

- Normal operation (0)
- Nondriving (1)
- Disable bit stuffing and NRZI encoding (2)

Mode 0 allows the transceiver to operate with normal USB data decoding and encoding.

Mode 1 allows the transceiver logic to support a soft disconnect feature which 3-states both the HS and FS transmitters, and removes any termination from the USB making it appear to an upstream port that the device has been disconnected from the bus. In this mode, the receive logic is still active.

Mode 2 disables the bit stuff and NRZI encoding logic therefore, 1s loaded from the DATA input bus become Js on the DP/DM lines and 0s become Ks. Note that this mode effects the automatic SYNC pattern and EOP generation by TXValid, which is disabled so that chirps can be generated on the USB. The operation of the receiver is undefined.

Note that the OpMode signals are normally changed only when the transmitter and the receiver are quiescent, i.e., when entering a test mode or for a device initiated resume, the OPMode is set and then TXValid is asserted. In this case, the SYNC pattern and EOP are not transmitted by the USS2X1.

The only exception is when the OPMode signals are set to mode 2 while TXValid is asserted (the transceiver is transmitting a packet), in order to flag an FS transmission error. See the Transmit Logic section for more information. In this case, the SYNC pattern has already been transmitted by the USS2X1. Therefore, upon the negation of TXValid the EOP must also be transmitted to properly terminate the packet.

Changing the OPMode signals under all other conditions, while the transceiver is receiving or transmitting data will generate undefined results. Setting OpMode to 3 will also produce undefined results.

USB 2.0 Test Mode Generation

The USB specification defines additional test modes. These are accomplished with the following techniques:

- To force an SE0 state on the bus, the USS2X1 is placed in OpMode 0 (normal operation) and no data is transmitted. This results in an HS idle mode on the bus, which is SE0. It is the responsibility of the SIE to validate any incoming packets and to transmit a NAK handshake packet, if the received packet is correct.
- To force a J state on the bus, the USS2X1 is placed in OpMode 2 (disable bit stuffing and NRZI encoding) and all 1s are transmitted by the SIE.
- To force a K state on the bus, the USS2X1 is placed in OpMode 2 (disable bit stuffing and NRZI encoding) and all 0s are transmitted by the SIE.
- To generate a test packet on the bus the USS2X1 is placed in OpMode 0 (normal operation) and all the test packet data (as defined in Chapter 7 of the USB 2.0 specification) is transmitted by the SIE.

Table 12. USB 2.0 Test Mode to USS2X1 Mapping

USB 2.0 Test Modes	USS2X1 Setup		
	Operational Mode	Transmitted Data	XcvrSelect & TermSelect
SE0_NAK	Normal	No transmit	HS
J	Disable	All 1s	HS
K	Disable	All 0s	HS
Test_Packet	Normal	Test packet data	HS

Note: The Test Force_Enable mode described in the USB 2.0 specification does not apply to upstream facing ports.

Operational Modes (continued)

Speed Selection

The XcvrSelect and TermSelect signals determine whether the device is in HS or FS mode, enabling the respective transceiver and termination. The HS detection handshake protocol requires independent control of transceivers and terminations, where the device enables FS terminations but is required to drive and listen to the bus with the HS transceiver. In all other cases, the state of the XcvrSelect and TermSelect signals are identical.

16-Bit Interface

The 64-pin package, USS2X1W supports a 16-bit data interface. The operation of the 16-bit version differs from that of the 8-bit version as follows:

- CLKOUT will run at half the rate of the equivalent 8-bit version (30 MHz).
- An additional signal (ValidH) is used to identify whether the high byte of the respective 16-bit data word is valid.
- Additional data pins are provided (DATA 15:8).
- The TXReady signal will drop low for one clock period each time 16 stuffed bits are accumulated. With the 8-bit interface, the TXReady signal will drop low after the accumulation of 8 stuffed bits.
- The RXValid signal will drop low for one clock period each time 16 stuffed bits are accumulated. With the 8-bit interface, the RXValid signal will drop low after the accumulation of 8 stuffed bits.

Note that the other sections of this document assume that the USS2X1 is operating with an 8-bit interface. The timings need to be adjusted appropriately for operation using a 16-bit interface.

Operational Modes (continued)

16-Bit Transmit Timing

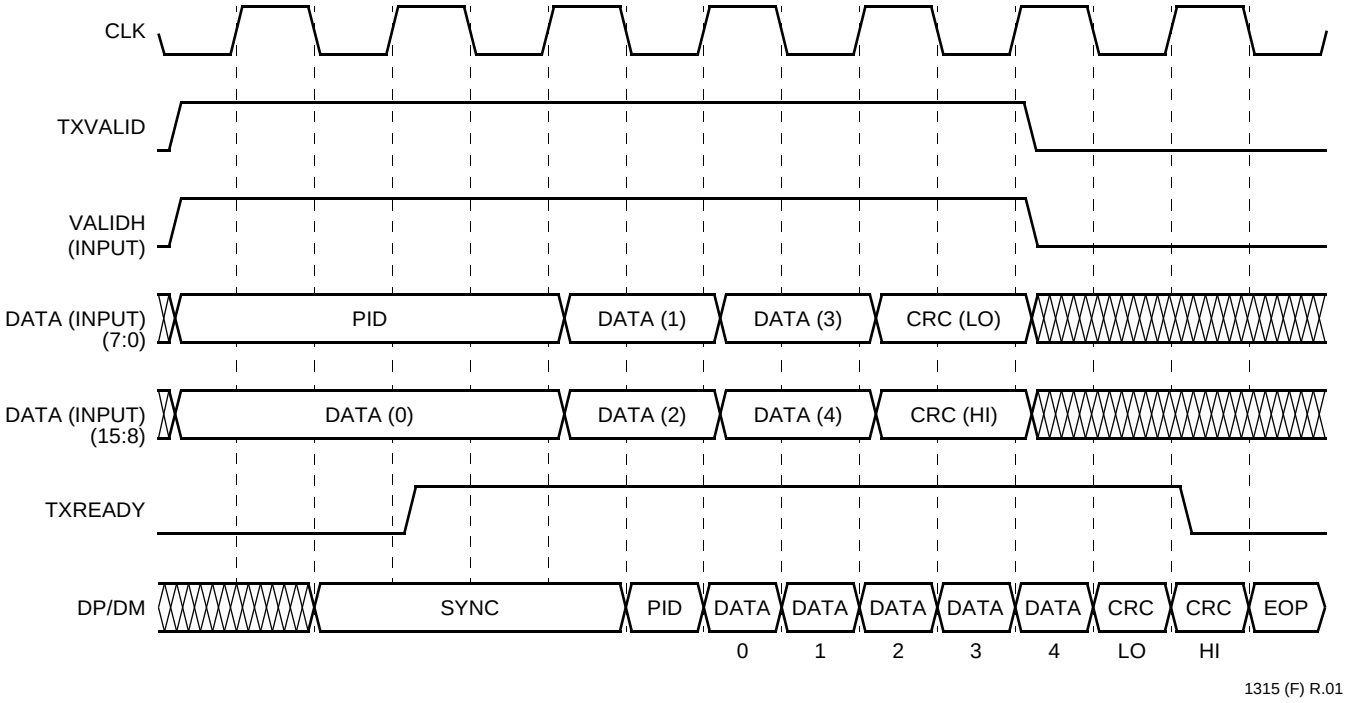

Figure 11. Transmit Timing for 16-Bit Data, Even Byte Count

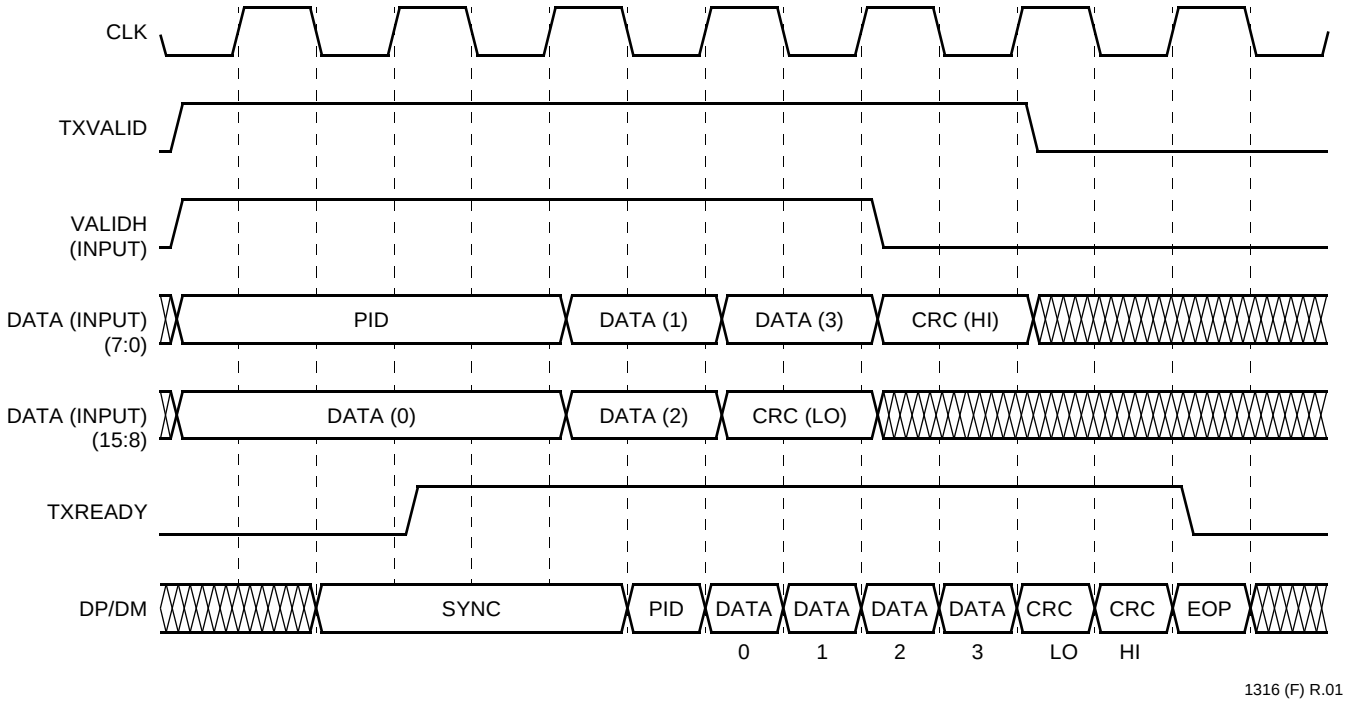

Figure 12. Transmit Timing for 16-Bit Data, Odd Byte Count

Operational Modes (continued))

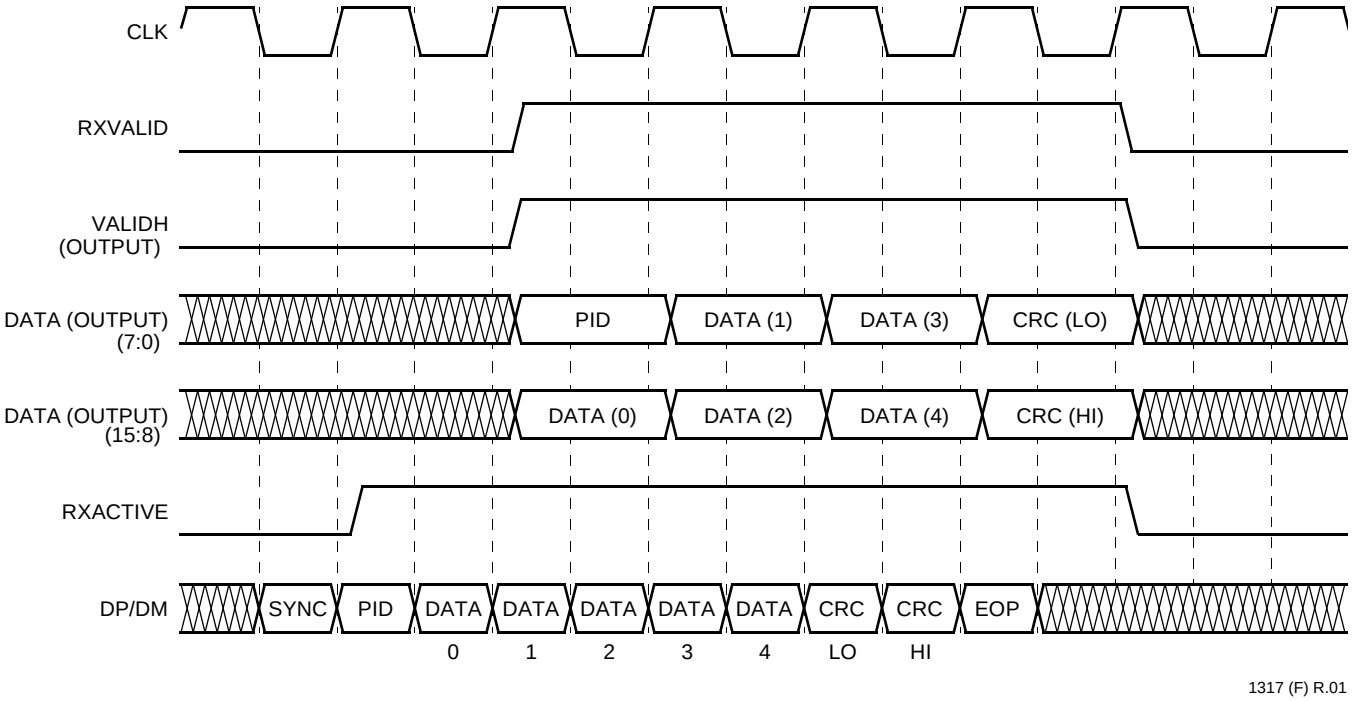

Figure 13. Receive Timing for 16-Bit Data, Even Byte Count

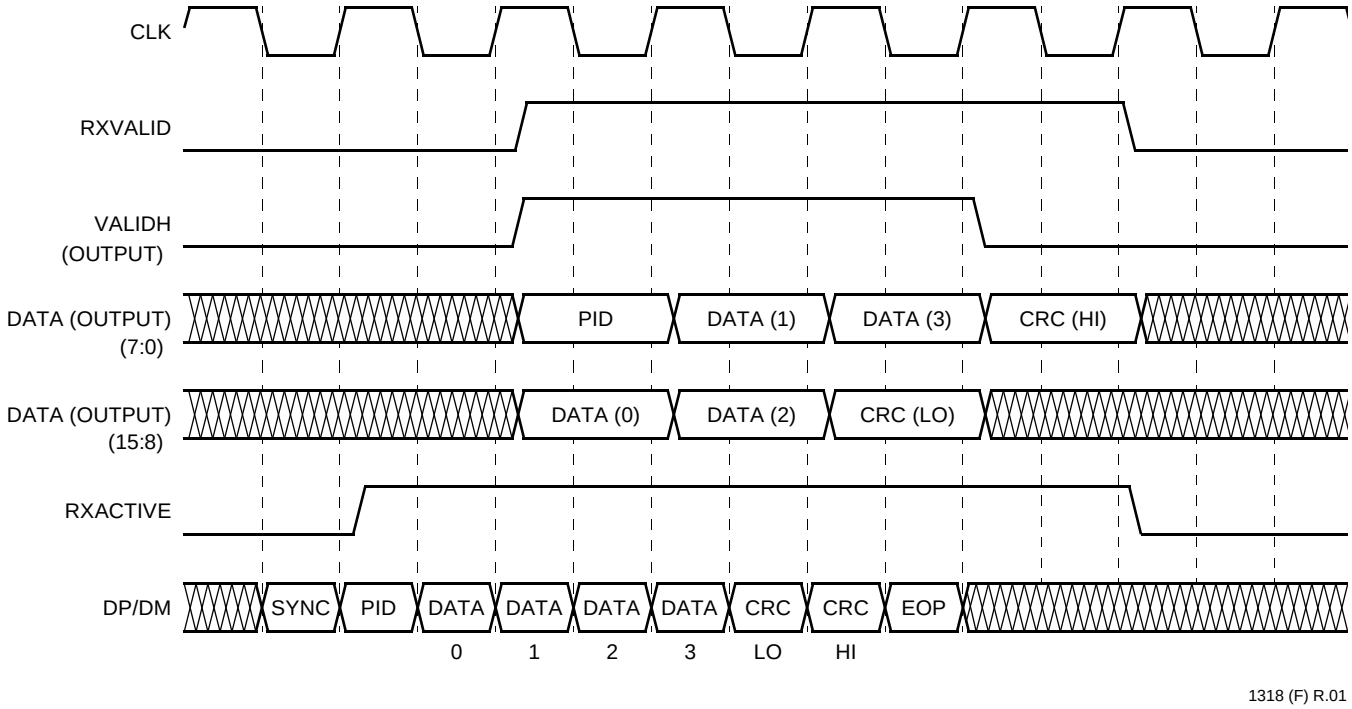

Figure 14. Receive Timing for 16-Bit Data, Odd Byte Count

Other Functions

The LineState signals are used for many functions. The LineState signals reflect the current state of the DP/DM signal lines. The thresholds used by the LineState to determined the state of DP/DM depend on the value of XcvrSelect. LineState uses HS thresholds when the HS termination is enabled (XcvrSelect = 0) and FS thresholds when the FS transceiver is enabled (XcvrSelect = 1).

The following sections make a distinction between soft SE0 and driven SE0. Soft SE0 is the bus signaling that results from the DP and DM signal lines being pulled down exclusively by the 15 kΩ pull-down resistors (Rpd). Driven SE0 is the result of generating an SE0 condition by enabling the FS transmitter. In this case, the DP and DM signal lines are being pulled down by the 45 Ω serial (Rs) termination resistors.

Note that Rpd and Rs are defined in Figure 7.1 of the USB 2.0 specification.

SE0 Handling

For full-speed operation, idle is a J state on the bus and SE0 is used as part of the EOP or to indicate reset. When asserted in an EOP, SE0 is never asserted on the bus for more than two low-speed bit times (1.3 μs). The assertion of SE0 for more than 2.5 μs is interpreted as a reset by a full-speed device.

For high-speed operation, idle is an SE0 state on the bus. SE0 is also used to reset a high-speed device. A high-speed device cannot use the 2.5 μs assertion of SE0 (as defined for FS operation) to indicate reset since the bus is often in this state between packets. If no bus activity (idle) is detected for more than 3 ms, a high-speed device must determine whether the downstream port is signaling a suspend or a reset. The Suspend Detection and Reset Detection sections detail how this determination is made. If a reset is signaled, the high-speed device will then initiate the HS detection handshake protocol, as defined in the HS Detection Handshake section.

Note that the initial assertion of SE0 on the bus is referred to in the core specification and this specification as HS Reset T0 (see Section 7.1.7.5 Reset Signaling of the USB 2.0 specification, Rev. 2).

Other Functions (continued)

Suspend Detection

If an HS device detects SE0 asserted on the bus for more than 3 ms (T1) its USS2X1 is placed in FS mode (XcvrSelect and TermSelect = 1). This enables the FS pull-up on the DP line, asserting a continuous FS J state on the bus. The SIE must then check the LineState signals for a J state condition. If J state condition is asserted at time T2, then the upstream port is asserting a soft SE0 and the USB is in a J state indicating a suspend condition. By time T4, the device must be fully suspended.

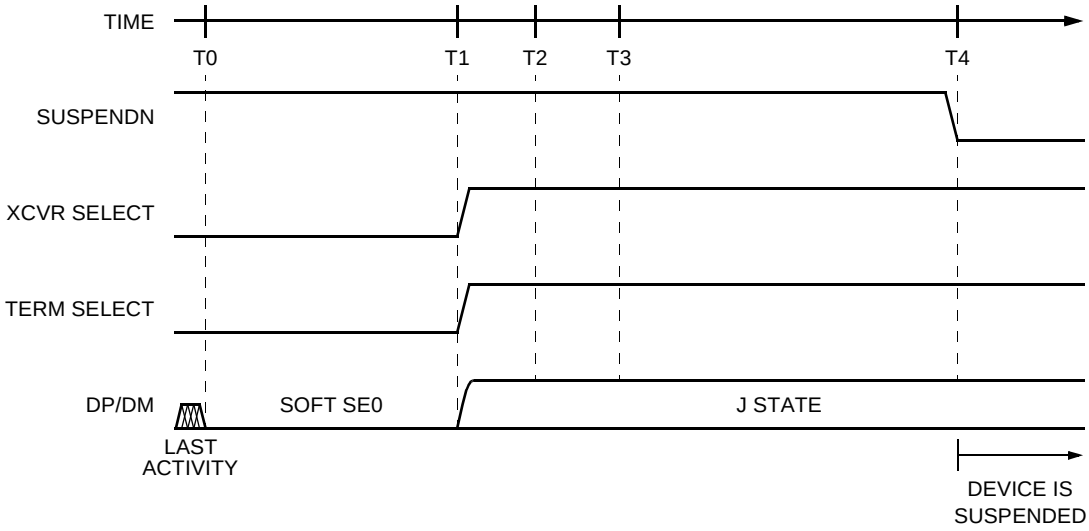

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Figure 15. Suspend Timing Behavior (HS Mode)

Table 13. Suspend Timing Values (HS Mode)

Timing Parameter	Description	Value
HS Reset T0	End of last bus activity, signaling either a reset or a suspend.	0 (reference)
T1	The time at which the device must place itself in FS mode after bus activity stops.	HS reset T0 + 3.0 ms < T1 {TWTREV} < HS reset T0 + 3.125 ms
T2	SIE samples LineState. If LineState = J, then the initial SE0 on the bus (T0—T1) had been due to a suspend state and the SIE remains in HS mode.	T1 + 100 µs < T2 {TWTWRSTHS} < T1 + 875 µs
T3	The earliest time where a device can issue resume signaling.	HS reset T0 + 5 ms {TWTRSM}
T4	The latest time that a device must actually be suspended, drawing no more than the suspend current from the bus.	HS reset T0 + 10 ms {T2SUSP}

Note: USB 2.0 core specification timing values are referenced in curly braces {}.

Other Functions (continued)

Reset Detection

If a device in HS mode detects bus inactivity for more than 3 ms (T1) its USS2X1 is placed in FS mode (XcvrSelect = 1 and TermSelect = 1). This enables the FS pull-up on the DP line to attempt to assert a continuous FS J state on the bus (dotted line in Figure 16). The SIE must then check the LineState signals for the SE0 condition. If SE0 is asserted at time T2, then the upstream port is forcing the reset state to the device (i.e., driven SE0). The device will then initiate the HS detection handshake protocol.

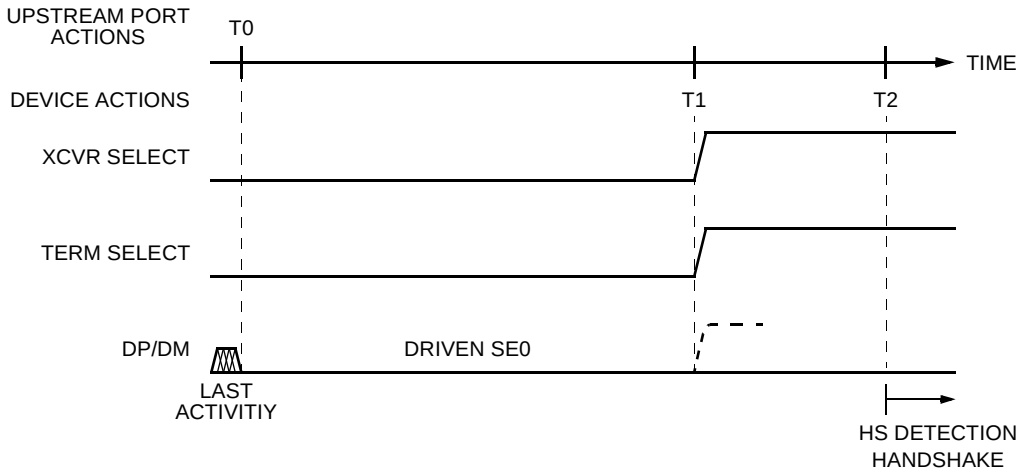

Figure 16. Reset Timing Behavior (HS Mode)

Table 14. Reset Timing Values (HS Mode)

Timing Parameter	Description	Value
HS Reset T0	Bus activity ceases, signaling either a reset or a suspend.	0 (reference)
T1	Earliest time at which the device may place itself in FS mode after bus activity stops.	HS reset T0 + 3.0 ms < T1 {T_{WTREV}} < HS reset T0 + 3.125 ms
T2	SIE samples LineState. If LineState = SE0, then the SE0 on the bus is due to a reset state. The device now enters the HS detection handshake protocol.	T1 + 100 µs < T2 {$T_{WTWRSTHS}$} < T1 + 875 µs

Other Functions (continued)

HS Detection Handshake

The high-speed detection handshake process is entered from one of three states: suspend, active FS, or active HS. The downstream port asserting an SE0 state on the bus initiates the HS detection handshake. Depending on the initial state, an SE0 condition can be asserted from 0 to 4 ms before initiating the HS detection handshake. These states are described in section 7.1.7.5 of the USB 2.0 specification, Rev. 2 (state 3 of the reset protocol for HS capable hubs and devices).

There are three ways in which a device may enter the HS handshake detection process:

1. If the device is suspended and it detects an SE0 state on the bus, it may immediately enter the HS handshake detection process.
2. If the device is in FS mode and an SE0 state is detected for more than 2.5 µs, it may enter the HS handshake detection process.
3. If the device is in HS mode and an SE0 state is detected for more than 3.0 ms, it may enter the HS handshake detection process. In HS mode, a device must first determine whether the SE0 state is signaling a suspend or a reset condition. To do this, the device reverts to FS mode by placing XcvrSelect and TermSelect into FS mode. The device must not wait more than 3.125 ms before the reversion to FS mode. After reverting to FS mode no less than 100 µs and no more than 875 µs later, the SIE must check the LineState signals. If a J state is detected, the device will enter a suspend state. If an SE0 state is detected, then the device will enter the HS handshake detection process.

In each case, the assertion of the SE0 state on the bus initiates the reset interval (referred to in this section as HS reset T0). The minimum reset interval is 10 ms. Depending on the previous mode that the bus was in, the delay between the initial assertion of the SE0 state (HS reset T0) and entering the HS handshake detection process (T0 in Table 15, Table 16, and Table 17 can be from 0 to 4 ms.

The USS2X1 relies on the SIE to perform much of the event timing, and the SIE requires a stable CLKOUT signal to perform accurate timing. In cases 2 and 3 above CLKOUT has been running and is stable, however in case 1 the USS2X1 is reset from a suspend state, and the internal oscillator and clocks of the transceiver are powered down. A device has up to 6 ms after the release of SuspendN (HS reset T0) to assert a minimum of a 1 ms Chirp K. The Clock Control and PLL section describes the behavior of the USS2X1 which allows it to reliably generate a 1 ms Chirp K.

FS Downstream Facing Port

The following is an example of the USS2X1 behavior when the downstream facing port that it is attached to does not support HS operation (a USB1.X host/hub).

Upon entering the HS detection process (T0) XcvrSelect and TermSelect are in FS mode. The D+ pull-up is asserted and the HS terminations are disabled. The SIE then sets OpMode to disable bit stuffing and NRZI encoding, and begins the transmission of all 0s data, which asserts a HS K (chirp) on the bus (T1). The device chirp must last at least 1.0 ms and must end no later than 7.0 ms after HS reset T0. At time T1, the SIE sets XcvrSelect to HS mode and begins listening for a chirp sequence from the downstream port.

If the downstream port is not HS capable, then the HS K asserted by the device is ignored and the alternating sequence of HS chirp Ks and Js is not generated. If the downstream chirps are not detected (T4), the device will enter FS mode by returning XcvrSelect to FS mode.

Other Functions (continued)

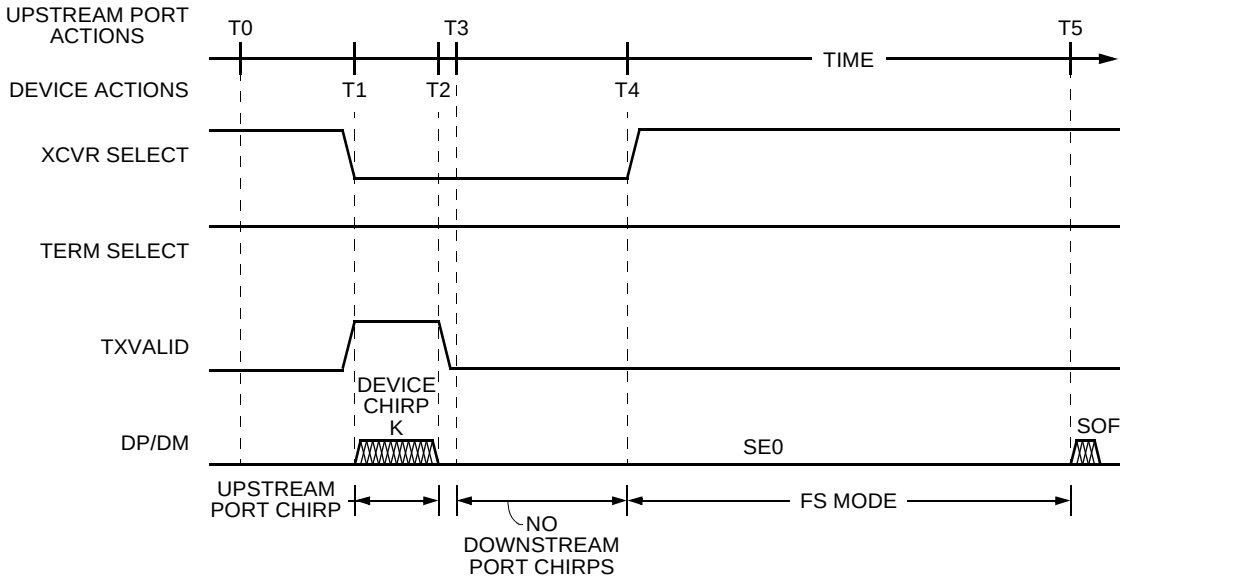

Figure 17. HS Detection Handshake Timing Behavior (FS Mode)

Table 15. HS Detection Handshake Timing Values (FS Mode)

Timing Parameter	Description	Value
T0*	HS handshake begins. D+ pull-up enabled, HS terminations disabled.	0 (reference)
T1†	Device enables HS transceiver and asserts chirp K on the bus.	T0 < T1 < HS reset T0 + 6.0 ms
T2	Device removes chirp K from the bus (1 ms minimum width).	T1 + 1.0 ms {TUCH} < T2 < HS reset T0 + 7.0 ms {TUCHEND}
T3	Earliest time when downstream port may assert chirp K on the bus.	T2 < T3 < T2+100 µs {TWTDCH}
T4	Downstream port chirp not detected by the device. Device reverts to FS default state and waits for end of reset.	T2 + 1.0 ms < T4 {TWTFS} < T2 + 2.5 ms
T5	Earliest time at which downstream port may end reset.	HS reset T0 + 10 ms {TDRST (Min)}

* T0 may occur to 4 ms after HS reset T0.
† The SIE must assert the chirp K for 66000 CLKOUT cycles to ensure a 1 ms minimum duration.

Other Functions (continued)

HS Downstream Facing Port

The following is an example of the USS2X1 behavior when the downstream facing port that it is attached to supports HS operation (a USB2.0 host/hub).

Upon entering the HS detection process (T0), XcvrSelect and TermSelect are in FS mode. The D+ pull-up is asserted and the HS terminations are disabled. The SIE then sets OpMode to disable bit stuffing and NRZI encoding, and begins the transmission of all 0s data, which asserts a HS K (chirp) on the bus (T1).The device chirp must last at least 1.0 ms, and must end no later than 7.0 ms after HS reset T0. At time T1, the SIE sets XcvrSelect to HS mode and begins listening for a chirp sequence from the downstream port.

If the downstream port is HS capable, then it will begin generating an alternating sequence of chirp Ks and chirp Js (T3) after the termination of the chirp from the device (T2). After the device sees the valid downstream port chirp sequence chirp K-J-K-J-K-J (T6), it will enter HS mode by setting TermSelect to HS mode (T7). Figure 18 provides a state diagram for chirp K-J-K-J-K-J validation. Prior to the end of reset (T9), the upstream port must terminate the sequence of chirp Ks and chirp Js (T8) and assert SE0 (T8—T9). Note that the sequence of chirp Ks and chirp Js constitutes bus activity.

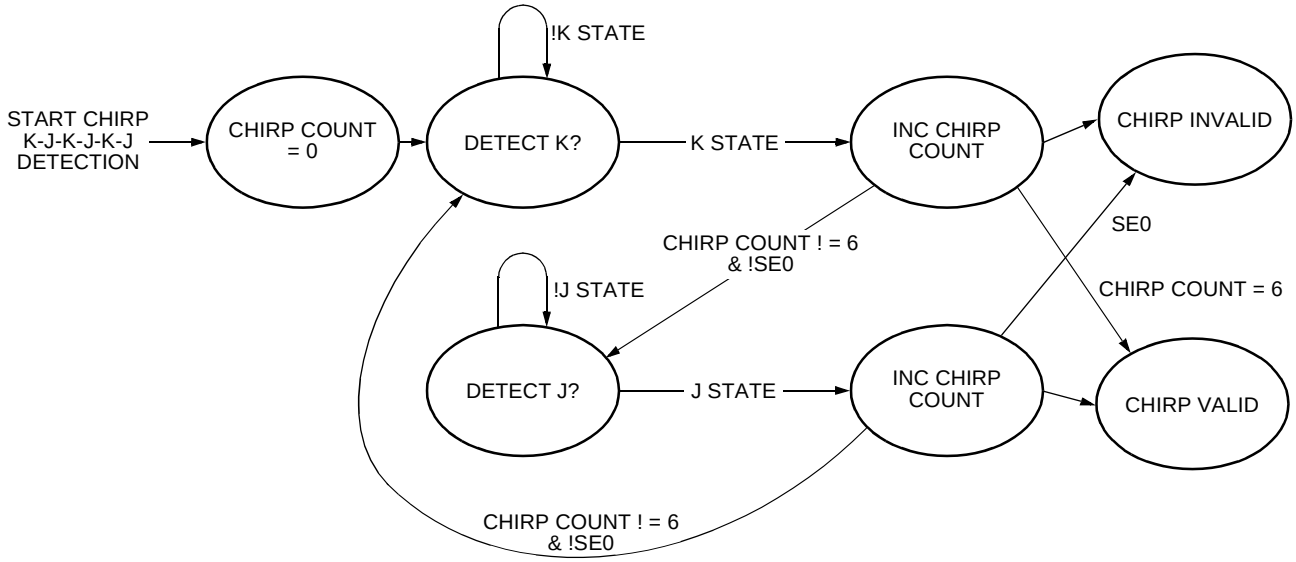

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Figure 18. Chirp K-J-K-J-K-J Sequence Detection State Diagram

The SIE must use LineState signal transitions to step through the chirp K-J-K-J-K-J state diagram, where K state is equivalent to LineState = K state and J state is equivalent to LineState = J state. The SIE must employ a counter (chirp count) to count the number of chirp K and chirp J states. Note that LineState does not filter the bus signals, so the requirement that a bus state must be continuously asserted for 2.5 μs, must be verified by the SIE sampling the LineState signals.

Other Functions (continued)

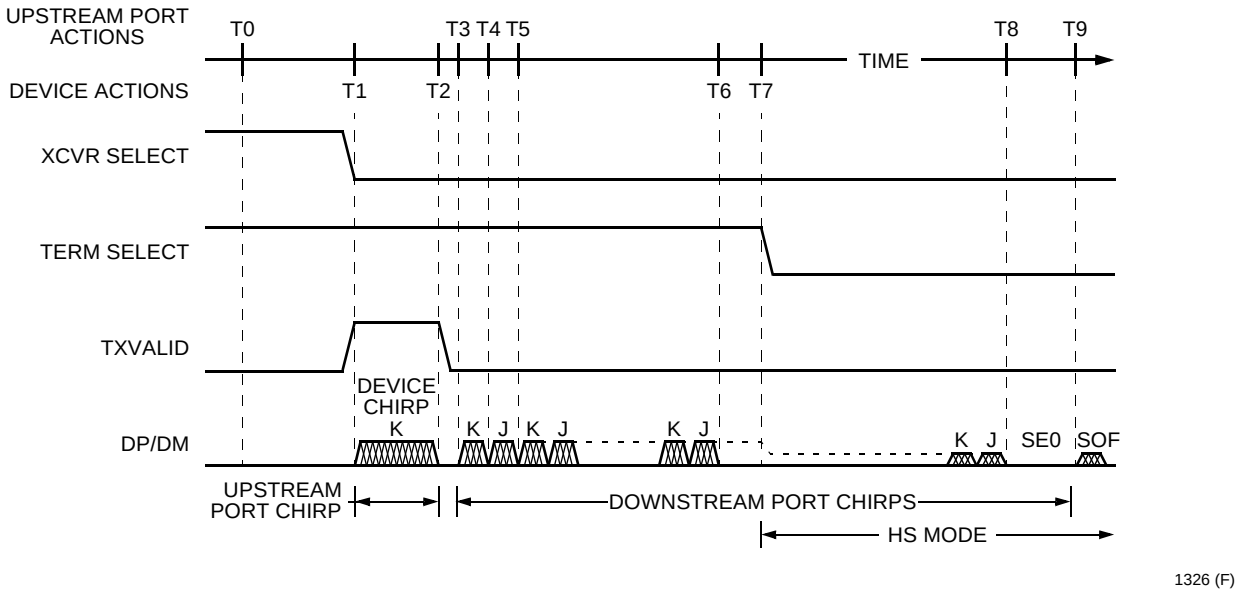

Figure 19. HS Detection Handshake Timing Behavior (HS Mode)

Table 16. Reset Timing Values

Timing Parameter	Description	Value
T0*	HS handshake begins. D+ pull-up enabled, HS terminations disabled.	0 (reference)
T1†	Device asserts chirp K on the bus.	T0 < T1 < HS reset T0 + 6.0 ms {T_{UCHEND} – T_{UCH}}
T2	Device removes chirp K from the bus (1 ms minimum width).	T0 + 1.0 ms {T_{UCH}} < T2 < HS reset T0 + 7.0 ms {T_{UCHEND}}
T3‡	Downstream port asserts chirp K on the bus.	T2 < T3 < T2 + 100 µs {T_{WTDCH}}
T4	Downstream port toggles chirp K to chirp J on the bus.	T3 + 40 µs {T_{DCHBIT} (min)} < T4 < T3 + 60 µs {T_{DCHBIT} (max)}
T5	Downstream port toggles chirp J to chirp K on the bus.	T4 + 40 µs {T_{DCHBIT} (min)} < T5 < T4 + 60 µs {T_{DCHBIT} (max)}
T6	Device detects downstream port chirp.	T6
T7	Downstream port chirp detected by the device. Device removes D+ pull-up and asserts HS terminations, reverts to HS default state and waits for end of reset.	T6 < T7 < T6 + 500 µs {T_{WTHS}}
T8	Terminate downstream port chirp K-J sequence (repeating T4 and T5).	T9 – 500 µs {T_{DCHSE0} (max)} < T8 < T9 – 100 µs {T_{DCHSE0} (min)}
T9	The earliest time at which a downstream port may end reset. The latest time at which the device may remove the D+ pull-up and assert the HS terminations, reverts to HS default state.	HS reset T0 + 10 ms {T_{DRST} (min)}

* T0 may be up to 4 ms after HS reset T0.
† Due to the assertion of the HS termination on the downstream port and FS termination on the upstream port, between T1 and T7 the signaling levels on the bus are higher than HS signaling levels and are less than FS signaling levels.
‡ The SIE must use LineState to detect the downstream port chirp sequence.

Other Functions (continued)

Suspend Timing

If reset is entered from a suspended state, the internal oscillator and clocks of the transceiver have already been powered down. Figure 20 shows how CLKOUT is used to control the duration of the chirp generated by the device.

When reset is entered from a suspended state (J to SE0 transition reported by LineState), SuspendN is combinatorially negated at time T0 by the SIE. The USS2X1 oscillator and PLL take several milliseconds to stabilize. The USS2X1 will not generate any transitions of the CLKOUT signal until it is usable, where usable is defined as stable to within ±10% of the nominal frequency and the duty cycle accuracy 50 ± 5%. After CLKOUT is usable, the SIE must initialize a timer (T1) and look for SE0 to be asserted for at least 2.5 µs. If the test is true (T1 ≥ Tfiltse0), then start the reset handshake protocol.

If the test is false, the latest time that could successfully start the chirp sequence was exceeded and the SIE never saw SE0 for at least 2.5 µs (T0 ≥ Tuchend – Tuch & T1 < Tfiltse0), then return to the suspend state (assert SuspendN).

The first transition of CLKOUT occurs at T1. The SIE must assert a chirp K for 66000 CLKOUT cycles to ensure a 1 ms minimum duration. If CLKOUT is 10% fast (66 MHz), then chirp K will be 1.0 ms. If CLKOUT is 10% slow (54 MHz), then chirp K will be 1.2 ms. The 5.8 ms requirement for the first CLKOUT transition after SuspendN ensures enough time to assert a 1 ms chirp K and still complete before T3. Once the chirp K is completed (T3), the SIE can begin looking for downstream chirps and use CLKOUT to time the process.

To detect the assertion of the downstream chirp Ks and chirp Js for 2.5 µs {TFILT}, the SIE must see the appropriate LineState signals asserted continuously for 165 CLKOUT cycles.

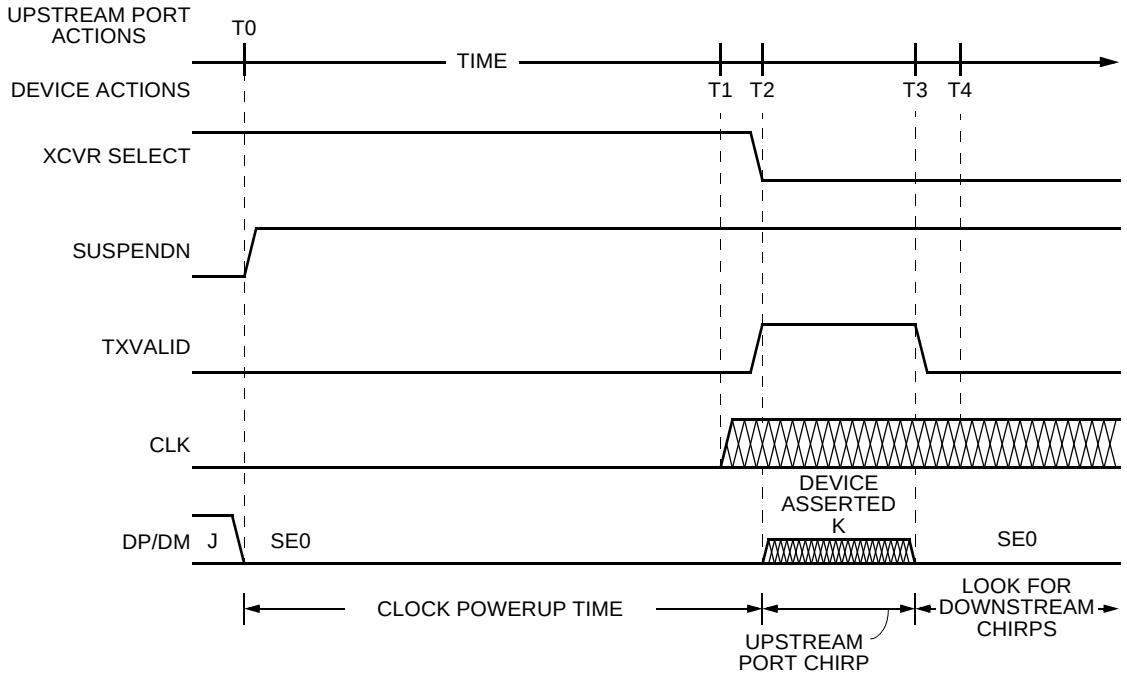

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Figure 20. HS Detection Handshake Timing Behavior from Suspend

Other Functions (continued)

Table 17. HS Detection Handshake Timing Values from Suspend

Timing Parameter	Description	Value
T0	While in suspend state an SE0 is detected on the USB. HS handshake begins. D+ pull-up enabled, HS terminations disabled, SuspendN negated.	0 (HS reset T0)
T1	First transition of CLKOUT. CLKOUT usable (frequency accurate to ±10%, duty cycle accurate to 50 ± 5%).	T0 < T1 < T0 + 5.6 ms
T2	Device asserts chirp K on the bus.	T1 < T2 < T0 + 5.8 ms
T3	Device removes chirp K from the bus (1 ms minimum width) and begins looking for downstream chirps.	T2 + 1.0 ms {TUCH} < T3 < T0 + 7.0 ms {TUCHEND}
T4	CLKOUT nominal (CLKOUT is frequency accurate to ±500 ppm, duty cycle accurate to 50 ± 1%).	T1 < T3 < T0 + 20.0 ms TDRST (Min) + TRSMRCY}

Assertion of Resume

In this case, an event internal to the device initiates the resume process. A device with remote wake-up capability must wait for at least 5 ms after the bus is in the idle state before sending the remote wake-up resume signaling. This allows the hubs to get into their suspend state and prepare for propagating resume signaling.

The device has 10 ms where it can draw a nonsuspend current before it must drive resume signaling. At the beginning of this period, the SIE may negate SuspendN, allowing the transceiver, oscillator, and PLL to power up and stabilize.

Figure 21 illustrates the behavior of a device returning to HS mode after being suspended. At T4, a device that was previously in FS mode would maintain TermSelect and XcvrSelect high.

To generate resume signaling (FS K), the USS2X1 is placed in the disable bit stuffing and NRZI encoding operational mode, TermSelect and XcvrSelect must be in FS mode, TXValid asserted, and all 0s data is presented on the DATA input bus for at least 1 ms (T1—T2).

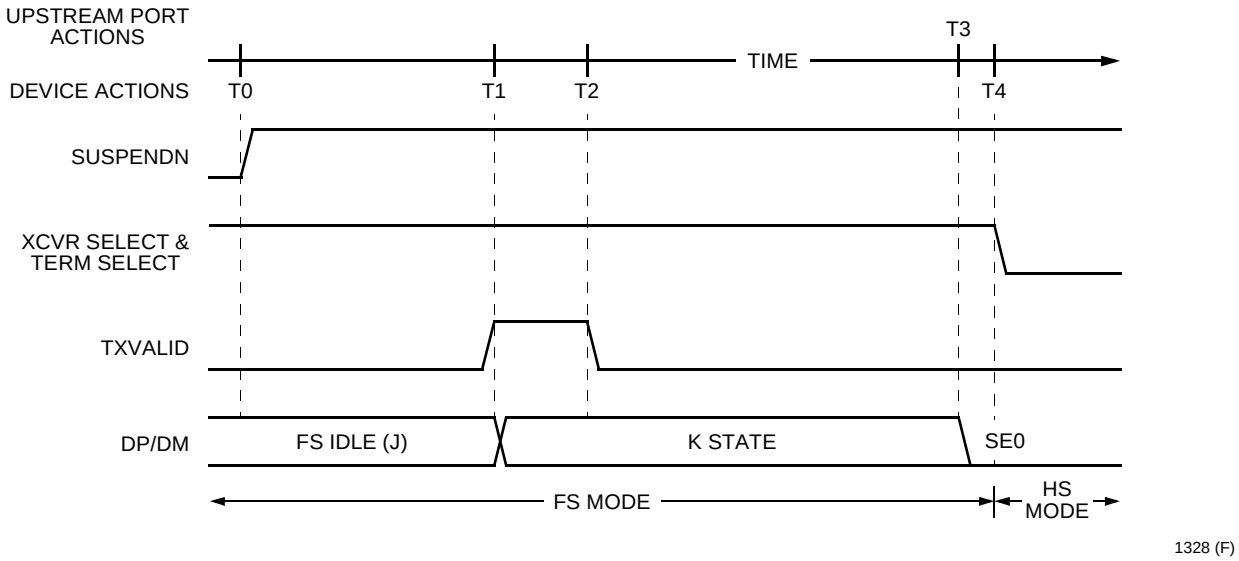


Figure 21. Resume Timing Behavior (HS Mode)

Other Functions (continued)

Table 18. Suspend Timing Values (HS Mode)

Timing Parameter	Description	Value
T0	Internal device event initiating the resume process.	0 (reference)
T1	Device asserts FS K on the bus to signal resume request to downstream port.	T0 < T1 < T0 + 10 ms {T_{DRSMDN}}
T2	The device releases FS K on the bus; however, by this time the K state is held by downstream port.	T1 + 1.0 ms {T_{DRSMUP} (min)} < T2 < T1 + 15 ms {T_{DRSMUP} (max)}
T3	Downstream port asserts SE0.	T1 + 20 ms {T_{DRSMDN}}
T4	Latest time at which a device, which was previously in HS mode, must restore HS mode after bus activity stops.	T3 + 1.33 µs {two low-speed bit times}

Detection of Resume

Resume signaling always takes place in FS mode (TermSelect and XcvrSelect = FS enabled), so the behavior for an HS device is identical to that of an FS device. The SIE uses the LineState signals to determine when the USB transitions from the J to the K state and finally to the terminating low-speed EOP (SE0 for 1.25 µs—1.5 µs).

The resume signaling (FS K) will be asserted for at least 20 ms. At the beginning of this period, the SIE may negate SuspendN, allowing the transceiver, oscillator and PLL to powerup and stabilize.

The low-speed EOP condition is relatively short. SIEs that simply look for an SE0 condition to exit suspend mode do not necessarily give the USS2X1's clock generator enough time to stabilize. It is recommended that all SIE implementations key off the J-to-K transition for exiting suspend mode (SuspendN = 1). And within 1.25 µs after the transition to the SE0 state (low-speed EOP), the SIE must enable normal operation, i.e., enter HS or FS mode depending on the mode the device was in when it was suspended.

If the device was in FS mode, then the SIE leaves the FS terminations enabled. After the SE0 expires, the downstream port will assert a J state for one low-speed bit time, and the bus will enter an FS idle state (maintained by the FS terminations).

If the device was in HS mode, then the SIE must switch to the FS terminations before the SE0 expires (<1.25 µs).

After the SE0 expires, the bus will then enter an HS idle state (maintained by the HS terminations).

Note: Glitches that occur on the USB during suspend are handled as follows. When a device is suspended, a J state is on the bus and the SIE should be looking for a K (resume) or an SE0 (reset). In either case, a glitch that looks like a K or an SE0 will cause the USS2X1 ocillator to start up. The USS2X1 will hold off any CLKOUT transitions until CLKOUT is usable. Once CLKOUT is running (several milliseconds later), the SIE must check LineState. If a J state is asserted, then the SIE returns to the suspend state; if a K state is asserted, then the SIE starts the resume process; and if SE0 is asserted, then the SIE starts the reset process.

HS Device Attach

Figure 22 demonstrates the timing of the USS2X1 control signals during a device attach event. When an HS device is attached to an upstream port, power is asserted to the device and the device sets XcvrSelect and TermSelect to FS mode (time T1).

V_{BUS} is the 5 V power available on the USB. Device reset in Figure 22 indicates that V_{BUS} is within normal operational range as defined in the USB 2.0 specification. The assertion of device reset (T0) will initialize the device and cause the SIE state machine to set the XcvrSelect and TermSelect signals to FS mode (T1). Note that device reset is not the same as the USS2X1 reset signal. Device reset is an input to the SIE, which in turn can use it to assert reset to the USS2X1.

Other Functions (continued)

The standard FS technique of using a pull up on DP to signal the attach of an FS device is employed. The SIE must then check the LineState signals for SE0. If LineState = SE0 is asserted at time T2, then the upstream port is forcing the reset state to the device (i.e., driven SE0). The device will then reset itself before initiating the HS detection handshake protocol.

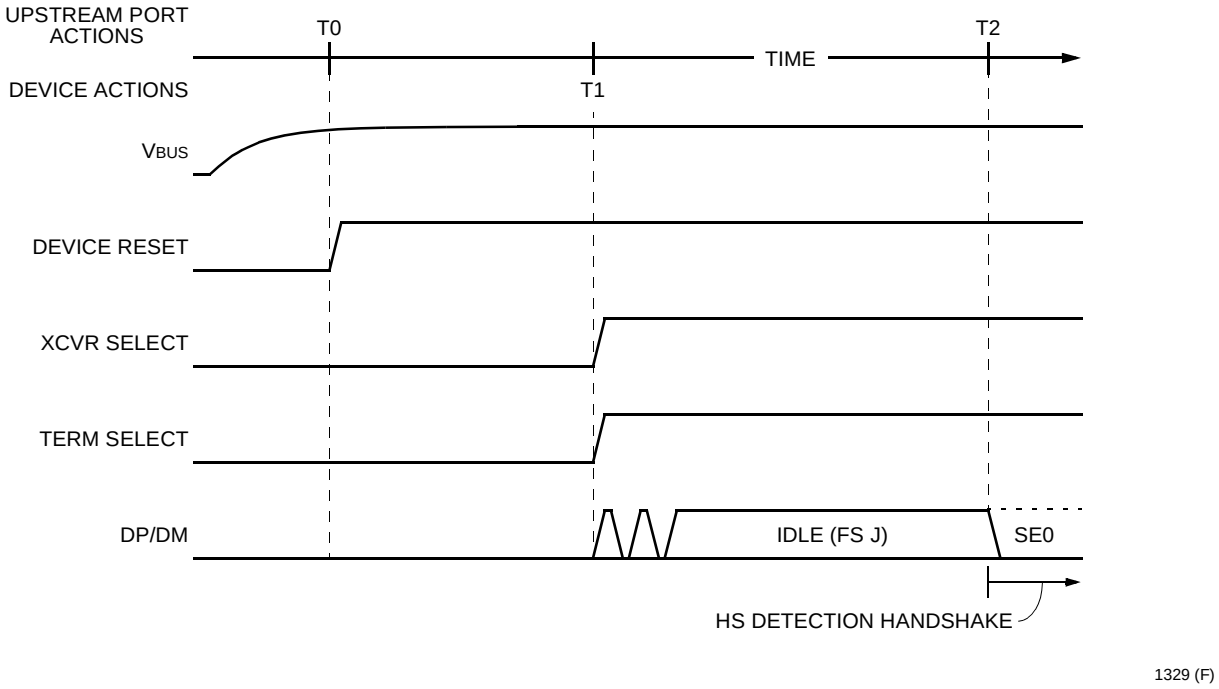


Figure 22. Device Attach Behavior

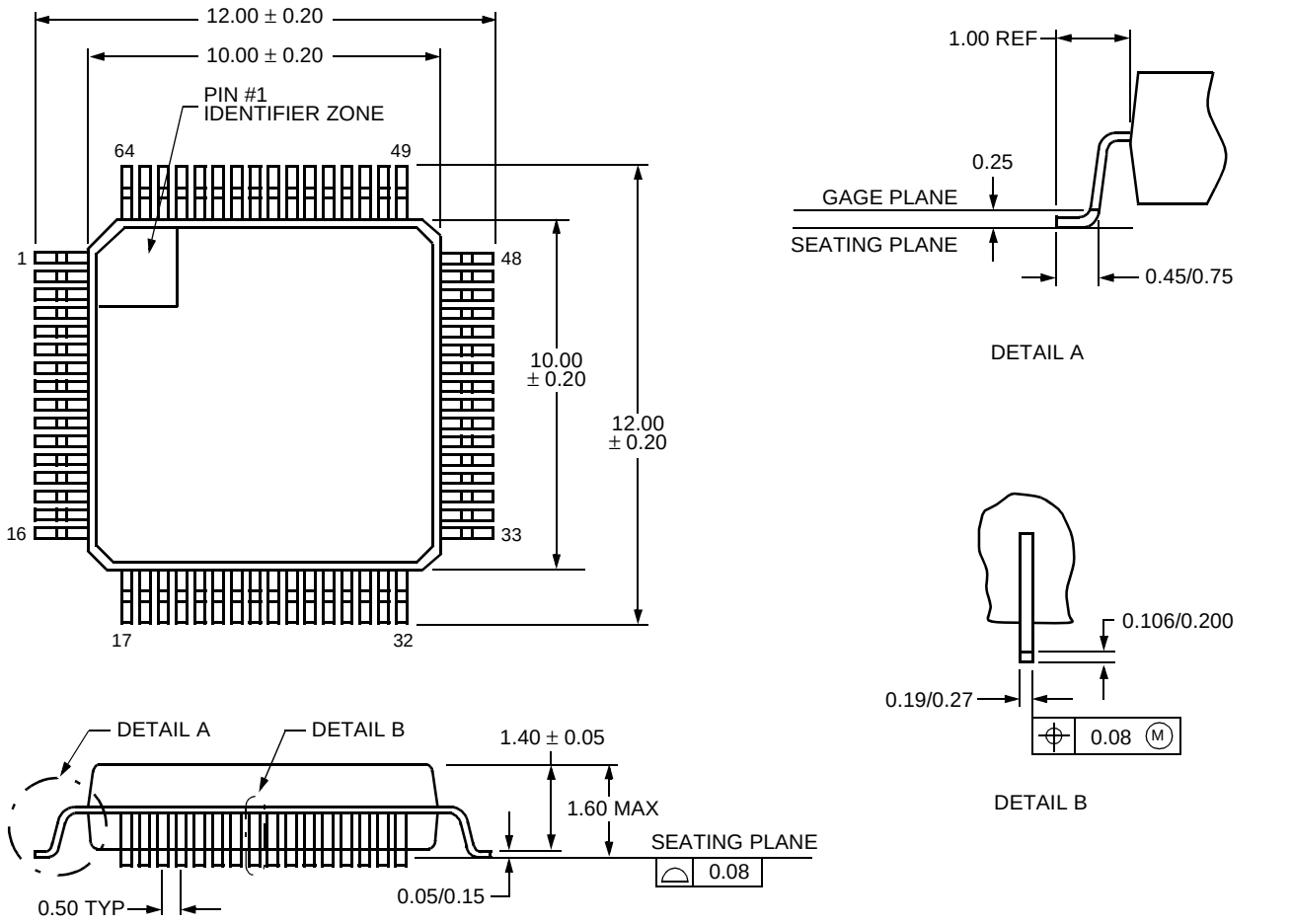
Table 19. Attach and Reset Timing Values

Timing Parameter	Description	Value
T0	V_{bus} valid.	0 (reference)
T1	Maximum time from V_{bus} valid to when the device must signal attach.	T0 + 100 ms {T_{SIGATT}} < T1
T2 (HS Reset T0)	Debounce interval. The device now enters the HS detection handshake protocol.	T1 + 100 ms {T_{ATTDB}} < T2

Outline Diagrams

64-Pin TQFP

Dimensions are in millimeters.

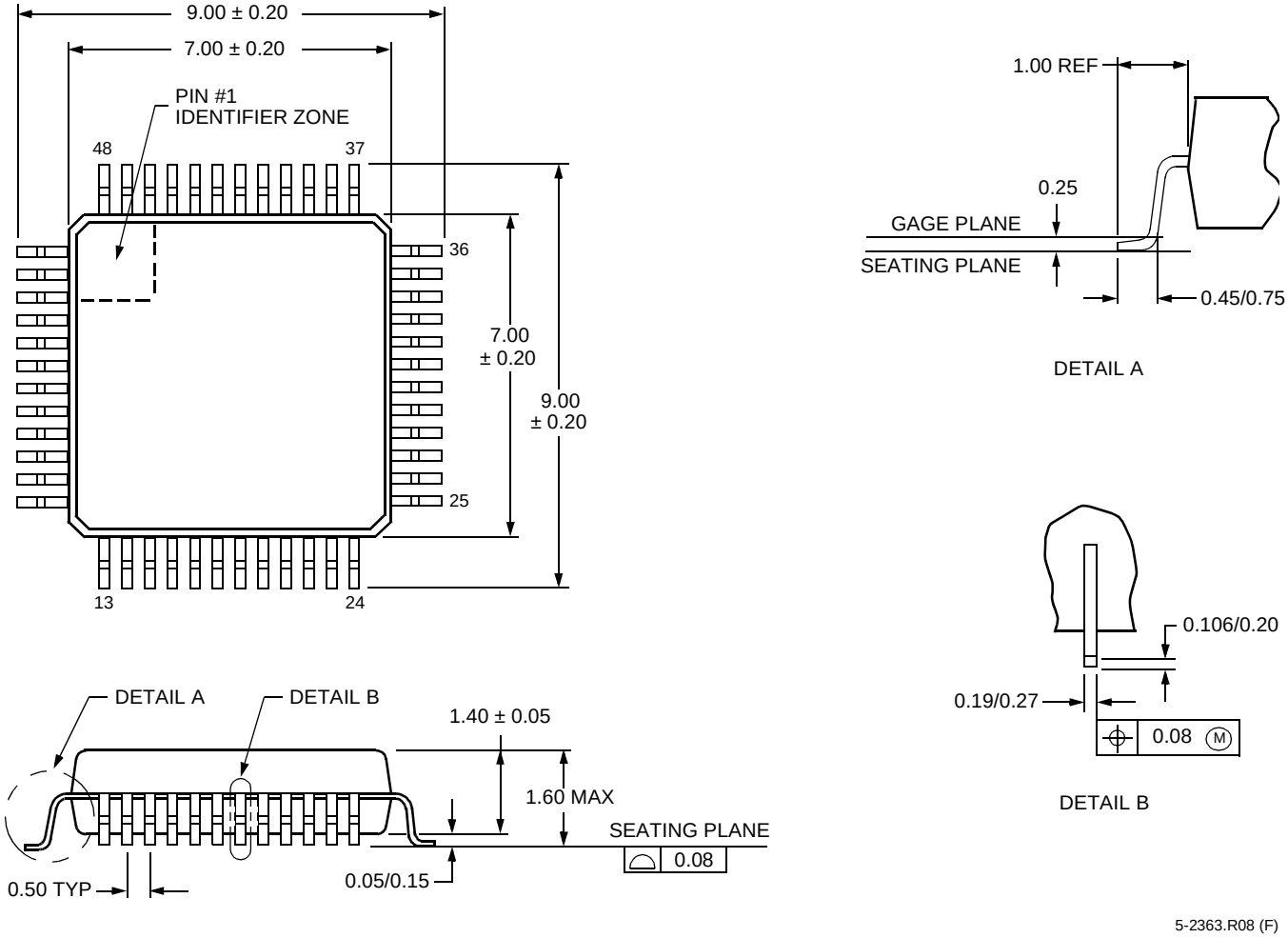


5-3080.R07 (F)

Outline Diagrams (continued)

48-Pin TQFP

Dimensions are in millimeters.



5-2363.R08 (F)

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