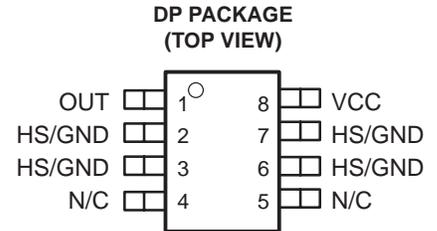


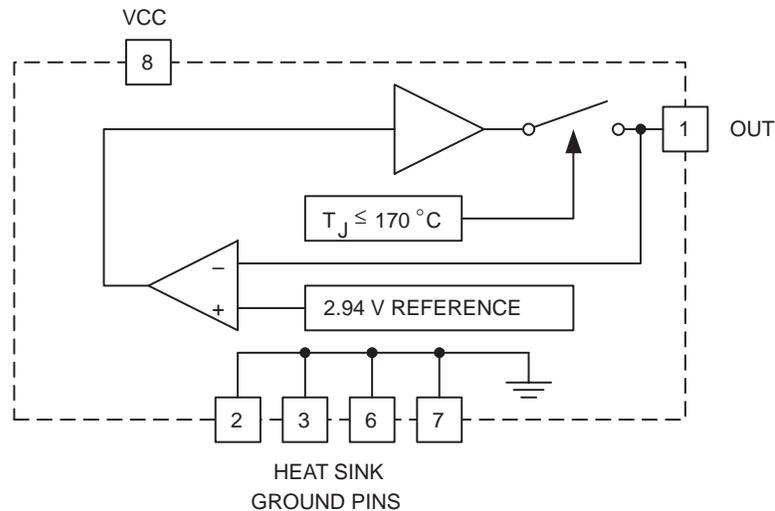
- Complies With VME64 Standard
- 2.94-V Regulated Output Voltage With 1% Tolerance at 25°C
- Provides Bias for up to 32 Lines of Active Termination for VME busses
- -575-mA Sourcing Current for Termination
- +475-mA Sinking Current for Active Negation Drivers
- Current Limit and Thermal Shutdown Protection
- Low Thermal Resistance Surface-Mount Packages



### description

The VME bus bias generator provides current for up to 32 lines of active termination for a VME64 parallel bus. The VME standards require termination at both ends of the bus. The voltage regulator and internal logic circuits of these parts provide all the functionality and performance necessary to bias termination resistors for the VME bus. The VME bus bias generator sink current maintains regulation with all active negation drivers negated. Internal circuit trimming is used to trim the output voltage to a 1% tolerance. The UC563 regulator source/sink will provide better VME bus performance and work with active negation drivers. The regulator with resistor provides the bus with higher pullup current than passive termination. Other features include thermal shutdown and current limit for short circuit conditions. This device is available in low thermal resistance versions of the industry standard 8-pin power SOIC.

### block diagram



UDG-99094

NOTE: Indicated pinout is for the 8-pin power SOIC package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2000, Texas Instruments Incorporated

# UC563

## 32-LINE VME BUS BIAS GENERATOR

SLUS169A - APRIL 1999 - REVISED NOVEMBER 2000

### absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

VCC	7 V
Regulator output current	600 mA
Storage temperature, $T_{stg}$	-65°C to 150°C
Junction temperature, $T_J$	-55°C to 150°C
Lead temperature (soldering, 10 Sec.)	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Interface Products Data Book (TI Literature Number SLUD002) for thermal limitations and considerations of packages. All voltages are referenced to ground.

### recommended operating conditions

VCC voltage	4.75 V to 5.25 V
-------------	------------------

### ORDERING INFORMATION

$T_J$	PACKAGED DEVICES
	SOIC (DP)
0°C to 70°C	UC563DP

† The DP package is available tape and reeled. Add TR suffix to each device type to order quantities of 2500 per reel.

### electrical characteristics, $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$ , $V_{CC} = 5\text{ V}$ , $C_{OUT} = 4.7\text{ F}$ , $T_A = T_J$ , (unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>Supply Current Section</b>					
Supply current	No load		35	60	mA
	$I_{OUT} = -575\text{ mA}$		610	635	mA
<b>Regulator Section</b>					
Output voltage	25°C, No load	2.91	2.94	2.97	V
Load regulation	$-575\text{ mA} \leq I_{OUT} \leq 475\text{ mA}$ , See Note 1		25	30	mV
Line regulation	$4.875\text{ V} \leq V_{CC} \leq 5.25\text{ V}$ , No load		10	20	mV
Short circuit current	$V_{OUT} = 0\text{ V}$		-1200	-600	mA
	$V_{OUT} = 3.5\text{ V}$	500	1200		mA
Thermal shutdown	See Note 2		170		°C
Thermal shutdown hysteresis	See Note 2		10		°C

NOTES: 1. Tested at a constant junction temperature by low duty cycle pulse testing.  
2. Ensured by design. Not production tested.

### pin assignments

**GND:** Ground pin.

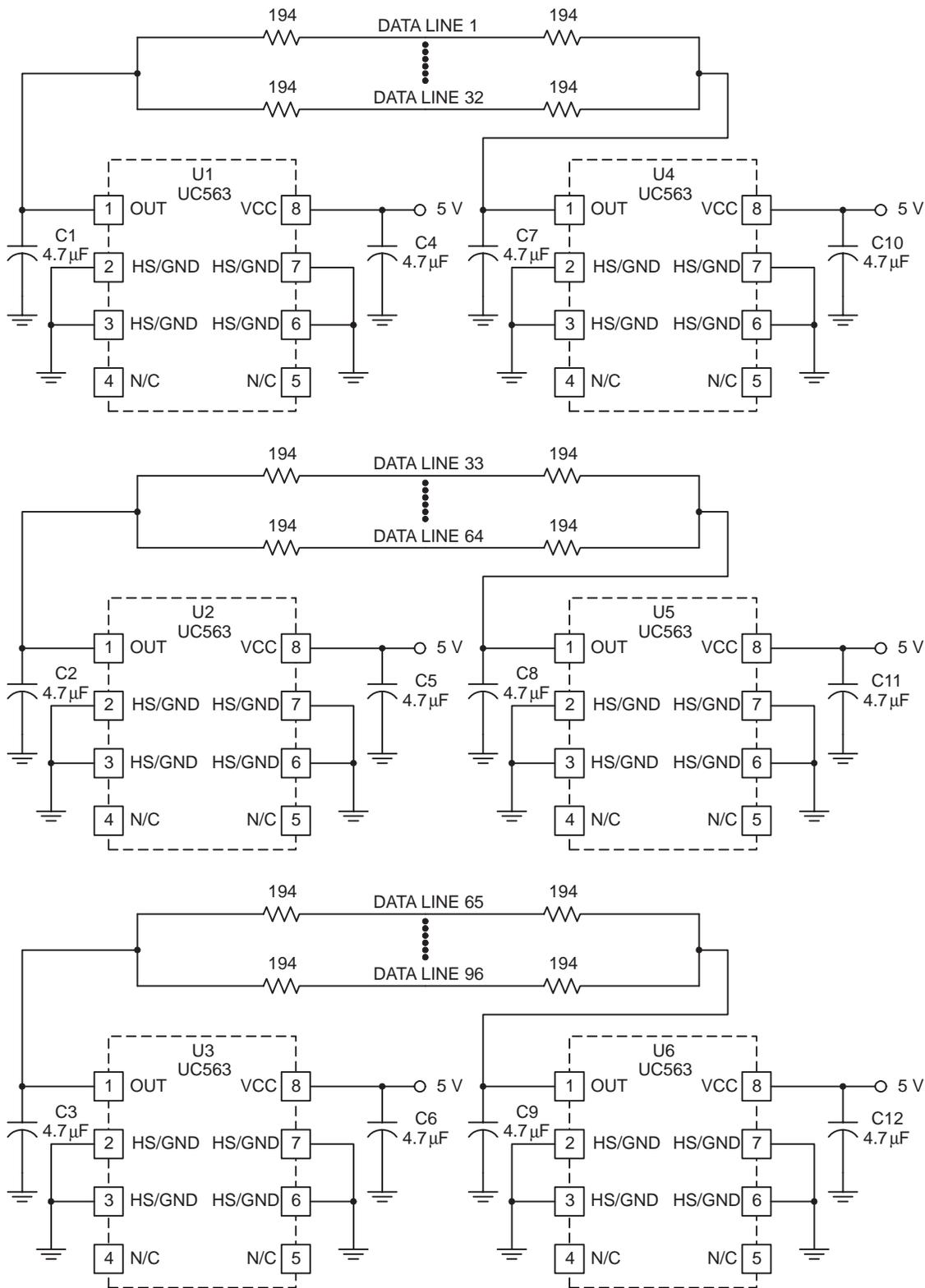
**HS/GND:** Heat sink GND. Connect to large area PC board traces to increase power dissipation capability.

**OUT:** 2.94-V regulated output voltage pin. The part is internally current limited for both sinking and sourcing current to prevent damage. For best performance, a 4.7- $\mu\text{F}$  low ESR capacitor is recommended.

**VCC:** Supply voltage pin. The pin should be decoupled with at least a 2.2- $\mu\text{F}$  low ESR capacitor. For best performance, a 4.7- $\mu\text{F}$  low ESR capacitor is recommended. Lead lengths should be kept at a minimum.



## typical application



UDG-00133

## **IMPORTANT NOTICE**

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.