NEC

MOS INTEGRATED CIRCUIT

μPD78P0208

8-BIT SINGLE-CHIP MICROCOMPUTER

The μPD78P0208 is a product in the μPD780208 subseries within the 78K/0 series, in which on-chip mask ROM of the μPD780208 is replaced with one-time PROM or EPROM.

Since user programs can be written to PROM, this microcomputer is best suited for evaluation in system development, manufacture of small quantities of multiple products, and fast start-up of applications.

For specific functions and other detailed information, consult the following user's manual.

This manual is required reading for design work.

μPD780208 Subseries User's Manual : IEU-1413

78K/0 Series User's Manual, Instruction : IEU-1372

FEATURES

- Pin compatible with mask ROM products (except for V_{PP} pin)
- Internal PROM: 60K bytes**Note 1**
  - μPD78P0208KL-T : EPROM (best suited for system evaluation)
  - μPD78P0208GF : PROM (best suited for manufacture of small quantities)
- Internal high-speed RAM : 1024 bytes
- Internal expansion RAM : 1024 bytes**Note 2**
- Buffer RAM : 64 bytes
- FIP® display RAM : 80 bytes
- Can be operated at the same power supply voltage as mask ROM products:
  V_{DD} = 2.7 to 5.5 V (except for A/D converter).
  A/D converter's power supply voltage: AV_{DD} = 4.0 to 5.5 V.
- QTOP™ microcomputer

Notes 1. Internal PROM capacity can be changed according to the internal memory switching register (IMS).

2. Internal expansion RAM capacity can be changed according to the internal expansion RAM switching register (IXS).

Remark The QTOP microcomputer is a single-chip microcomputer with a built-in one-time PROM that is totally supported by NEC. The support includes writing application programs, marking, screening, and verification.

This product differs from mask ROM products in the following respects.

- It can use the same memory mapping as mask ROM products, depending upon the IMS and IXS settings.
- FIP0 to FIP12 have on-chip pull-down resistors.
- Port 3 and FIP13 to FIP52 (port 8 to port 12) do not have on-chip pull-down resistors.
- Port 7 does not have a on-chip pull-up resistor.

In this reference, all ROM components that are common to one-time PROM and EPROM are referred to as PROM.

The information in this document is subject to change without notice.

Document No. U11295EJ1V0DS00 (1st edition)
(Previous No. IP-3475)
Date Published May 1996 P
Printed in Japan

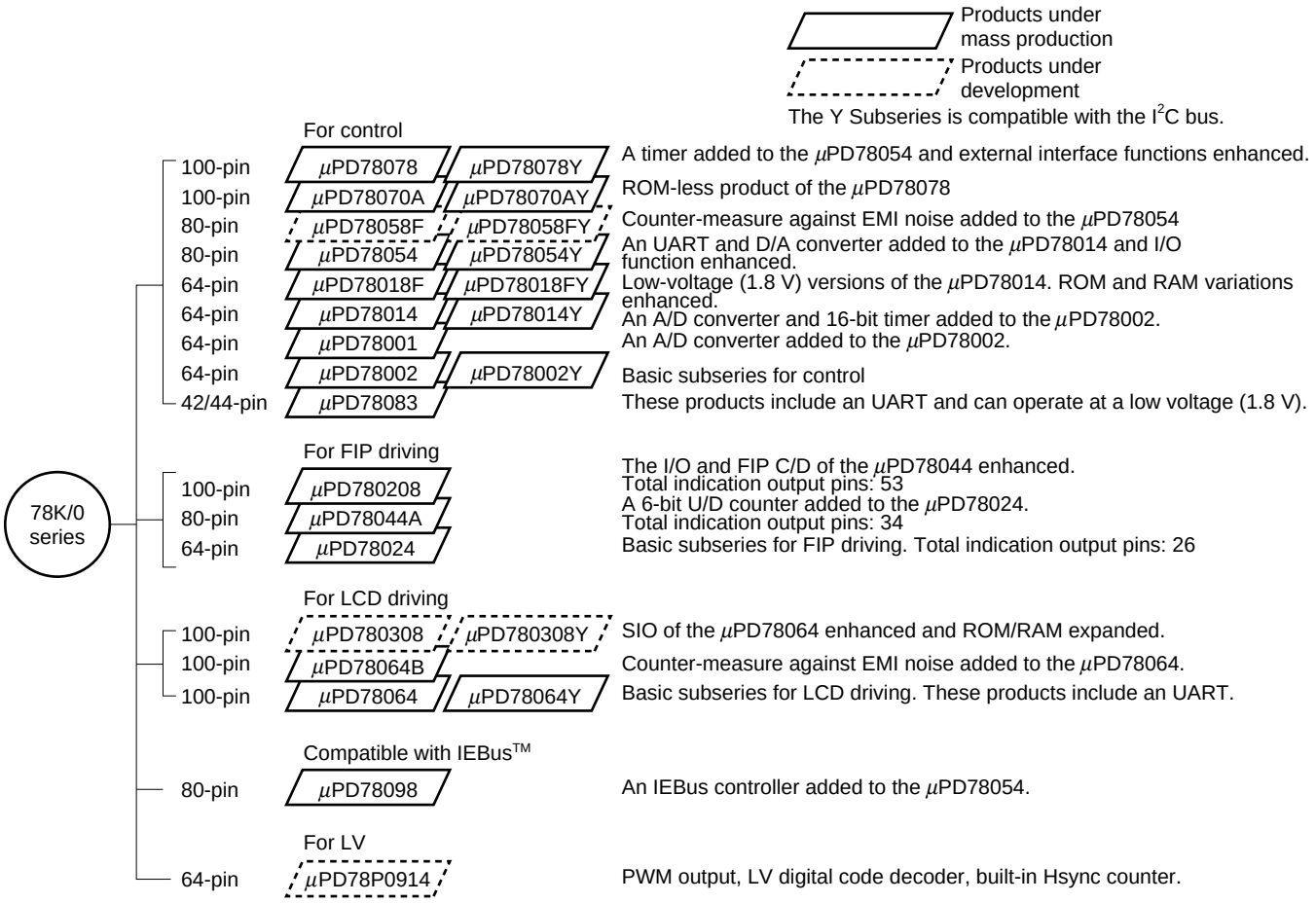
The mark ★ shows major revised points.

ORDERING INFORMATION

Part No.	Package		Internal ROM
μPD78P0208GF-3BA	100-pin plastic QFP	(14 × 20 mm)	One-Time PROM
μPD78P0208KL-T	100-pin ceramic WQFN	(14 × 20 mm)	EPROM

★ 78K/0 SERIES PRODUCT DEVELOPMENT

The 78K/0 series products were developed as shown below. The subseries names are indicated in frames.



The table below shows the main differences between subseries.

Subseries name \ Function		ROM capacity	Timer				8-bit A/D	8-bit D/A	Serial interface	I/O	V_{DD} Min. value	External expansion
			8-bit	16-bit	Watch	WDT						
For control	μPD78078	32K-60K	4ch	1ch	1ch	1ch	8ch	2ch	3ch (UART : 1ch)	88 pins	1.8 V	○
	μPD78070A	–								61 pins	2.7 V	
	μPD78058F	48K-60K	2ch							69 pins		
	μPD78054	16K-60K									2.0 V	
	μPD78018F	8K-60K						–	2ch	53 pins	1.8 V	
	μPD78014	8K-32K									2.7 V	
	μPD780001	8K		–	–				1 ch	39 pins		–
	μPD78002	8K-16K			1 ch		–			53 pins		○
	μPD78083				–		8 ch		1 ch (UART : 1 ch)	33 pins	1.8 V	–
For FIP driving	μPD780208	32K-60K	2 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	74 pins	2.7 V	–
	μPD78044A	16K-40K								68 pins		
	μPD78024	24K-32K								54 pins		
For LCD driving	μPD780308	48K-60K	2 ch	1 ch	1 ch	1 ch	8 ch	–	3 ch (UART : 1 ch)	57 pins	1.8 V	–
	μPD78064B	32K							2 ch (UART : 1 ch)		2.0 V	
	μPD78064	16K-32K										
Compatible with IEBus	μPD78098	32K-60K	2 ch	1 ch	1 ch	1 ch	8 ch	2 ch	3 ch (UART : 1 ch)	69 pins	2.7 V	○
For LV	μPD78P0914	32K	6 ch	–	–	1 ch	8 ch	–	2 ch	54 pins	4.5 V	○

OVERVIEW OF FUNCTIONS

Item		Function
Internal memory		• PROM: 60K bytes Note 1 • RAM Internal high-speed RAM : 1024 bytes Internal expansion RAM : 1024 bytes Note 2 Buffer RAM : 64 bytes FIP display RAM : 80 bytes
General register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Instruction cycle		On-chip instruction execution time cycle modification function
	Main system clock selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (5.0 MHz operation)
	Subsystem clock selected	122 μs (32.768 kHz operation)
Instruction set		• Multiplier/divider (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit handling (set, reset, test, Boolean operations)
I/O ports (including pins also used for FIP)		Total : 74 pins • CMOS input : 2 • CMOS I/O : 27 • N-ch open-drain I/O : 5 • P-ch open-drain I/O : 24 • P-ch open-drain output : 16
FIP controller/driver		Display output total : 53 • No. of segments : 9 to 40 • No. of digits : 2 to 16
A/D converter		• 8-bit resolution × 8 channels • Supply voltage: AV_{DD} = 4.0 to 5.5 V
Serial interface		• 3-wire serial I/O/SBI/2-wire serial I/O selectable modes: 1 channel • 3-wire serial I/O mode (on-chip maximum 64-byte automatic transmit/receive function): 1 channel
Timers		• 16-bit timer/event counter : 1 channel • 8-bit timer/event counters : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel
Timer outputs		3 (1 with 14 bit PWM output capability)
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz (5.0 MHz main system clock operation) 32.768 kHz (32.768 kHz subsystem clock operation)
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz (5.0 MHz main system clock operation)

Notes 1. The capacity of internal PROM can be changed according to the internal memory switching register (IMS) settings.

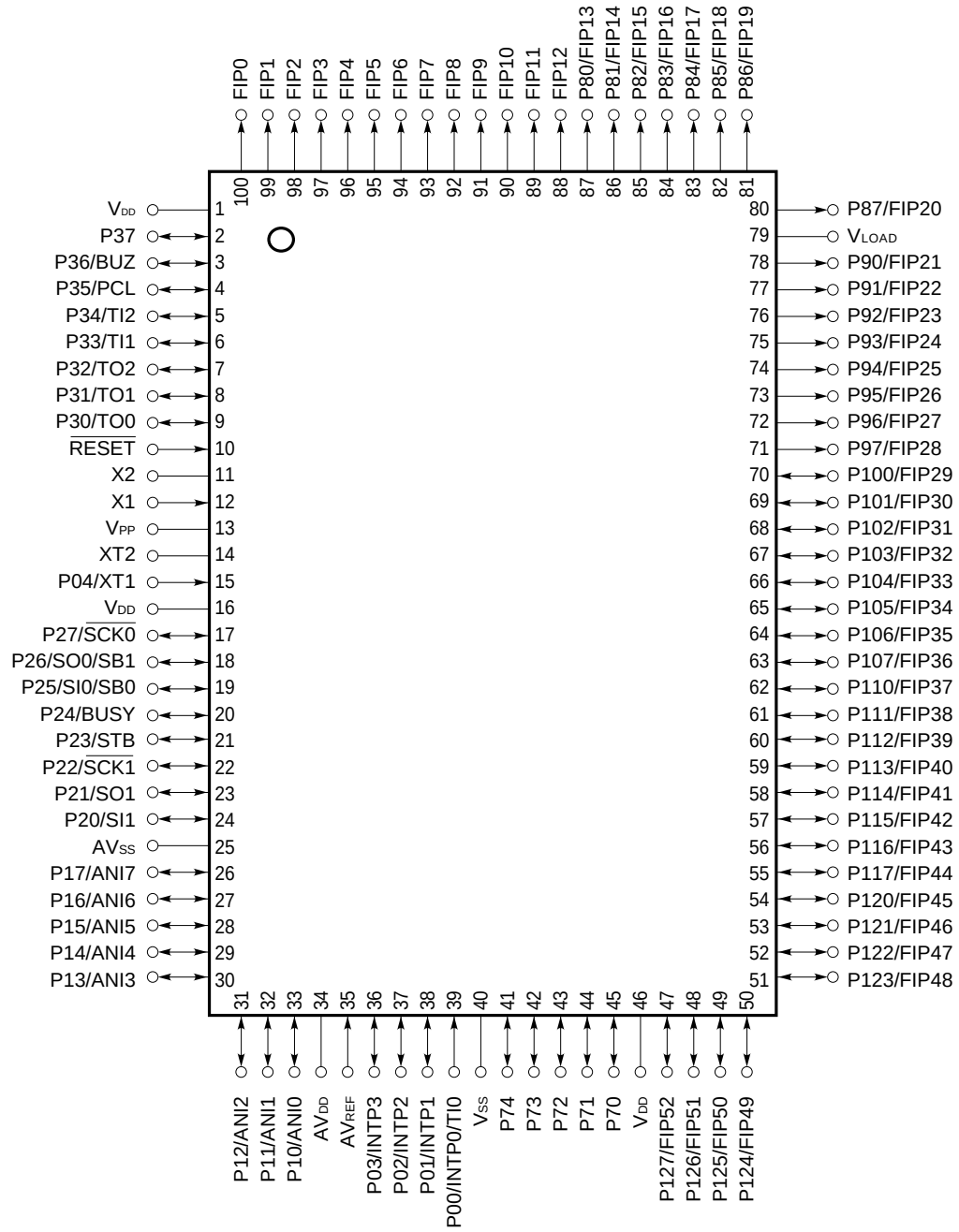
2. The capacity of internal expanded RAM can be changed according to the internal expanded RAM switching register (IXS) settings.

Item		Function
Vector interrupts	Maskable interrupt	Internal: 9, external: 4
	Non-maskable interrupt	Internal: 1
	Software interrupt	Internal: 1
Test input		Internal: 1
Supply voltage		V_{DD} = 2.7 to 5.5 V
Package		• 100-pin plastic QFP (14 × 20 mm) • 100-pin ceramic WQFN (14 × 20 mm)

PIN CONFIGURATION (TOP VIEW)

(1) Normal operating mode

- 100-pin plastic QFP (14 × 20 mm)
  μPD78P0208GF-3BA
- 100-pin ceramic WQFN (14 × 20 mm)
  μPD78P0208KL-T



Cautions 1. Connect the V_{PP} pin to V_{SS} directly.

2. Connect the AV_{DD} pin to V_{DD}.

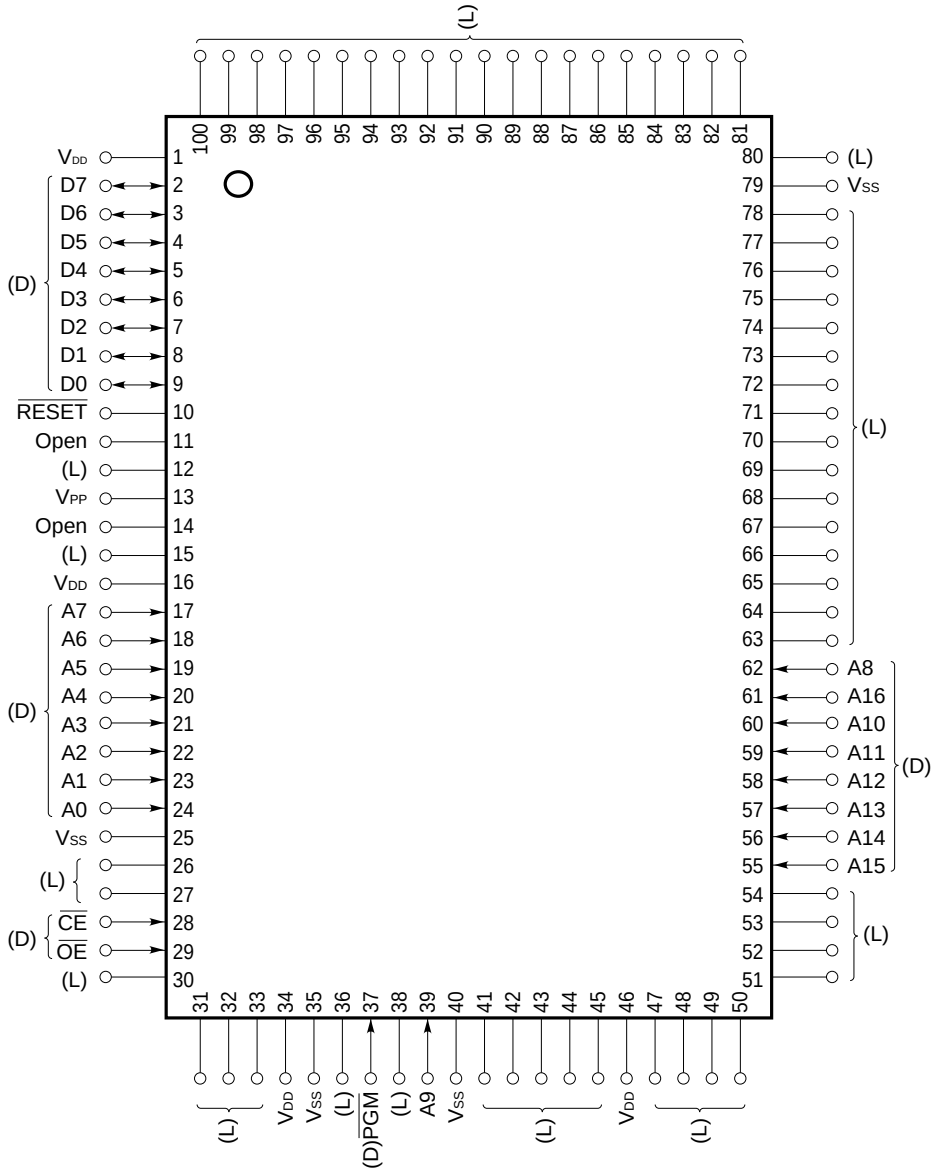
3. Connect the AV_{SS} pin to V_{SS}.

P00-P04 : Port 0
P10-P17 : Port 1
P20-P27 : Port 2
P30-P37 : Port 3
P70-P74 : Port 7
P80-P87 : Port 8
P90-P97 : Port 9
P100-P107 : Port 10
P110-P117 : Port 11
P120-P127 : Port 12
INTP0-INTP3 : Interrupt from Peripherals
TI0-TI2 : Timer Input
TO0-TO2 : Timer Output
SB0, SB1 : Serial Bus
SI0, SI1 : Serial Input
SO0, SO1 : Serial Output
$\overline{SCK0}$, $\overline{SCK1}$: Serial Clock

PCL : Programmable Clock
BUZ : Buzzer Clock
STB : Strobe
BUSY : Busy
FIP0-FIP52 : Fluorescent Indicator Panel
V_{LOAD} : Negative Power Supply
X1, X2 : Crystal (Main System Clock)
XT1, XT2 : Crystal (Subsystem Clock)
$\overline{RESET}$: Reset
ANI0-ANI7 : Analog Input
AV_{DD} : Analog Power Supply
AV_{SS} : Analog Ground
AV_{REF} : Analog Reference Voltage
V_{DD} : Power Supply
V_{PP} : Programming Power Supply
V_{SS} : Ground

(2) PROM programming mode

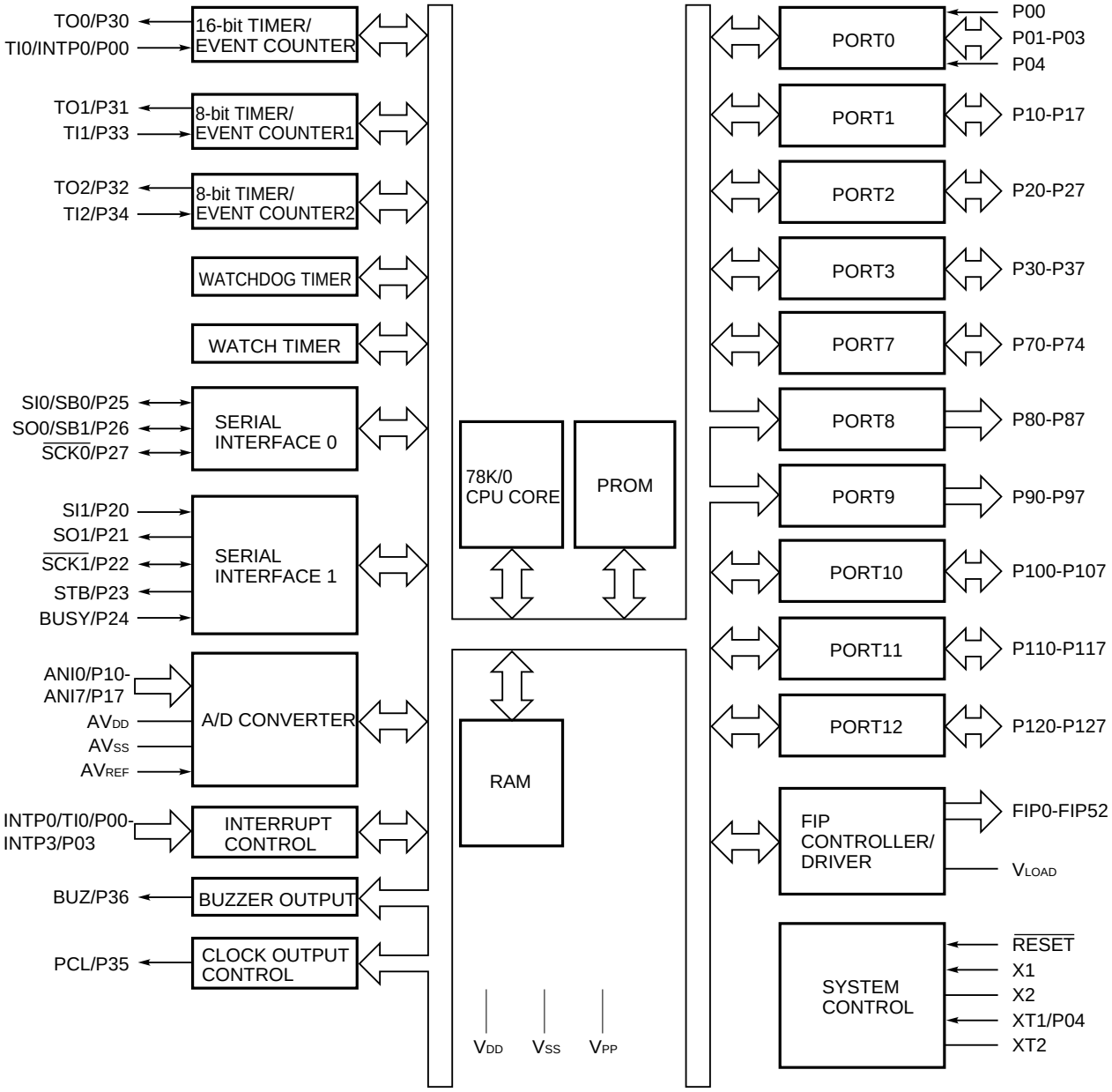
- 100-pin plastic QFP (14 × 20 mm)
  μPD78P0208GF-3BA
- 100-pin ceramic WQFN (14 × 20 mm)
  μPD78P0208KL-T



Cautions 1. (L) : Connect to VSS through individual pull-down resistors.
2. (D) : To be connected through drivers.
3. VSS : Connect to ground.
4. $\overline{\text{RESET}}$: Set to low level.
5. Open : Do not connect.

A0-A16	:	Address Bus	$\overline{\text{RESET}}$	:	Reset
D0-D7	:	Data Bus	VDD	:	Power Supply
$\overline{\text{CE}}$	:	Chip Enable	VPP	:	Programming Power Supply
$\overline{\text{OE}}$	:	Output Enable	VSS	:	Ground
$\overline{\text{PGM}}$	:	Program			

BLOCK DIAGRAM



CONTENTS

1. DIFFERENCES BETWEEN THE μPD78P0208 AND MASK ROM PRODUCTS

The μPD78P0208 contains an on-chip one-time PROM in which data can be written once or an EPROM featuring repetitive program write and deletion.

Functions other than PROM specifications and mask options can be set as equivalent to those of mask ROM products, by setting the internal memory switching register (IMS) and internal expansion RAM switching register (IXS) accordingly.

Table 1-1 lists the points of difference between the μPD78P0208 and mask ROM products.

Table 1-1 Differences between μPD78P0208 and Mask ROM Products

Item	μPD78P0208	Mask ROM products
ROM structure	One-time PROM/EPROM	Mask ROM
ROM capacity	60K bytes	μPD780204 : 32K bytes μPD780205 : 40K bytes μPD780206 : 48K bytes μPD780208 : 60K bytes
Internal expansion RAM capacity	1024 bytes	μPD780204 : None μPD780205 : None μPD780206 : 1024 bytes μPD780208 : 1024 bytes
Changing the internal ROM capacity using the internal memory switching register (IMS)	Possible**Note 1**	Impossible
Changing the internal expansion RAM capacity using the internal expansion RAM switching register (IXS)	Possible**Note 2**	Impossible
Includes IC pins	No	Yes
Includes V_{PP} pins	Yes	No
P30/TO0-P32/TO2,P33/TI1 P34/TI2, P35/PCL, P36/BUZ, P37	No on-chip pull-down resistors	An on-chip pull-down resistor can be incorporated for each pin by specifying mask options.
P70-P74	No on-chip pull-up resistors	An on-chip pull-up resistor can be incorporated for each pin by specifying mask options.
FIP0-FIP12	On-chip pull-down resistors provided (connect to V_{LOAD})	An on-chip pull-down resistor can be incorporated for each pin by specifying mask options.
P80/FIP13-P87/FIP20 P90/FIP21-P97/FIP28 P100/FIP29-P107/FIP36 P110/FIP37-P117/FIP44 P120/FIP45-P127/FIP52	No on-chip pull-down resistors	An on-chip pull-down resistor can be incorporated for each pin by specifying mask options. (These pins can be connected to V_{LOAD} or V_{SS} in four-bit units.)
Electrical characteristics	Refer to the data sheet of each product.	

Notes 1. A $\overline{\text{RESET}}$ input sets the internal PROM capacity to 60K bytes.

2. A $\overline{\text{RESET}}$ input sets the internal expansion RAM capacity to 1024 bytes.

2. LIST OF PIN FUNCTIONS

2.1 PINS FOR NORMAL OPERATING MODE

(1) Port pins (1/2)

Pin name	I/O	Function		Reset	Combination pin
P00	Input	Port 0.	Input only	Input	INTP0/TI0
P01	I/O	5-bit I/O port.	Each pin can be designated as an input or output pin separately. If used as an input port, an on-chip pull-up resistor can be used by software.	Input	INTP1
P02					INTP2
★ P03					INTP3
P04 Note 1	Input		Input only	Input	XT1
P10-P17	I/O	Port 1. 8-bit I/O port. Each pin can be designated as an input or output pin separately. If used as an input port, an on-chip pull-up resistor can be used by software. Note 2		Input	ANI0-ANI7
P20	I/O	Port 2. 8-bit I/O port. Each pin can be designated as an input or output pin separately. If used as an input port, an on-chip pull-up resistor can be used by software.		Input	SI1
P21					SO1
P22					$\overline{SCK1}$
P23					STB
P24					BUSY
P25					SI0/SB0
P26					SO0/SB1
P27					$\overline{SCK0}$
P30	I/O	Port 3. 8-bit I/O port. Each pin can be designated as an input or output pin separately. Can directly drive LEDs. If used as an input port, an on-chip pull-up resistor can be used by software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—

Notes 1. When using pin combination P04/XT1 as an input port, set bit 6 of the processor clock control register (PCC) to 1 (do not use the subsystem clock oscillator circuit's on-chip feedback resistor).

2. When using pin combination P10/ANI0-P17/ANI7 as the analog input for the A/D converter, set input mode for port 1. This setting disables the on-chip pull-up resistors.

(1) Port pins (2/2)

Pin name	I/O	Function	Reset	Combination pin
P70-P74	I/O	Port 7. N-ch open-drain 5-bit I/O port. Each pin can be designated as an input or output pin separately. Can directly drive LEDs.	Input	—
P80-P87	Output	Port 8. P-ch open-drain 8-bit high withstand voltage output port. Can directly drive LEDs.	Output	FIP13-FIP20
P90-P97	Output	Port 9. P-ch open-drain 8-bit high withstand voltage output port. Can directly drive LEDs.	Output	FIP21-FIP28
P100-P107	I/O	Port 10. P-ch open-drain 8-bit high withstand voltage output port. Each pin can be designated as an input or output pin separately. Can directly drive LEDs.	Input	FIP29-FIP36
P110-P117	I/O	Port 11. P-ch open-drain 8-bit high withstand voltage I/O port. Each pin can be designated as an input or output pin separately. Can directly drive LEDs.	Input	FIP37-FIP44
P120-P127	I/O	Port 12. P-ch open-drain 8-bit high withstand voltage I/O port. Each pin can be designated as an input or output pin separately. Can directly drive LEDs.	Input	FIP45-FIP52

(2) Non-port pins (1/2)

Pin name	I/O	Function	Reset	Combination pin
INTP0	Input	Can be set for effective edge (rising edge, falling edge, or both rising and falling edges). Inputs external interrupts.	Input	P00/TI0
INTP1				P01
INTP2				P02
★ INTP3		Falling edge detection and external interrupt input	Input	P03
SI0	Input	Input of serial data for serial interface	Input	P25/SB0
SI1				P20
SO0	Output	Output of serial data for serial interface	Input	P26/SB1
SO1				P21
SB0	I/O	Input/output of serial data for serial interface	Input	P25/SI0
SB1				P26/SO0
$\overline{SCK0}$	I/O	Serial clock input/output for serial interface	Input	P27
$\overline{SCK1}$				P22
STB	Output	Output of automatic transmit/receive strobe signal for serial interface	Input	P23
BUSY	Input	Input of automatic transmit/receive busy signal for serial interface	Input	P24
TI0	Input	External count clock input to 16-bit timer (TM0)	Input	P00/INTP0
TI1		External count clock input to 8-bit timer (TM1)		P33
TI2		External count clock input to 8-bit timer (TM2)		P34
TO0	Output	16-bit timer (TM0) output (combined with 14-bit PWM output)	Input	P30
TO1		8-bit timer (TM1) output		P31
TO2		8-bit timer (TM2) output		P32
PCL	Output	Clock output (for trimming main system clock or sub-system clock)	Input	P35
BUZ	Output	Buzzer output	Input	P36
FIP0-FIP12	Output	High current output with high withstand voltage for the grids/segments of FIP controller/driver On-chip pull-down resistors provided (connect to V_{LOAD})	Output	—
FIP13-FIP20	Output	High current output with high withstand voltage for the grids/segments of FIP controller/driver	Output	P80-P87
FIP21-FIP28	Output	High current output with high withstand voltage for the grids/segments of FIP controller/driver	Output	P90-P97
FIP29-FIP36			Input	P100-P107
FIP37-FIP44				P110-P117
FIP45-FIP52				P120-P127
V_{LOAD}	—	Pull-down resistor connection for FIP controller/driver	—	—

(2) Non-port pins (2/2)

Pin name	I/O	Function	Reset	Combination pin
ANI0-ANI7	Input	Analog input for A/D converter	Input	P10-P17
AV_{REF}	Input	Reference voltage input for A/D converter	—	—
AV_{DD}	—	Analog power supply for A/D converter. Connect to V_{DD}.	—	—
AV_{SS}	—	Ground for A/D converter. Connect to V_{SS}.	—	—
$\overline{RESET}$	Input	System reset input	—	—
X1	Input	Crystal connection for main system clock oscillation	—	—
X2	—		—	—
XT1	Input	Crystal connection for subsystem clock oscillation	Input	P04
XT2	—		—	—
V_{DD}	—	Positive power supply	—	—
V_{PP}	—	Connect to V_{SS}.	—	—
V_{SS}	—	Ground level	—	—

2.2 PINS FOR PROM PROGRAMMING MODE

Pin name	I/O	Function
$\overline{RESET}$	Input	PROM programming mode selection. PROM programming mode is selected when +5 V or +12.5 V is added to the V_{PP} pin or low-level input is added to the $\overline{RESET}$ pin.
V_{PP}	Input	PROM programming mode selection and high voltage input during program write or verification
A0-A16	Input	Address bus
D0-D7	I/O	Data bus
$\overline{CE}$	Input	PROM enable input/program pulse input
$\overline{OE}$	Input	Read strobe input to PROM
$\overline{PGM}$	Input	Program/program inhibit input during PROM programming mode
V_{DD}	—	Positive power supply
V_{SS}	—	Ground level

2.3 I/O CIRCUITS FOR PINS AND TREATMENT OF UNUSED PINS

Table 2-1 describes the types of I/O circuits for pins and the treatment of unused pins.

Fig. 2-1 shows the configuration of these various types of I/O circuits.

Table 2-1 Types of I/O Circuits for Pins (1/2)

Pin name	I/O circuit type	I/O	Recommended connection method for unused pins
P00/INTP0/TI0	2	Input	Connect to V_{SS}.
P01/INTP1	8-A	I/O	Connect to V_{SS} through a separate resistor.
P02/INTP2			
P03/INTP3			
P04/XT1	16	Input	Connect to V_{DD} or V_{SS}.
P10/ANI0-P17/ANI7	11	I/O	Connect to V_{DD} or V_{SS} through a separate resistor.
P20/SI1	8-A		
P21/SO1	5-A		
P22/$\overline{SCK1}$	8-A		
P23/STB	5-A		
P24/BUSY	8-A		
P25/SI0/SB0	10-A		
P26/SO0/SB1			
P27/$\overline{SCK0}$			
P30/TO0	5-A		
P31/TO1			
P32/TO2			
P33/TI1	8-A		
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
★ P70-P74	13-D		
FIP0-FIP12	14	Output	Open
P80/FIP13-P87/FIP20	14-B		
P90/FIP21-P97/FIP28			

Table 2-1 Types of I/O Circuits for Pins (2/2)

Pin name	I/O circuit type	I/O	Recommended connection method for unused pins
P100/FIP29-P107/FIP36	15-B	I/O	Connect to V_{DD} or V_{SS} through a separate resistor. ★
P110/FIP37-P117/FIP44			
P120/FIP45-P127/FIP52			
$\overline{RESET}$	2	Input	—
XT2	16	—	Open
AV_{REF}	—		Connect to V_{SS}.
AV_{DD}			Connect to V_{DD}.
AV_{SS}			Connect to V_{SS}.
V_{LOAD}			
V_{PP}			Connect to V_{SS} directly.

Fig. 2-1 List of I/O Circuits for Pins (1/2)

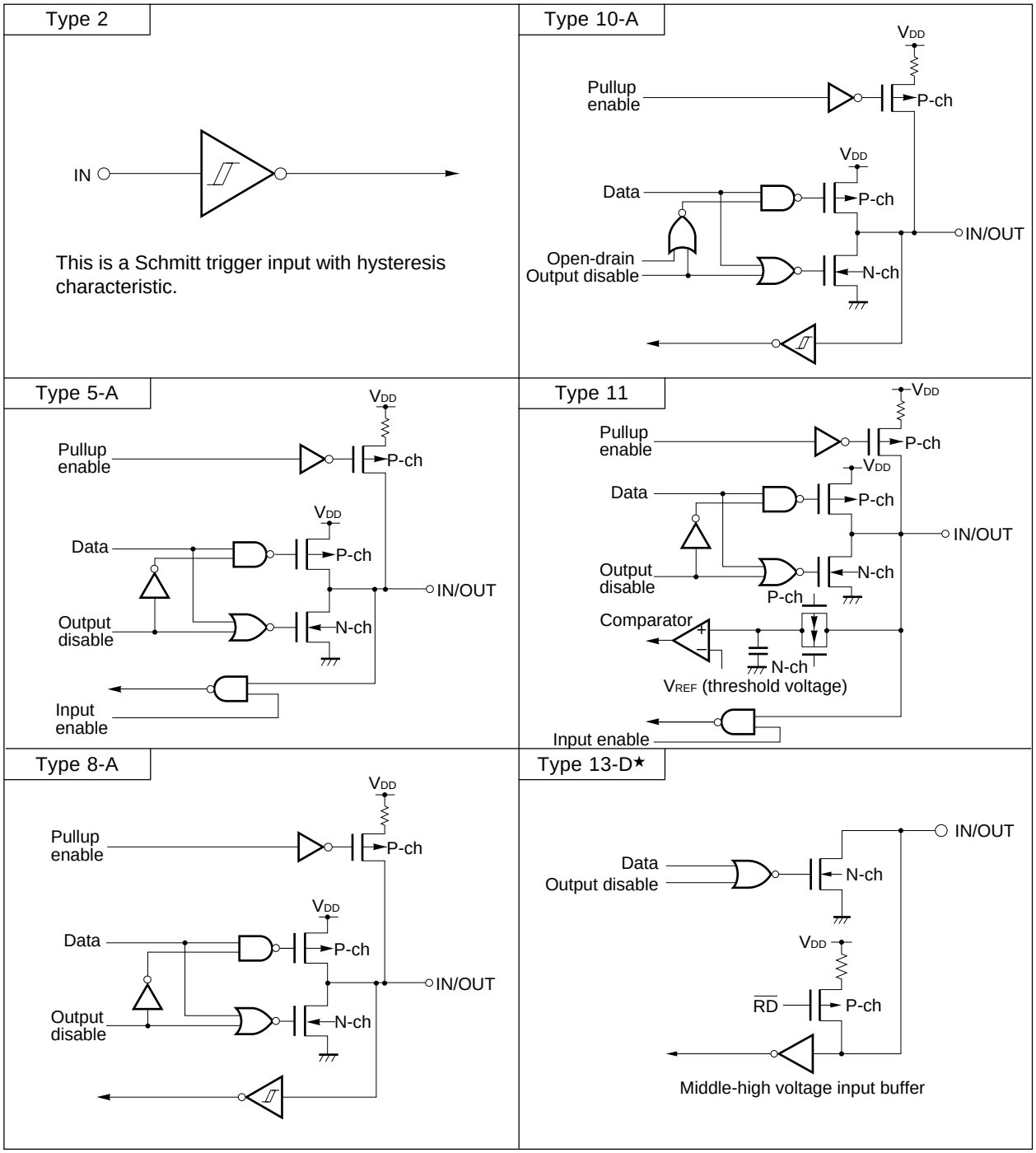
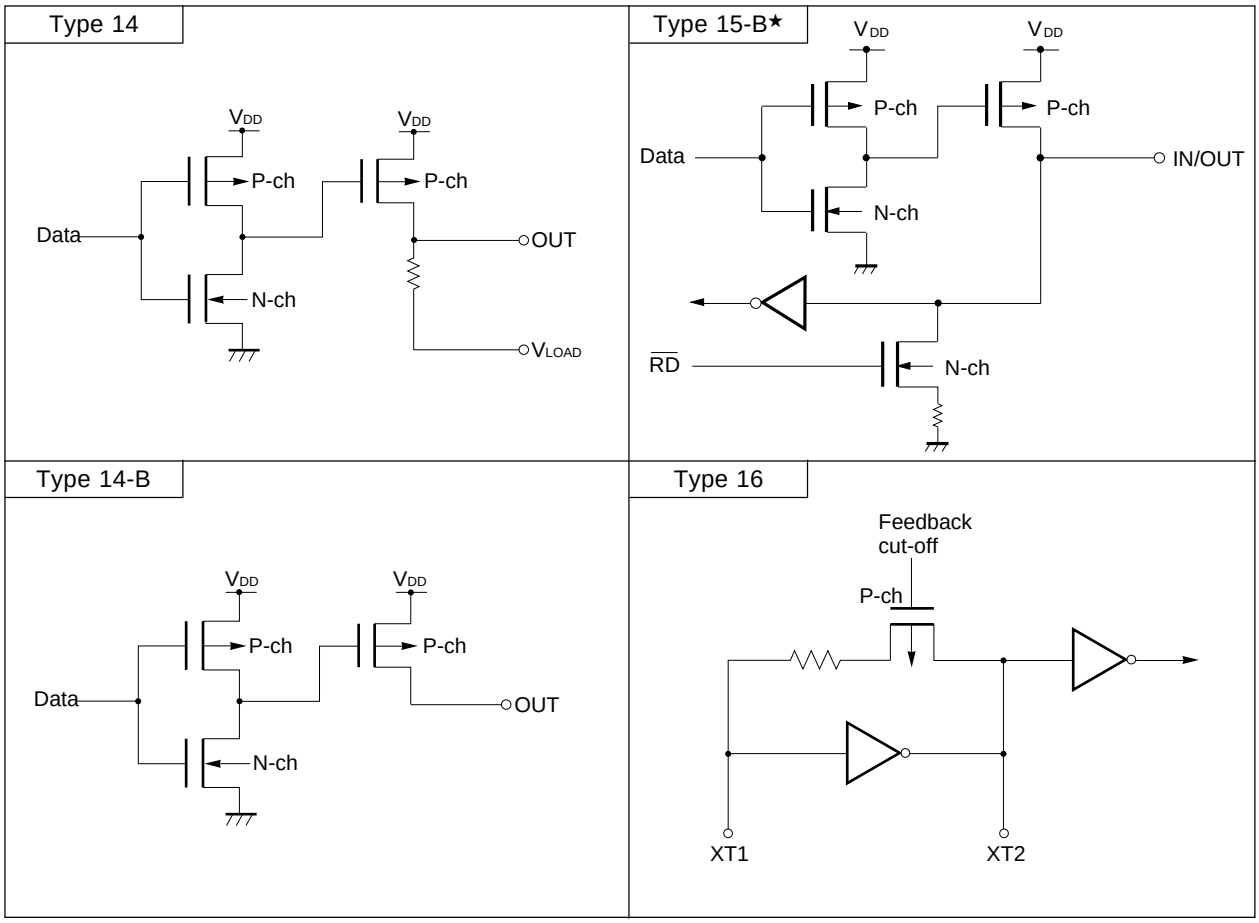


Fig. 2-1 List of I/O Circuits for Pins (2/2)



3. INTERNAL MEMORY SWITCHING (IMS) REGISTER

This register enables the software to avoid using part of the internal memory. The IMS register can be set to establish the same memory mapping as used in ROM products that have a different internal ROM capacity.

The IMS register is set using 8-bit memory operation instructions.

A $\overline{\text{RESET}}$ input sets the IMS register to CFH.

Fig. 3-1 Format of IMS Register

Symbol	7	6	5	4	3	2	1	0	Address	Reset value	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CFH	R/W

ROM3	ROM2	ROM1	ROM0	Internal ROM capacity selection
1	0	0	0	32K bytes
1	0	1	0	40K bytes
1	1	0	0	48K bytes
1	1	1	1	60K bytes
Other than above				Setting prohibited

RAM2	RAM1	RAM0	Internal high-speed RAM selection
1	1	0	1024 bytes
Other than above			Setting prohibited

Table 3-1 lists IMS register settings for memory mapping equivalent to various mask ROM products.

Table 3-1 IMS Register Settings

Target mask ROM product	IMS setting
μPD780204	C8H
μPD780205	CAH
μPD780206	CCH
μPD780208	CFH

4. INTERNAL EXPANDED RAM SWITCHING (IXS) REGISTER

The μPD78P0208 can set the IXS register to establish the same memory mapping as used in ROM products that have a different internal expanded RAM capacity.

The IXS register is set using 8-bit memory operation instructions.

A $\overline{\text{RESET}}$ input sets the IXS register to 0AH.

Fig. 4-1 Format of IXS Register

Symbol	7	6	5	4	3	2	1	0	Address	Reset value	R/W
IXS	0	0	0	0	IXRAM3	IXRAM2	IXRAM1	IXRAM0	FFF4H	0AH	W

IXRAM3	IXRAM2	IXRAM1	IXRAM0	Internal expanded RAM capacity selection
1	0	1	0	1024 bytes
1	1	0	0	No internal expanded
Other than above				Setting prohibited

Table 4-1 lists IXS register settings for memory mapping equivalent to various mask ROM products.

Table 4-1 IXS Register Settings

Target mask ROM product	IXS setting	
μPD780204	0CH	
μPD780205		
μPD780206	0AH	★
μPD780208		★

5. PROM PROGRAMMING

The μPD78P0208 has an on-chip 60KB PROM device for use as program memory. When programming, set the V_{PP} and $\overline{RESET}$ pins for PROM programming mode. See **(2) PROM programming mode** in PIN CONFIGURATION (TOP VIEW) with regard to treatment of other, unused pins.

Caution Write a program in the range between addresses 0000H and EFFFH. (Set EFFFH in the program-end address.) PROM programmers which cannot specify the writing address cannot be used.

5.1 OPERATION MODE

PROM programming mode is selected when +5 V or +12.5 V is added to the V_{PP} pin or low-level input is added to the $\overline{RESET}$ pin. This mode can be set to operation mode by setting the $\overline{CE}$ pin, $\overline{OE}$ pin, and $\overline{PGM}$ pin as shown in Table 5-1 below.

In addition, the PROM contents can be read by setting read mode.

Table 5-1 PROM Programming Operation Mode

Pin / Operation mode	$\overline{RESET}$	V_{PP}	V_{DD}	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	D0-D7
Page data latch	L	+12.5 V	+6.5 V	H	L	H	Data input
Page write				H	H	L	High impedance
Byte write				L	H	L	Data input
Program verify				L	L	H	Data output
Program inhibit				×	H	H	High impedance
				×	L	L	
Read		+5 V	+5 V	L	L	H	Data output
Output disable				L	H	×	High impedance
Standby				H	×	×	High impedance

× = L or H

(1) Read mode

Set $\overline{CE}$ to L and $\overline{OE}$ to L to set read mode.

(2) Output disable mode

Set $\overline{OE}$ to H to set high impedance for data output and output disable mode.

Consequently, if several μPD78P0208 devices are connected to a data bus, the $\overline{OE}$ pins can be controlled to select data output from any of the devices.

(3) Standby mode

Set $\overline{CE}$ to H to set standby mode.

In this mode, data output is set to high impedance regardless of the $\overline{OE}$ setting.

(4) Page data latch mode

At the beginning of page write mode, set $\overline{CE}$ to H, $\overline{PGM}$ to H, and $\overline{OE}$ to L to set page data latch mode.

In this mode, 1 page (4 bytes) of data are latched to the internal address/data latch circuit.

(5) Page write mode

After latching the address and data for one page (4 bytes) using page data latch mode, adding a 0.1 ms program pulse (active, low) to the $\overline{PGM}$ pin with both $\overline{CE}$ and $\overline{OE}$ set to H causes page write to be executed. Later, setting both $\overline{CE}$ and $\overline{OE}$ to L causes program verification to be executed.

If programming is not completed after one program pulse, the write and verify operations may be repeated X times (where X - 10).

(6) Byte write mode

Adding a 0.1 ms program pulse (active, low) to the $\overline{PGM}$ pin with $\overline{CE}$ set to L and $\overline{OE}$ set to H causes byte write to be executed. Later, setting $\overline{OE}$ to L causes program verification to be executed.

If programming is not completed after one program pulse, the write and verify operations may be repeated X times (where X - 10).

(7) Program verify mode

Set $\overline{CE}$ to L, $\overline{PGM}$ to H, and $\overline{OE}$ to L to set program verify mode. Use verify mode for verification following each write operation.

(8) Program inhibit mode

Program inhibit mode is used to write to a single device when several μPD78P0208 devices are connected in parallel to $\overline{OE}$, V_{PP}, and D0 to D7 pins.

Use the page write mode or byte write mode described above for each write operation. Write operations cannot be done for devices in which the $\overline{PGM}$ pin has been set to H.

5.2 PROM WRITE SEQUENCE

Fig. 5-1 Page Program Mode Flowchart

G = Start address

N = Program end address

Fig. 5-2 Page Program Mode Timing

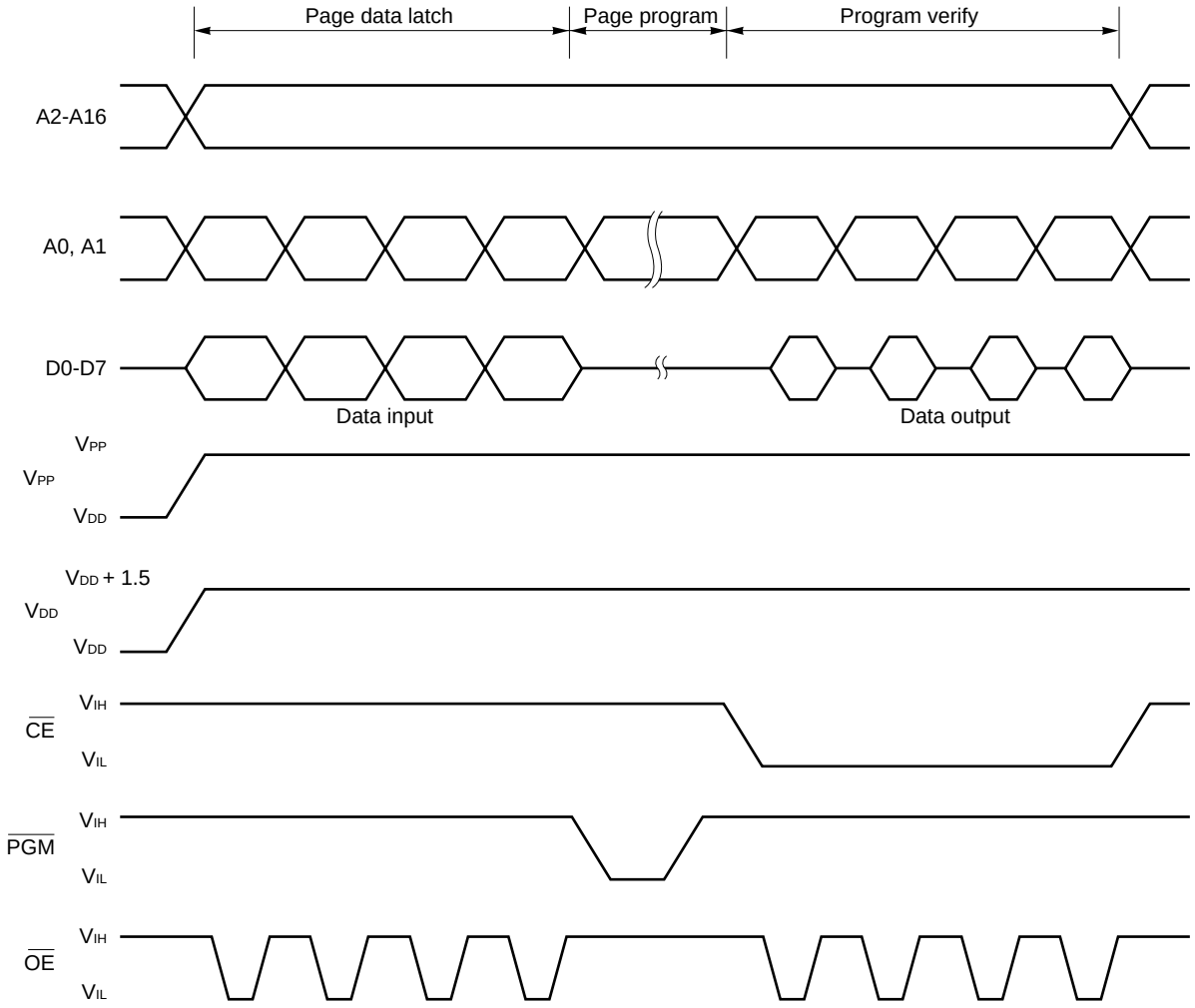
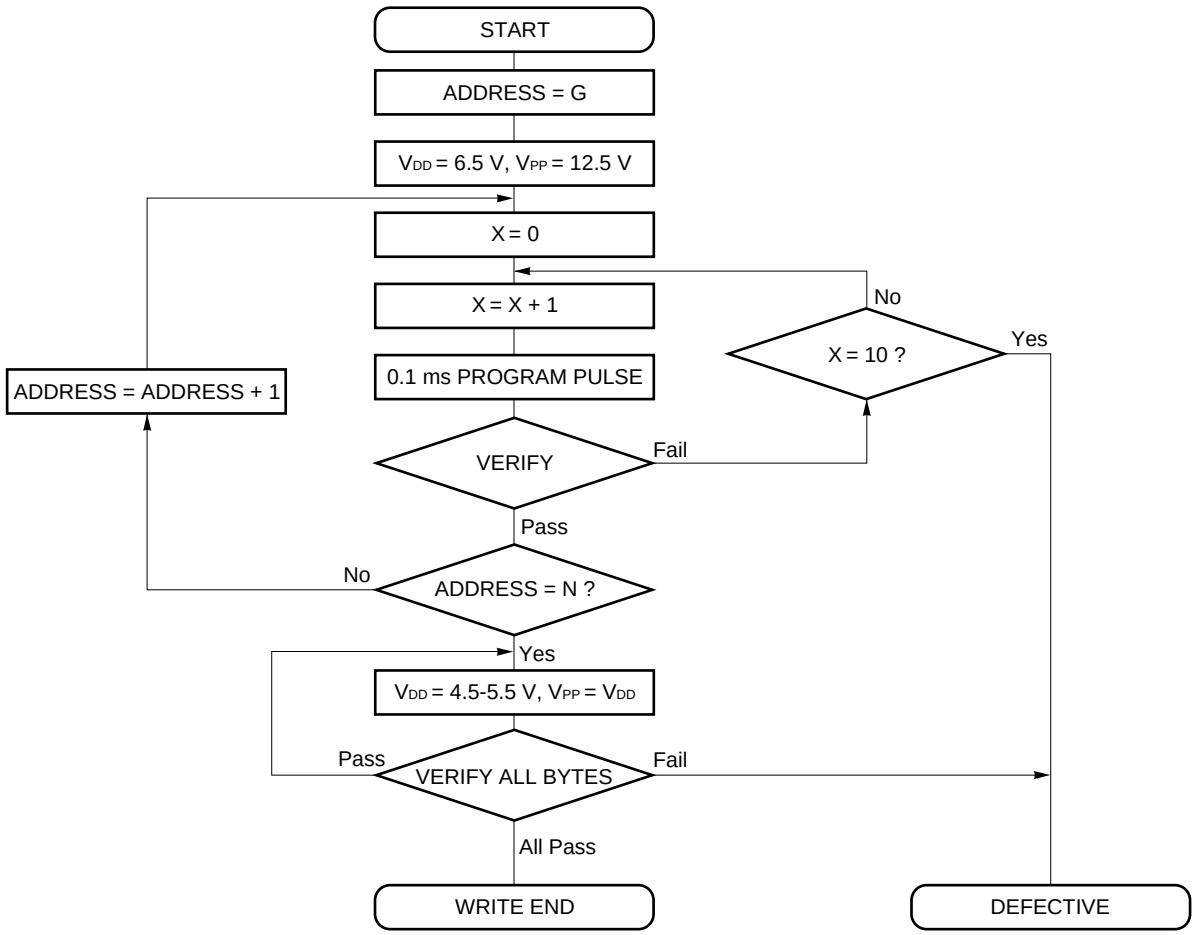


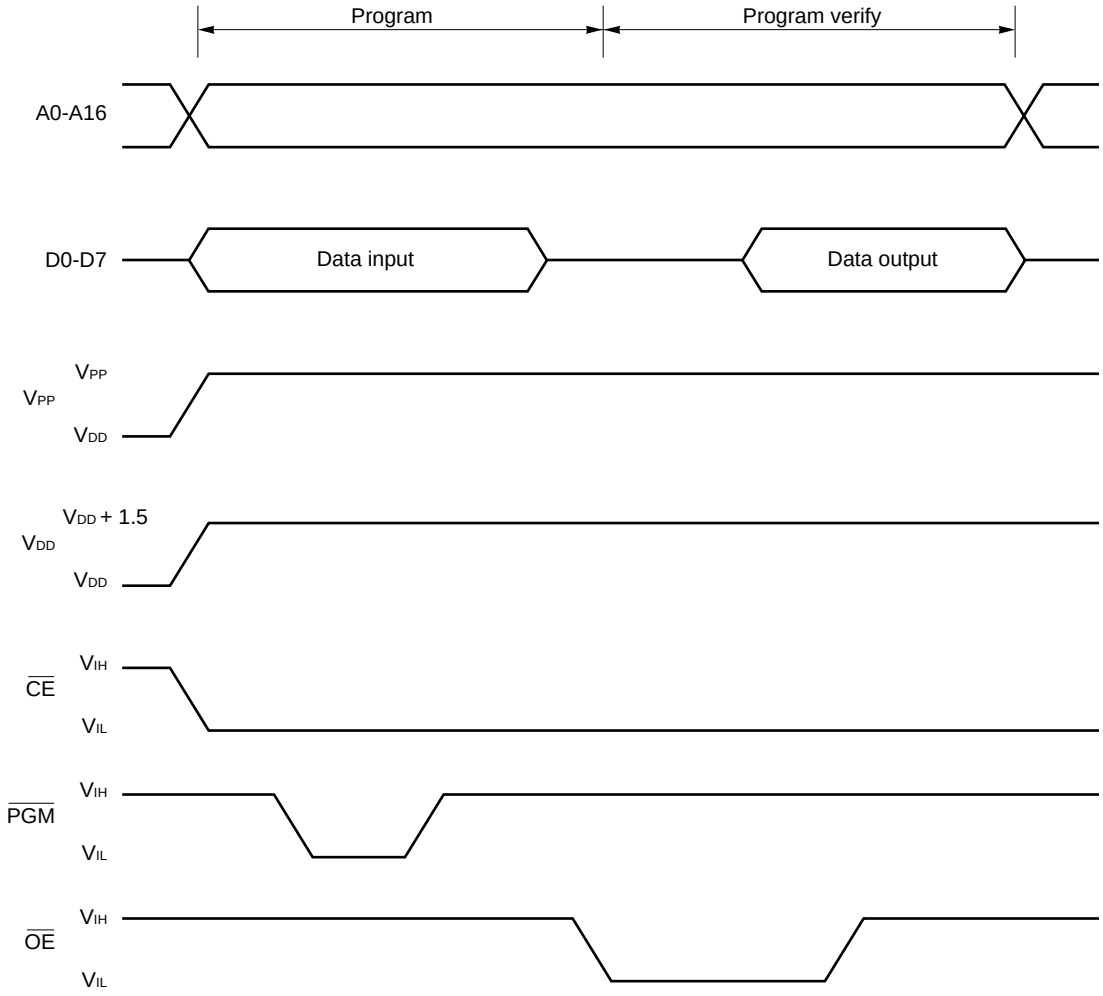
Fig. 5-3 Byte Program Mode Flowchart



G = Start address

N = Program end address

Fig. 5-4 Byte Program Mode Timing



Cautions 1. Add V_{DD} before V_{PP}, and turn off the V_{DD} after V_{PP}.

2. Do not allow V_{PP} to exceed +13.5 V including overshoot.

3. Reliability problems may result if the device is inserted or pulled out while +12.5 V is applied at V_{PP}.

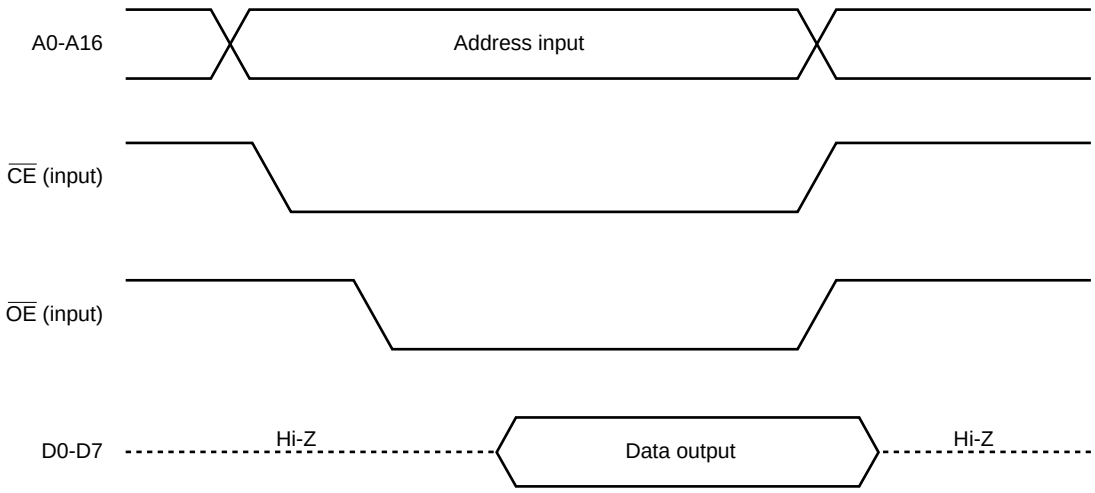
5.3 PROM READ SEQUENCE

Follow this sequence to read the PROM contents to an external data bus (D0 to D7).

(1) Set the $\overline{\text{RESET}}$ pin to low level and add +5 V to the V_{PP} pin. See **(2) PROM programming mode** in PIN CONFIGURATION (TOP VIEW) with regard to treatment of other, unused pins.
(2) Add +5 V to the V_{DD} and V_{PP} pins.
(3) Input the data address to be read to pins A0 to A16.
(4) Set read mode.
(5) Output the data to pins D0 to D7.

Fig. 5-5 shows the timing of steps (2) to (5) above.

Fig. 5-5 PROM Read Timing



6. ERASURE CHARACTERISTICS (μPD78P0208KL-T ONLY)

Data written in the μPD78P0208KL-T program memory can be erased (FFH); therefore users can write other data in the memory.

To erase the written data, expose the erasure window to light with a wavelength shorter than approx. 400 nm. Normally, ultraviolet light with a wavelength of 254 nm is employed. The amount of light required to completely erase the data is as follows:

- Intensity of ultraviolet light × erasing time: 30 W•s/cm^2 min. ★
- Erasing time: 40 minutes or more (When using a 12000 μW/cm^2 ultraviolet lamp. It may, however, take more time due to lamp deterioration, dirt on the erasure window, or the like.) ★

The ultraviolet lamp should be placed within 2.5 cm from the erasure window during erasure. In addition, if a filter is attached to the ultraviolet lamp, remove the filter before erasure.

7. PROTECTIVE FILM COVERING THE ERASURE WINDOW (μPD78P0208KL-T ONLY)

To prevent EPROM from being erased inadvertently by light other than that from the lamp used for erasing EPROM, or to prevent the internal circuits other than EPROM from malfunctioning by light, stick a protective film on the erasure window except when EPROM is to be erased.

8. SCREENING ONE-TIME PROM PRODUCTS

NEC cannot execute a complete test of one-time PROM products (μPD78P0208GF-3BA) due to their structure before shipment. It is recommended that you screen (verify) PROM products after writing necessary data into them and storing them at 125 °C for 24 hours.

NEC offers a charged service called QTOP microcomputer service. This service includes writing to one-time PROM, marking, screening, and verification. Ask your sales representative for details.

★ 9. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

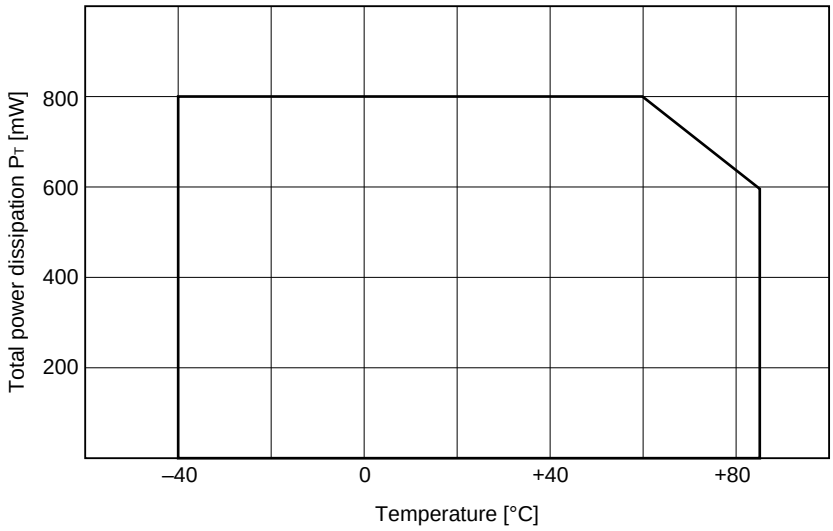
Parameter	Symbol	Conditions		Rating	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
	V_{LOAD}			V_{DD} – 45 to V_{DD} + 0.3	V
	V_{PP}			–0.3 to +13.5	V
	AV_{DD}			–0.3 to V_{DD} + 0.3	V
	AV_{REF}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltate	V_{I1}	P01 to P04, P10 to P17, P20 to P27, P30 to P37, X1, X2, $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P00/A9		–0.3 to +13.5	V
	V_{I3}	P70-P74	N-ch open drain	–0.3 to +16	V
	V_{I4}	P100 to P107, P110 to P117, P120 to P127	P-ch open drain	V_{DD} – 45 to V_{DD} + 0.3	V
Output voltage	V_O	P01 to P03, P10 to P17, P20 to P27, P30 to P37, P70 to P74		–0.3 to V_{DD} + 0.3	V
	V_{OD}	P80 to P87, P90 to P97, P100 to P107, P110 to P117, P120 to P127, FIP0 to FIP12		V_{DD} – 45 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	ANI0 to ANI7	Analog input pins	AV_{SS} – 0.3 to AV_{REF} + 0.3	V
High-level output current	I_{OH} **Note1**	1 pin of P01 to P03, P10 to P17, P20 to P27, P30 to P37		–10	mA
		Total for P01 to P03, P10 to P17, P02 to P27, P30 to P37		–30	mA
		1 pin of FIP0 to FIP12, P80 to P87, P90 to P97, P100 to P107, P110 to P117, P120 to P127		–30	mA
		Total for P80 to P87, FIP0 to FIP12	Peak value	–240	mA
			RMS	–120	mA
		Total for P90 to P97, P100 to P107, P110 to P117, P120 to P127	Peak value	–100	mA
			RMS	–60	mA
Low-level output current	I_{OL} **Note1**	1 pin of P01 to P03, P10 to P17, P20 to P27, P30 to P37, P70 to P74	Peak value	30	mA
			RMS	15	mA
		Total for P01 to P03, P10 to P17, P20 to 27, P30 to P37	Peak value	50	mA
			RMS	20	mA
		Total for P70 to P74	Peak value	100	mA
			RMS	60	mA
Total power dissipation	P_T **Note 2**	T_A = –40 to +60 °C		800	mW
		T_A = +85 °C		600	mW
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter, or even momentarily. In other words, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

Remark Unless otherwise specified, shared pin characteristics are the same as port pin characteristics.

Notes 1. The RMS should be calculated as follows: [RMS value] = [Peak value] × $\sqrt{\text{Duty}}$

Notes 2. Total power dissipation differs depending on the temperature (see the following figure).



How to calculate total power dissipation

The total power dissipation of the μPD78P0208GF is the sum of the values at the following three parts. Design your application set so that the sum is lower than the total power dissipation P_T. (The recommended operating condition is 80% or lower of the rated value.)

<1> CPU: the power consumed by CPU and calculated with V_{DD} (max.) × I_{DD1} (max.)

<2> Output pins: the power consumption when the maximum current flows at all output pins (normal output and display output).

<3> Pull-down resistors: the power dissipated at the on-chip pull-down resistors connected to display output pins

The calculation example of the total power dissipation is provided below. The following total power dissipation calculation example assumes the case where the characters shown in the figure on the next page are displayed.

Example: The operating conditions are as follows:

V_{DD} = 5 V ±10%, operating at 5.0 MHz

Supply current (I_{DD1}) = 21.6 mA

FIP display outputs: 11 grids × 10 segments (cut width is 1/16)

It is assumed that up to 15 mA flows to each grid pin, and that up to 3 mA flows to each segment pin.

It is also assumed that all display outputs are turned off at key scan timings.

Display output voltage: grid $V_{OD} = V_{DD} - 2$ V (Voltage drop of 2 V is assumed.)

segment $V_{OD} = V_{DD} - 0.4$ V (Voltage drop of 0.4 V is assumed.)

Voltage applied to fluorescent indication panel (V_{LOAD}) = –35 V

On-chip pull-down resistor = 25 kΩ

<1> Power consumption of CPU: 5.5 V × 21.6 mA = 118.8 mW

<2> Power consumption at output pins

Grid: $2\ V \times 15\ mA \times \frac{11\ grids}{12\ timings} \times (1 - 1/16) = 25.8\ mW$

Segment: $0.4\ V \times 3mA \times \frac{31\ segments}{12\ timings} \times (1 - 1/16) = 2.9\ mW$

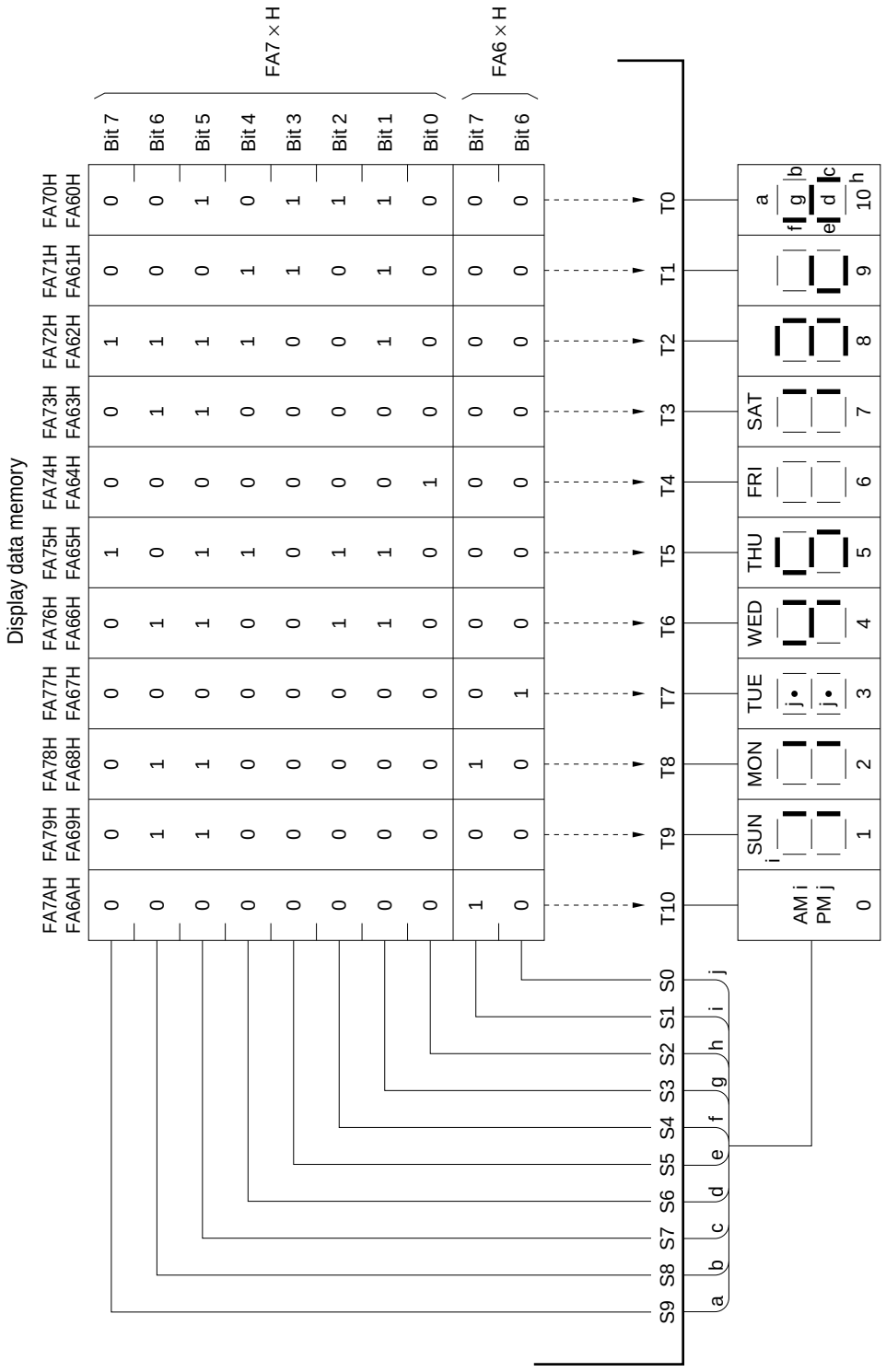
<3> Power consumption at pull-down resistors

Grid: $\frac{(35\ V + (5.5\ V - 2\ V))^2}{25\ k\Omega} \times \frac{11\ grids}{12\ timings} \times (1 - 1/16) = 50.9\ mW$

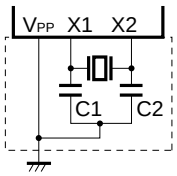
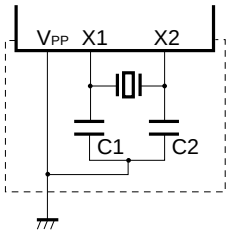
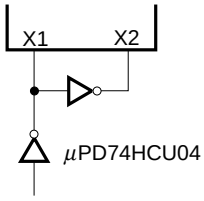
Segment: $\frac{(35\ V + (5.5\ V - 0.4\ V))^2}{25\ k\Omega} \times \frac{31\ segments}{12\ timings} \times (1 - 1/16) = 155.8\ mW$

Total power dissipation = **<1>** + **<2>** + **<3>** = 118.8 + 2.9 + 25.8 + 155.8 + 50.9 = 354.2 mW (< P_T = 600 mW)

According to the graph shown on the previous page,the total power dissipation in the temperature range of T_A = –40 to +85 °C must be lower than 600 mW. Therefore, the calculation result in this example (354.2 mW) satisfies the requirement. If the calculation result for the total power dissipation becomes higher than the rated value, the power consumption must be reduced.


Display data memory
FA7AH FA79H FA78H FA77H FA76H FA75H FA74H FA73H FA72H FA71H FA70H
FA6AH FA69H FA68H FA67H FA66H FA65H FA64H FA63H FA62H FA61H FA60H
Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0
FA7 × H
FA6 × H
Bit 7 Bit 6
T0 T1 T2 T3 T4 T5 T6 T7 T8 T9 T10
S0 S1 S2 S3 S4 S5 S6 S7 S8 S9
a b c d e f g h i j
AM i
PM j
SUN MON TUE WED THU FRI SAT
0 1 2 3 4 5 6 7 8 9 10h

MAIN SYSTEM CLOCK OSCILLATION CIRCUIT CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Resonator	Recommended circuit	Parameter	Conditions	Min.	Typ.	Max.	Unit
Ceramic resonator		Oscillator frequency (f_X)**Note 1**		1		5	MHz
		Oscillation settling time**Note 2**				4	ms
Crystal resonator		Oscillator frequency (f_X)**Note 1**		1	4.19	5	MHz
		Oscillation settling time**Note 2**	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (f_X)**Note 1**		1		5	MHz
		X1 input high-/low-level width (t_{XH}/t_{XL})		85		500	ns

Notes 1. Only the oscillator characteristics are shown. See **AC characteristics** for instruction execution times.

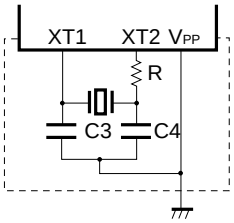
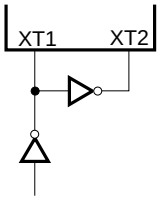
2. This is the time required for oscillation to stabilize after a reset or STOP mode release.

Cautions 1. When the main system clock oscillator is used, the following should be noted concerning wiring in the area in the figure enclosed by a broken line to prevent the influence of wiring capacitance, etc.

- **The wiring should be kept as short as possible.**
- **No other signal lines should be crossed.**
- **Keep away from lines carrying a high fluctuating current.**
- **The oscillator capacitor grounding point should always be at the same potential as V_{SS}.**
- **Do not connect to a ground pattern carrying a high current.**
- **A signal should not be taken from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation settling time has been secured by the program before switching back to the main system clock.

SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Resonator	Recommended circuit	Parameter	Conditions	Min.	Typ.	Max.	Unit
Crystal resonator		Oscillator frequency (f_{XT})**Note 1**		32	32.768	35	kHz
		Oscillation settling time**Note 2**	V_{DD} = 4.5 to 5.5 V		1.2	2	s
						10	
External clock		XT1 input frequency (f_{XT})**Note 1**		32		100	kHz
		XT1 input high-/low-level width (t_{XTH}/t_{XTL})		5		15	μs

Notes 1. Only the oscillator characteristics are shown. See **AC characteristics** for instruction execution times.

2. This is the time required for oscillation to stabilize after power (V_{DD}) is turned on.

Cautions 1. When the subsystem clock oscillator is used, the following should be noted concerning wiring in the area in the figure enclosed by a broken line to prevent the influence of wiring capacitance, etc.

- **The wiring should be kept as short as possible.**
- **No other signal lines should be crossed.**
- **Keep away from lines carrying a high fluctuating current.**
- **The oscillator capacitor grounding point should always be at the same potential as V_{SS}.**
- **Do not connect to a ground pattern carrying a high current.**
- **A signal should not be taken from the oscillator.**

2. The subsystem clock oscillator is a low-amplitude circuit in order to achieve a low consumption current, and is more prone to misoperation due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

RECOMMENDED OSCILLATOR CONSTANT

Main System Clock: Ceramic Resonator (T_A = –40 to +85 ½C)

Manufacturer	Product name	Frequency (MHz)	Circuit constant		Oscillator voltage range		Remark
			C1 (pF)	C2 (pF)	Min. (V)	Max. (V)	
Murata Mfg. Co., Ltd.	CSB1000J	1.0	100	100	2.80	5.50	
Toyama	CSA2.00MG040	2.0	100	100	2.96	5.50	
	CST2.00MG040	2.0	—	—	2.96	5.50	Built-in capacitor
	CSA4.00MG	4.0	30	30	2.85	5.50	
	CST4.00MGW	4.0	—	—	2.85	5.50	Built-in capacitor
	CSA5.00MG	5.0	30	30	3.05	5.50	
	CST5.00MGW	5.0	—	—	3.05	5.50	Built-in capacitor
TDK Corp.	CCR1000K2	1.0	100	100	2.70	5.50	
	FCR4.00MC5	4.0	—	—	2.75	5.50	Built-in capacitor
	CCR4.00MC3	4.0	—	—	2.70	5.50	Built-in capacitor
	FCR5.00MC5	5.0	—	—	2.78	5.50	Built-in capacitor
	CCR5.00MC3	5.0	—	—	2.75	5.50	Built-in capacitor
Matsushita Electronics	EFOEC5004A4	5.0	—	—	2.70	5.50	Built-in capacitor
Components Co., Ltd.	EFOEN5004A4	5.0	—	—	2.70	5.50	Built-in capacitor
	EFOS5004B5	5.0	—	—	2.70	5.50	Built-in capacitor Surface-mount type

Caution The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation but do not guarantee accuracy of the oscillation frequency. If the application circuit requires accuracy of the oscillation frequency, it is necessary to set the oscillation frequency of the resonator in the application circuit. For this, it is necessary to directly contact the manufacturer of the resonator being used.

Subsystem Clock: Crystal Resonator (T_A = –40 to +85½C)

Manufacturer	Product name	Frequency (kHz)	Circuit constant			Oscillator voltage range	
			C3 (pF)	C4 (pF)	R (kΩ)	Min. (V)	Max. (V)
Kinseki, Ltd.	P-3 (Load capacitance 12 pF)	32.768	15	33	220	2.7	5.5

Caution The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation but do not guarantee accuracy of the oscillation frequency. If the application circuit requires accuracy of the oscillation frequency, it is necessary to set the oscillation frequency of the resonator in the application circuit. For this, it is necessary to directly contact the manufacturer of the resonator that being used.

CAPACITANCE (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V				15	pF
Output capacitance	C_{OUT}	f = 1 MHz Unmeasured pins returned to 0 V				35	pF
Input/output capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V	P01 to P03, P10 to P17, P20 to P27, P30 to P37			15	pF
			P70 to P74			20	pF
			P100 to P107, P110 to P117, P120 to P127			35	pF

Remark Unless otherwise specified, shared pin characteristics are the same as port pin characteristics.

OPERATING POWER SUPPLY VOLTAGE (T_A = –40 to +85 °C)

Parameter	Conditions	Min.	Typ.	Max.	Unit
CPU**Note 1**		2.7**Note 2**		5.5	V
Display controller		4.5		5.5	V
PWM mode of 16-bit timer/ event counter (TM0)		4.5		5.5	V
A/D converter		4.0		5.5	V
Other hardware		2.7		5.5	V

Notes 1. Except for system clock oscillator, display controller, and PWM.

2. The operating power supply voltage differs depending on the cycle time. See **AC Characteristics**.

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
High-level input voltage	V_{IH1}	P21, P23		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P03, P20, P22, P24 to P27, P33, P34, $\overline{\text{RESET}}$		0.8V_{DD}		V_{DD}	V
	V_{IH3}	P70 to P74	N-ch open-drain	0.7V_{DD}		15	V
	V_{IH4}	X1, X2		V_{DD} – 0.5		V_{DD}	V
	V_{IH5}	XT1/P04, XT2	V_{DD} = 4.5 to 5.5 V	0.8V_{DD}		V_{DD}	V
				0.9V_{DD}		V_{DD}	V
	V_{IH6}	P10 to P17, P30 to P32, P35 to P37	V_{DD} = 4.5 to 5.5 V	0.65V_{DD}		V_{DD}	V
				0.7V_{DD}		V_{DD}	V
	V_{IH7}	P100 to P107, P110 to P117, P120 to P127	V_{DD} = 4.5 to 5.5 V	0.7V_{DD}		V_{DD}	V
				V_{DD} – 0.5		V_{DD}	V
Low-level input voltage	V_{IL1}	P21, P23		0		0.3V_{DD}	V
	V_{IL2}	P00 to P03, P20, P22, P24 to P27, P33, P34, $\overline{\text{RESET}}$		0		0.2V_{DD}	V
	V_{IL3}	P70 to P74	V_{DD} = 4.5 to 5.5 V	0		0.3V_{DD}	V
				0		0.2V_{DD}	V
	V_{IL4}	X1, X2		0		0.4	V
	V_{IL5}	XT1/P04, XT2	V_{DD} = 4.5 to 5.5 V	0		0.2V_{DD}	V
				0		0.1V_{DD}	V
	V_{IL6}	P10 to P17, P30 to P32, P35 to P37		0		0.3V_{DD}	V
	V_{IL7}	P100 to P107, P110 to P117, P120 to P127		V_{DD} – 40		0.3V_{DD}	V
High-level output voltage	V_{OH}	P01 to P03, P10 to P17, P20 to P27, P30 to P37, P80 to P87, P90 to P97, P100 to P107, P110 to P117, P120 to P127, FIP0 to FIP12	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA	V_{DD} – 1.0			V
			I_{OH} = –100 μA	V_{DD} – 0.5			V
Low-level output voltage	V_{OL1}	P30 to P37, P70 to P74	V_{DD} = 4.5 to 5.5 V I_{OL} = 15 mA		0.4	2.0	V
		P01 to P03, P10 to P17, P20 to P27	V_{DD} = 4.5 to 5.5 V I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{\text{SCK0}}$	V_{DD} = 4.5 to 5.5 V With open-drain and pull-up (R = 1 kΩ)			0.2V_{DD}	V
	V_{OL3}	I_{OL} = 400 μA				0.5	V
High-level input leakage	I_{LIH1}	V_{IN} = V_{DD}	P00 to P03, P10 to P17, P20 to P27, P30 to P37, P70 to P74, $\overline{\text{RESET}}$			3	μA
	I_{LIH2}		X1, X2, XT1/P04, XT2			20	μA
	I_{LIH3}	V_{IN} = 15 V	P70 to P74			80	μA
	I_{LIH4}	P110 to P117, P120 to P127 V_{IN} = V_{DD}	V_{DD} = 4.5 to 5.5 V			3**Note 1**	μA
						3**Note 2**	μA

Notes 1. For P110 to P117 and P120 to P127, a high-level input leakage current of 50 μA (MAX.) flows only during the 1.5 clocks (no-wait time) after an instruction has been executed to read out ports 11, 12 (P11, P12) or port mode registers 11, 12 (PM11, PM12). Outside the period of 1.5 clocks following executing a read-out instruction, the current is 3 μA (MAX.).

2. For P110 to P117 and P120 to P127, a high-level input leakage current of 30 μA (MAX.) flows only during the 1.5 clocks (no-wait time) after an instruction has been executed to read out P11, P12, PM11, and PM12. Outside the period of 1.5 clocks following executing a read-out instruction, the current is 3 μA (MAX.).

Remark Unless otherwise specified, shared pin characteristics are the same as port pin characteristics.

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Low-level input leakage current	I_{LIL1}	V_{IN} = 0 V	P00 to P03, P10 to P17, P20 to P27, P30 to P37, RESET			–3	μA
	I_{LIL2}		X1, X2, XT1/P04, XT2			–20	μA
	I_{LIL3}		P70 to P74			–3 Note 4	μA
	I_{LIL4}		P100 to P107, P110 to P117, P120 to P127			–10	μA
High-level input leakage current	I_{LOH1}	V_{OUT} = V_{DD}	P01 to P03, P10 to P17, P20 to P27, P30 to P37, P80 to P87, P90 to P97, P100 to P107, P110 to P117, P120 to P127, FIP0 to FIP12			3	μA
	I_{LOH2}	V_{OUT} = 15 V	P70 to P74			80	μA
Low-level output leakage current	I_{LOL1}	V_{OUT} = 0 V	P01 to P03, P10 to P17, P20 to P27, P30 to P37, P70 to P74			–3	μA
	I_{LOL2}	V_{OUT} = V_{LOAD} = V_{DD} – 40 V	P80 to P87, P90 to P97, P100 to P107, P110 to P117, P120 to P127, FIP0 to FIP12			–10	μA
Display output current	I_{OD}	V_{DD} = 4.5 to 5.5 V, V_{OD} = V_{DD} – 2 V		–15	–18		mA
Software pull-up resistor	R_1	V_{IN} = 0 V, P01 to P03, P10 to P17, P20 to P27, P30 to P37	V_{DD} = 4.5 to 5.5 V	15	40	90	kΩ
				20		500	kΩ
On-chip pull-down resistor	R_2	FIP0 to FIP12	V_{OD} – V_{LOAD} = 40 V	25	70	135	kΩ
Power supply current Note 1	I_{DD1}	5.0 MHz crystal oscillation operation mode	V_{DD} = 5.0 V ±10 % Note 2		10.0	30.0	mA
			V_{DD} = 3.0 V ±10 % Note 3		1.1	3.3	mA
	I_{DD2}	5.0 MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ±10 %		1.6	4.8	mA
			V_{DD} = 3.0 V ±10 %		0.65	1.95	mA
	I_{DD3}	32.768 kHz crystal oscillation operation mode	V_{DD} = 5.0 V ±10 %		135	270	μA
			V_{DD} = 3.0 V ±10 %		95	190	μA
	I_{DD4}	32.768 kHz crystal oscillation HALT mode	V_{DD} = 5.0 V ±10 %		25	55	μA
			V_{DD} = 3.0 V ±10 %		5	15	μA
	I_{DD5}	XT1 = 0 V STOP mode when connecting to feedback resistor	V_{DD} = 5.0 V ±10 %		1	30	μA
			V_{DD} = 3.0 V ±10 %		0.5	10	μA
	I_{DD6}	XT1 = 0 V STOP mode when not connecting to feedback resistor	V_{DD} = 5.0 V ±10 %		0.1	30	μA
			V_{DD} = 3.0 V ±10 %		0.05	10	μA

Notes 1. This current excludes the AV_{REF} current, port current, and current which flows in the on-chip pull-down resistor.

2. When operating at high-speed mode (when the processor clock control register (PCC) is set to 00H)

3. When operating at low-speed mode (when the PCC is set to 04H)

4. For P70 to P74, a low-level input leakage current of –200 μA (MAX.) flows only during the 1.5 clocks (no-wait time) after an instruction has been executed to read out port 7 (P7) or port mode register 7 (PM7). Outside the period of 1.5 clocks following executing a read-out instruction, the current is –3 μA (MAX.).

Remark Unless otherwise specified, shared pin characteristics are the same as port pin characteristics.

AC CHARACTERISTICS

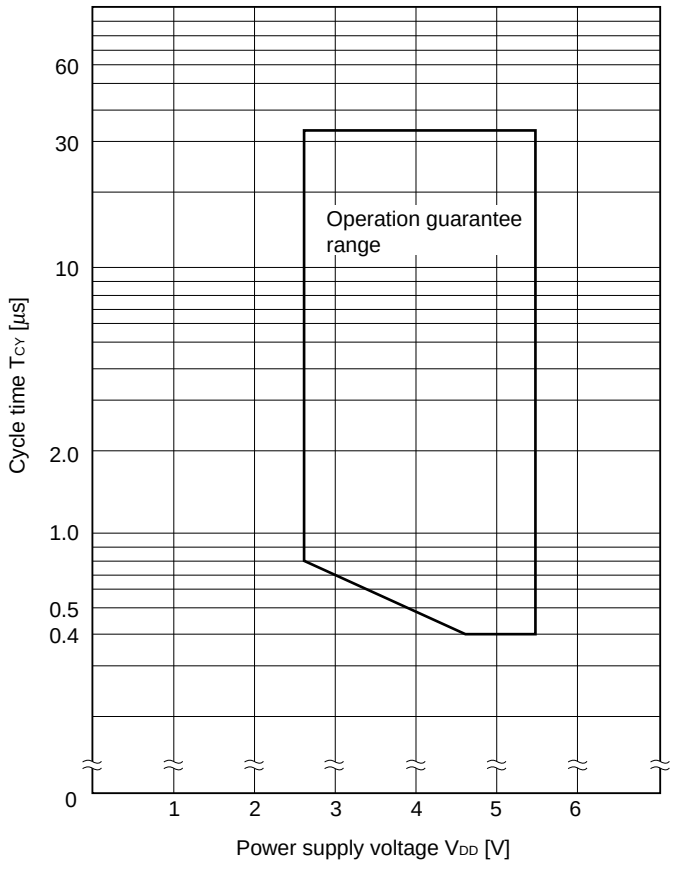
(1) Basic operation (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Cycle time (minimum) instruction execution time)	T_{CY}	Operated with main system clock	V_{DD} = 4.5 to 5.5 V	0.4		32	μs
				0.8		32	μs
		Operated with subsystem clock		40 Note 1	122	125	μs
TI1, TI2 input frequency	f_{TI}	V_{DD} = 4.5 to 5.5 V		0		2	MHz
				0		138	kHz
TI1, TI2 input high, low-level width	f_{TIH} f_{TIL}	V_{DD} = 4.5 to 5.5 V		250			ns
				3.6			μs
Interrupt input high, low-level width	f_{INTH} f_{INTL}	INTP0		$8/f_{sam}$ Note 2			μs
		INTP1 to INTP3		10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

Notes 1. Value when external clock input is used as subsystem clock. When a crystal is used, the value becomes 114 μs.

2. Selection of $f_{sam} = fx/2^{N+1}$, fx/64, fx/128 is available (N = 0 to 4) by bits 0 and 1 (SCS0, SCS1) of sampling clock select register (SCS).

T_{CY} vs V_{DD} (with main system clock operated)



(2) Serial interface (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

(a) Serial interface channel 0

(i) 3-wire serial I/O mode ($\overline{SCK0}$: Internal clock output)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK0}$ high, low-level width	t_{KH1}, t_{KL1}	V_{DD} = 4.5 to 5.5 V	$t_{KCY2}/2 – 50$			ns
			$t_{KCY2}/2 – 100$			ns
SI0 setup time to $\overline{SCK0}$↑	t_{SIK1}	V_{DD} = 4.5 to 5.5 V	100			ns
			150			ns
SI0 hold time from $\overline{SCK0}$↑	t_{KSI1}		400			ns
$\overline{SCK0}$↓→ SO0 output delay time	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is a load capacitance of the $\overline{SCK0}$ or SO0 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$: External clock input)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK0}$ high, low-level width	t_{KH2}, t_{KL2}	V_{DD} = 4.5 to 5.5 V	$t_{KCY2}/2 – 50$			ns
			$t_{KCY2}/2 – 100$			ns
SI0 setup time to $\overline{SCK0}$↑	t_{SIK2}	V_{DD} = 4.5 to 5.5 V	100			ns
			150			ns
SI0 hold time from $\overline{SCK0}$↑	t_{KSI2}		400			ns
$\overline{SCK0}$↓→ SO0 output delay time	t_{KSO2}	C = 100 pF[Note]			300	ns
$\overline{SCK0}$ rise, fail time	t_{R2}, t_{F2}				160	ns

Note C is a load capacitance of the SO0 output line.

(iii) SBI mode ($\overline{SCK0}$: Internal clock output)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
$\overline{SCK0}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 5.5 V		800			ns
				3200			ns
$\overline{SCK0}$ high, low-level width	t_{KH3}	V_{DD} = 4.5 to 5.5 V		$t_{KCY3}/2 - 50$			ns
	t_{KL3}			$t_{KCY3}/2 - 150$			ns
SB0, SB1 setup time to $\overline{SCK0}\infty$	t_{SIK3}	V_{DD} = 4.5 to 5.5 V		100			ns
				300			ns
SB0, SB1 hold time from $\overline{SCK0}\infty$	t_{KSI3}			$t_{KCY3}/2$			ns
$\overline{SCK0}\downarrow\rightarrow$ SB0, SB1 output delay time	t_{KSO3}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V	0		250	ns
				0		1000	ns
$\overline{SCK0}\infty\rightarrow$SB0, SB1↓	t_{KSB}			t_{KCY3}			ns
SB0, SB1↓$\rightarrow\overline{SCK0}\downarrow$	t_{SBK}			t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY3}			ns

Note R is a load resistance of the $\overline{SCK0}$, SB0, or SB1 output line, and C is its load capacitance.

(iv) SBI mode ($\overline{SCK0}$: External clock input)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
$\overline{SCK0}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 5.5 V		800			ns
				3200			ns
$\overline{SCK0}$ high, low-level width	t_{KH4}	V_{DD} = 4.5 to 5.5 V		400			ns
	t_{KL4}			1600			ns
SB0, SB1 setup time to $\overline{SCK0}\infty$	t_{SIK4}	V_{DD} = 4.5 to 5.5 V		100			ns
				300			ns
SB0, SB1 hold time from $\overline{SCK0}\infty$	t_{KSI4}			$t_{KCY4}/2$			ns
$\overline{SCK0}\downarrow\rightarrow$ SB0, SB1 output delay time	t_{KSO4}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V	0		250	ns
				0		1000	ns
$\overline{SCK0}\infty\rightarrow$SB0, SB1↓	t_{KSB}			t_{KCY4}			ns
SB0, SB1↓$\rightarrow\overline{SCK0}\downarrow$	t_{SBK}			t_{KCY4}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY4}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY4}			ns
$\overline{SCK0}$ rise, fall time	t_{R4} t_{F4}					160	ns

Note R is a load resistance of the SB0 or SB1 output line, and C is its load capacitance.

(v) 2-wire serial I/O mode ($\overline{SCK0}$: Internal clock output)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
$\overline{SCK0}$ cycle time	t_{KCY5}		1600			ns
$\overline{SCK0}$ high-level width	t_{KH5}		$t_{KCY5}/2 - 160$			ns
$\overline{SCK0}$ low-level width	t_{KL5}	V_{DD} = 4.5 to 5.5 V	$t_{KCY5}/2 - 50$			ns
			$t_{KCY5}/2 - 100$			ns
SB0, SB1 setup time to $\overline{SCK0}\infty$	t_{SIK5}	V_{DD} = 4.5 to 5.5 V	300			ns
			350			ns
SB0, SB1 hold time from $\overline{SCK0}\infty$	t_{KSI5}		600			ns
$\overline{SCK0}\downarrow\rightarrow$SB0, SB1 output delay time	t_{KSO5}	R = 1 kΩ, C = 100 pF[Note]	0		300	ns

Note R is a load resistance of the $\overline{SCK0}$, SB0, or SB1 output line, and C is its load capacitance.

(vi) 2-wire serial I/O mode ($\overline{SCK0}$: External clock input)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
$\overline{SCK0}$ cycle time	t_{KCY6}			1600			ns
$\overline{SCK0}$ high-level width	t_{KH6}			650			ns
$\overline{SCK0}$ low-level width	t_{KL6}			800			ns
SB0, SB1 setup time to $\overline{SCK0}\infty$	t_{SIK6}			100			ns
SB0, SB1 hold time from $\overline{SCK0}\infty$	t_{KSI6}			$t_{KCY6}/2$			ns
$\overline{SCK0}\downarrow\rightarrow$SB0, SB1 output delay time	t_{KSO6}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V	0		300	ns
				0		500	ns
$\overline{SCK0}$ rise, fall time	t_{R6} t_{F6}					160	ns

Note R is a load resistance of the SB0 or SB1 output line, and C is its load capacitance.

(b) Serial interface channel 1

(i) 3-wire serial I/O mode ($\overline{SCK1}$: Internal clock output)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY7}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK1}$ high, low-level width	t_{KH7}	V_{DD} = 4.5 to 5.5 V	$t_{KCY7}/2 - 50$			ns
	t_{KL7}		$t_{KCY7}/2 - 100$			ns
SI1 setup time to $\overline{SCK1}\infty$	t_{SIK7}	V_{DD} = 4.5 to 5.5 V	100			ns
			150			ns
SI1 hold time from $\overline{SCK1}\infty$	t_{KSI7}		400			ns
$\overline{SCK1}\downarrow\rightarrow$ SO1 output delay time	t_{KSO7}	C = 100 pF**Note**			300	ns

Note C is a load capacitance of the $\overline{SCK1}$ or SO1 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK1}$: External clock input)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY8}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK1}$ high, low-level width	t_{KH8}	V_{DD} = 4.5 to 5.5 V	$t_{KCY8}/2 - 50$			ns
	t_{KL8}		$t_{KCY8}/2 - 100$			ns
SI1 setup time to $\overline{SCK1}\infty$	t_{SIK8}	V_{DD} = 4.5 to 5.5 V	100			ns
			150			ns
SI1 hold time from $\overline{SCK1}\infty$	t_{KSI8}		400			ns
$\overline{SCK1}\downarrow\rightarrow$ SO1 output delay time	t_{KSO8}	C = 100 pF**Note**			300	ns
$\overline{SCK1}$ rise, fall time	t_{R8} t_{F8}				160	ns

Note C is a load capacitance of the SO1 output line.

(iii) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$: Internal clock output)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY9}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK1}$ high, low-level width	t_{KH9}	V_{DD} = 4.5 to 5.5 V	$t_{KCY9}/2 - 50$			ns
	t_{KL9}		$t_{KCY9}/2 - 100$			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK9}	V_{DD} = 4.5 to 5.5 V	100			ns
			150			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI9}		400			ns
SO1 output delay time from $\overline{SCK1}\downarrow$	t_{KSO9}	C = 100 pF[Note]			300	ns
STB↑ from $\overline{SCK1}\downarrow$	t_{SBD}		$t_{KCY9}/2 - 100$		$t_{KCY9}/2 + 100$	ns
Strobe signal high-level width	t_{SBW}		$t_{KCY9} - 30$		$t_{KCY9} + 30$	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}		100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}	V_{DD} = 4.5 to 5.5 V	100			ns
			150			ns
$\overline{SCK1}\downarrow$ from busy inactive	t_{SPS}				$2t_{KCY9}$	ns

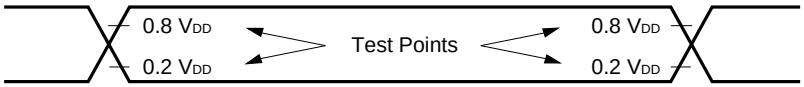
Note C is a load capacitance of the SO1 output line.

(iv) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$: External clock input)

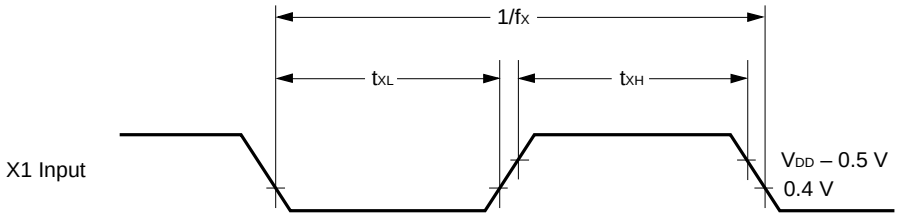
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY10}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK1}$ high, low-level width	t_{KH10}	V_{DD} = 4.5 to 5.5 V	400			ns
	t_{KL10}		800			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK10}		100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI10}		400			ns
SO1 output delay time from $\overline{SCK1}\downarrow$	t_{KSO10}	C = 100 pF[Note]			300	ns
$\overline{SCK1}$ rise, fall time	t_{R10}				160	ns
	t_{F10}					

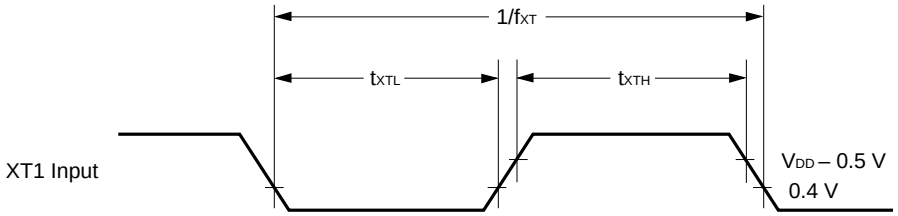
Note C is a load capacitance of the SO1 output line.

AC Timing Test Point (Excluding X1, XT1 Input)

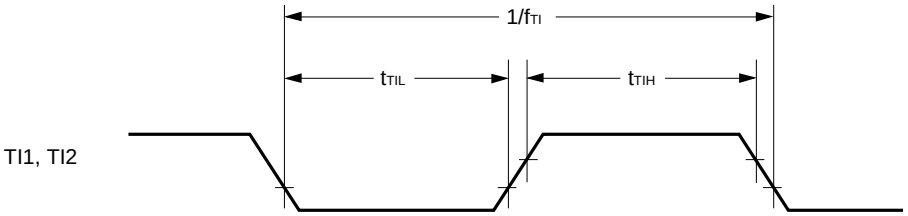


Clock Timing



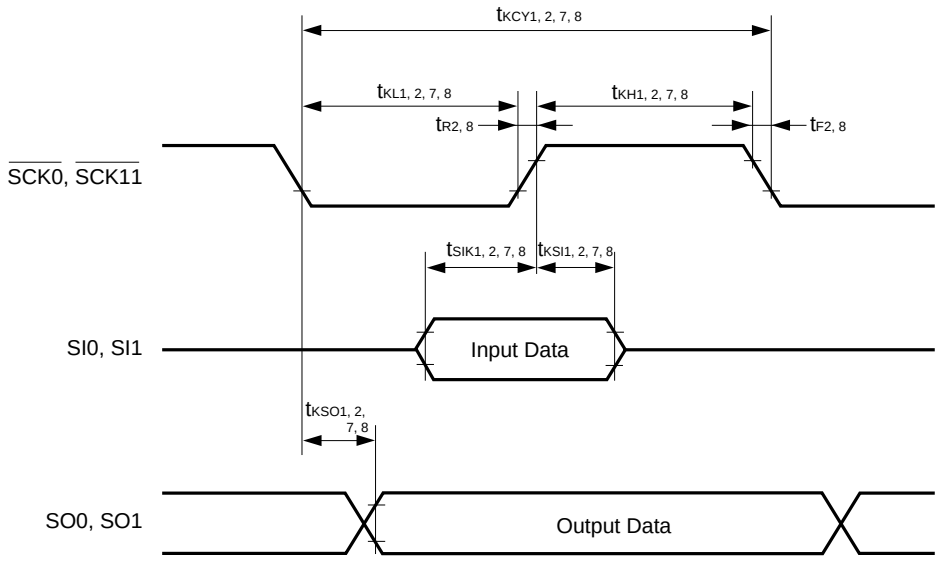


TI Timing

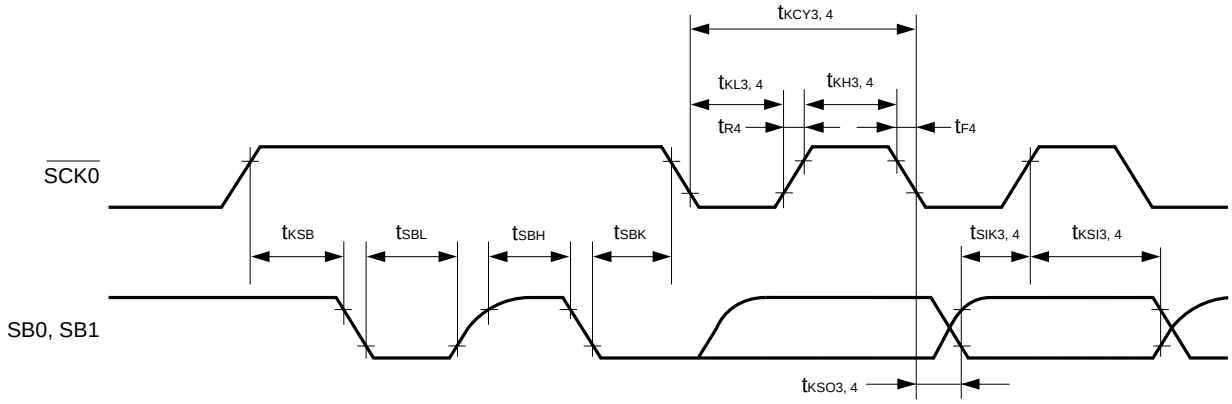


Serial Transfer Timing

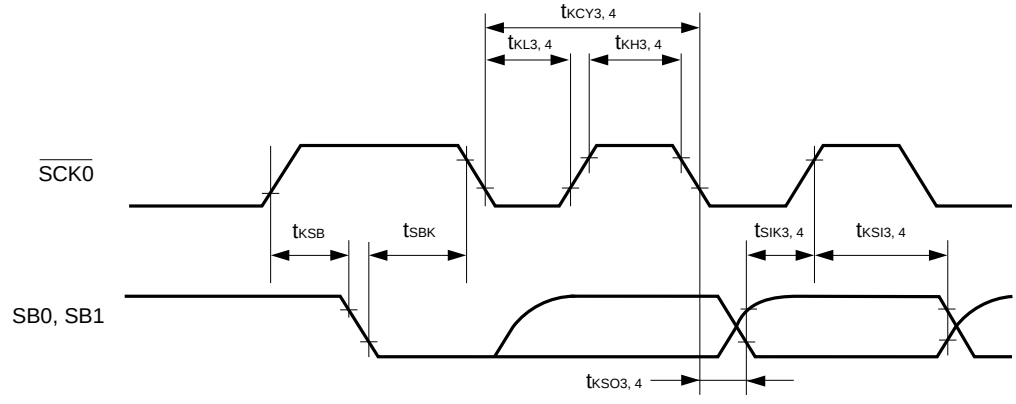
3-wire serial I/O mode:



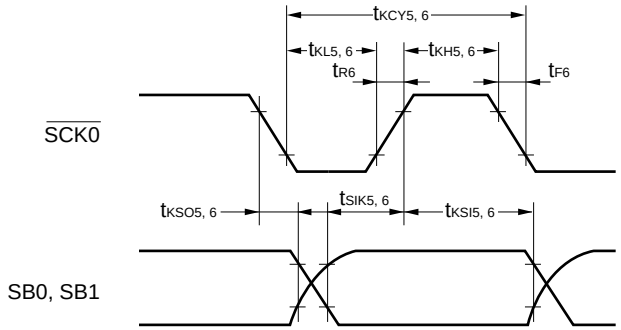
SBI mode (bus release signal transfer):



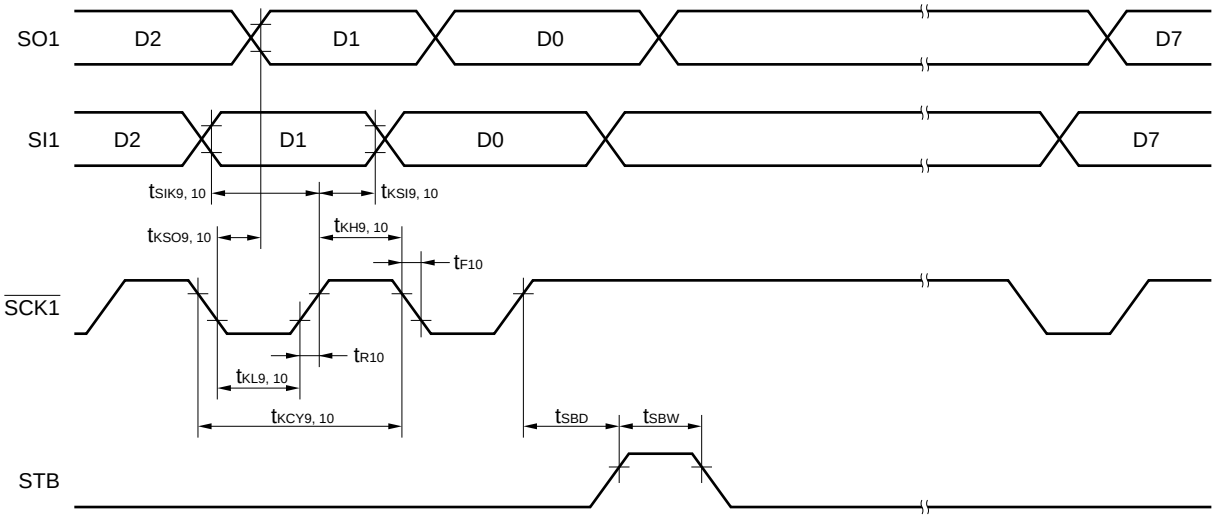
SBI mode (command signal transfer):



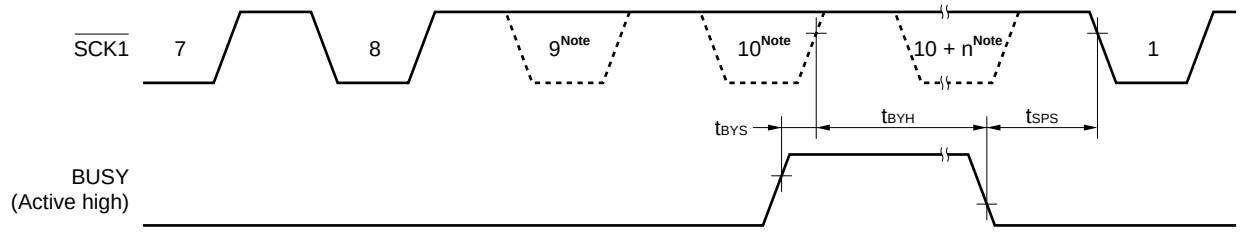
2-wire serail I/O mode:



3-wire serial I/O mode with automatic transmit/receive function:



3-wire serial I/O mode with automatic transmit/receive function (busy processing):



Note Though it does not become low level actually, here described as it does due to the timing rule.

A/D CONVERTER CHARACTERISTICS (T_A = –40 to +85 °C, AV_{DD} = V_{DD} = 4.0 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution			8	8	8	bit
Total error[Note 1]					0.6	%
Conversion time[Note 2]	t_{CONV}	1 MHz - fx - 5.0 MHz	19.1		200	μs
Sampling time[Note 3]	t_{SAMP}		24/f_X			μs
Analog signal input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
Reference voltage	AV_{REF}		4.0		AV_{DD}	V
AV_{REF} resistor	R_{AIREF}		4	14		kΩ

Notes 1. Quantization error (±1/2LSB) is not included. This parameter is indicated as the ratio to the full-scale value.

2. Set the A/D conversion time to 19.1 μs or more.

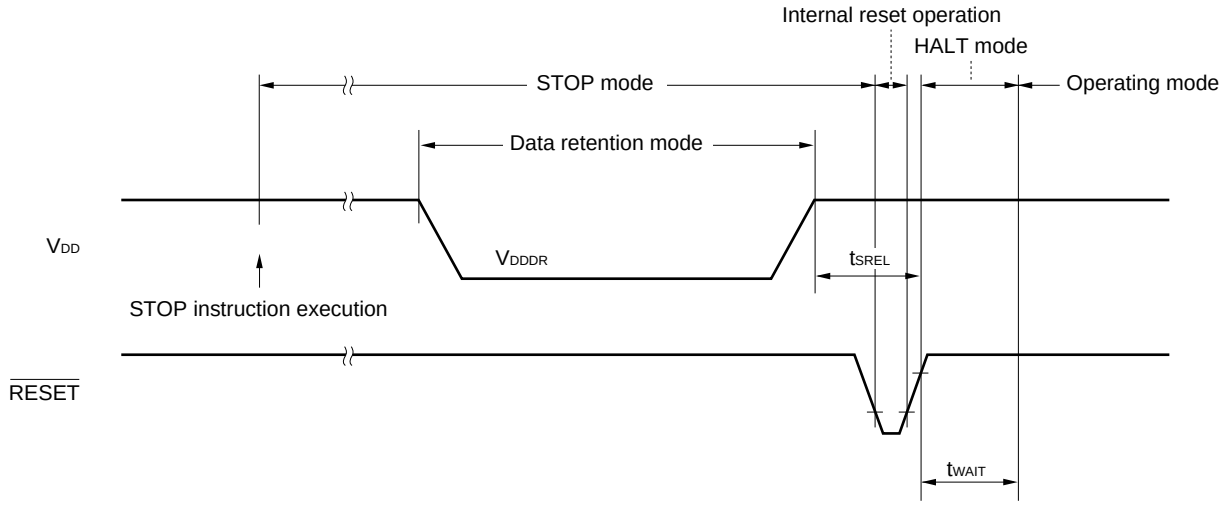
3. Sampling time depends on the conversion time.

DATA RETENTION CHARACTERISTICS AT LOW SUPPLY VOLTAGE IN DATA MEMORY STOP MODE (T_A = –40 to +85 °C)

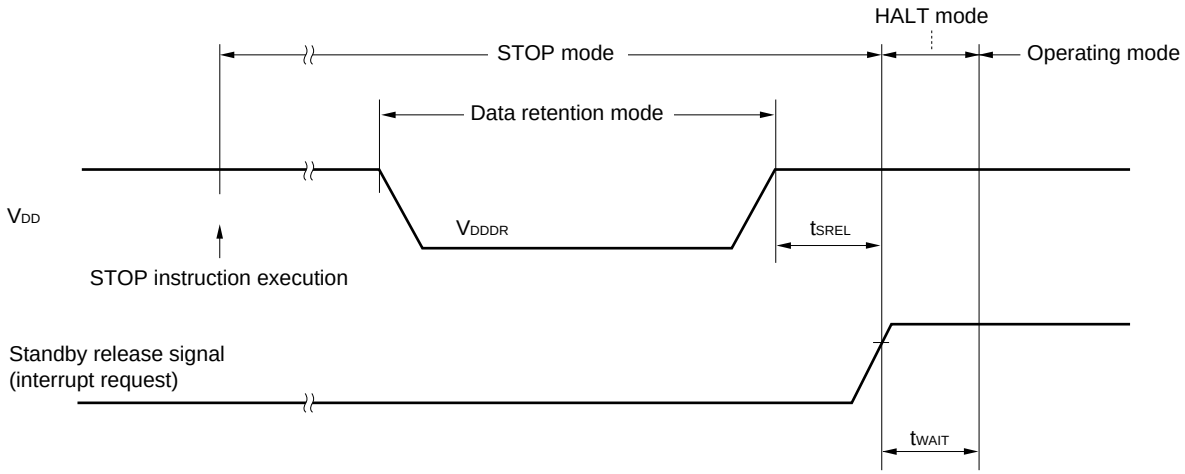
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data retention supply voltage	V_{DDDR}		1.8		5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 2.0 V Subsystem clock stopped, Feedback resistor non-connected		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation settling time	t_{WAIT}	Release by $\overline{\text{RESET}}$		2^{17}/fx		ms
		Release by interrupt		**Note**		ms

Note Selection of 2^{12}/fx, 2^{14}/fx to 2^{17}/fx is available by bits 0 to 2 (OSTS0 to OSTS2) of oscillation settling time select register (OSTS).

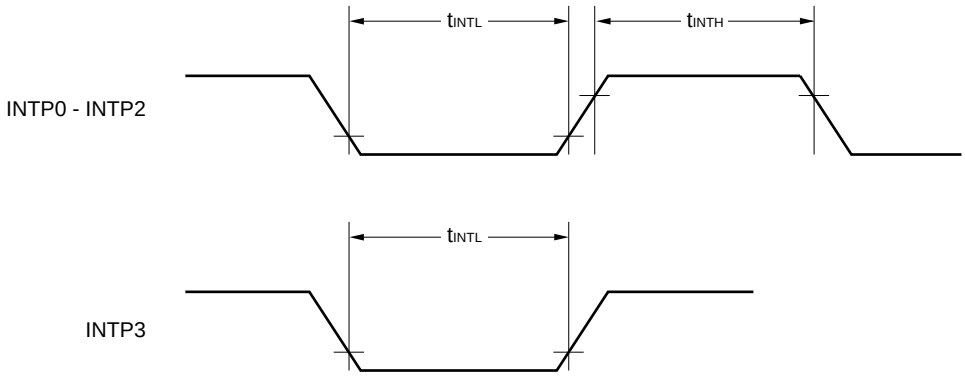
Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



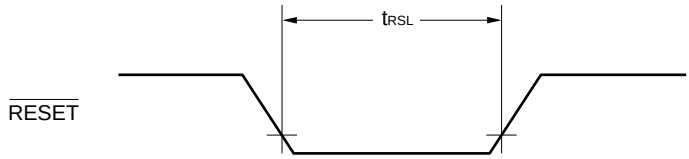
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



PROM PROGRAMMING CHARACTERISTICS

DC Characteristics

(1) PROM write mode (T_A = 25 ±5 °C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Symbol[Note]	Conditions	Min.	Typ.	Max.	Unit
Input voltage high	V_{IH}	V_{IH}		$0.7V_{DD}$		V_{DD}	V
Input voltage low	V_{IL}	V_{IL}		0		$0.3V_{DD}$	V
Output voltage high	V_{OH}	V_{OH}	I_{OH} = –1 mA	V_{DD} – 1.0			V
Output voltage low	V_{OL}	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input leakage current	I_{LI}	I_{LI}	$0 \le V_{IN} \le V_{DD}$	–10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		12.2	12.5	12.8	V
V_{DD} supply voltage	V_{DD}	V_{CC}		6.25	6.5	6.75	V
V_{PP} supply current	I_{PP}	I_{PP}	$\overline{PGM} = V_{IL}$			50	mA
V_{DD} supply current	I_{DD}	I_{CC}				50	mA

(2) PROM read mode (T_A = 25 ±5 °C, V_{DD} = 5.0 ±0.5 V, V_{PP} = V_{DD} ±0.6 V)

Parameter	Symbol	Symbol[Note]	Conditions	Min.	Typ.	Max.	Unit
Input voltage high	V_{IH}	V_{IH}		$0.7V_{DD}$		V_{DD}	V
Input voltage low	V_{IL}	V_{IL}		0		$0.3V_{DD}$	V
Output voltage high	V_{OH1}	V_{OH1}	I_{OH} = –1 mA	V_{DD} – 1.0			V
	V_{OH2}	V_{OH2}	I_{OH} = –100 μA	V_{DD} – 0.5			V
Output voltage low	V_{OL}	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input leakage current	I_{LI}	I_{LI}	$0 \le V_{IN} \le V_{DD}$	–10		+10	μA
Output leakage current	I_{LO}	I_{LO}	$0 \le V_{OUT} \le V_{DD}$, $\overline{OE} = V_{IH}$	–10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		V_{DD} – 0.6	V_{DD}	V_{DD} + 0.6	V
V_{DD} supply voltage	V_{DD}	V_{CC}		4.5	5.0	5.5	V
V_{PP} supply current	I_{PP}	I_{PP}	$V_{PP} = V_{DD}$			100	μA
V_{DD} supply current	I_{DD}	I_{CCA1}	$\overline{CE} = V_{IL}$, $V_{IN} = V_{IH}$			50	mA

Note Corresponding μPD27C1001A symbol

AC Characteristics

(1) PROM write mode

(a) Page program mode (T_A = 25 ±5 °C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Symbol[Note]	Conditions	Min.	Typ.	Max.	Unit
Address setup time (to $\overline{OE}\downarrow$)	t_{AS}	t_{AS}		2			μs
$\overline{OE}$ setup time	t_{OES}	t_{OES}		2			μs
$\overline{CE}$ setup time (to $\overline{OE}\downarrow$)	t_{CES}	t_{CES}		2			μs
Input data setup time (to $\overline{OE}\downarrow$)	t_{DS}	t_{DS}		2			μs
Address hold time (from $\overline{OE}\infty$)	t_{AH}	t_{AH}		2			μs
	t_{AHL}	t_{AHL}		2			μs
	t_{AHV}	t_{AHV}		0			μs
Input data hold time (from $\overline{OE}\infty$)	t_{DH}	t_{DH}		2			μs
Data output float delay time from $\overline{OE}\infty$	t_{DF}	t_{DF}		0		250	ns
V_{PP} setup time (to $\overline{OE}\downarrow$)	t_{VPS}	t_{VPS}		1.0			ms
V_{DD} setup time (to $\overline{OE}\downarrow$)	t_{VDS}	t_{VCS}		1.0			ms
Program pulse width	t_{PW}	t_{PW}		0.095	0.1	0.105	ms
Valid data delay time from $\overline{OE}\downarrow$	t_{OE}	t_{OE}				1	μs
$\overline{OE}$ pulse width during data latching	t_{LW}	t_{LW}		1			μs
$\overline{PGM}$ setup time	t_{PGMS}	t_{PGMS}		2			μs
$\overline{CE}$ hold time	t_{CEH}	t_{CEH}		2			μs
$\overline{OE}$ hold time	t_{OEH}	t_{OEH}		2			μs

(b) Byte program mode (T_A = 25 ±5 °C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Symbol[Note]	Conditions	Min.	Typ.	Max.	Unit
Address setup time (to $\overline{PGM}\downarrow$)	t_{AS}	t_{AS}		2			μs
$\overline{OE}$ setup time	t_{OES}	t_{OES}		2			μs
$\overline{CE}$ setup time (to $\overline{PGM}\downarrow$)	t_{CES}	t_{CES}		2			μs
Input data setup time (to $\overline{PGM}\downarrow$)	t_{DS}	t_{DS}		2			μs
Address hold time (from $\overline{OE}\infty$)	t_{AH}	t_{AH}		2			μs
Input data hold time (from $\overline{PGM}\infty$)	t_{DH}	t_{DH}		2			μs
Data output float delay time from $\overline{OE}\infty$	t_{DF}	t_{DF}		0		250	ns
V_{PP} setup time (to $\overline{PGM}\downarrow$)	t_{VPS}	t_{VPS}		1.0			ms
V_{DD} setup time (to $\overline{PGM}\downarrow$)	t_{VDS}	t_{VCS}		1.0			ms
Program pulse width	t_{PW}	t_{PW}		0.095		0.105	ms
Valid data delay time from $\overline{OE}\downarrow$	t_{OE}	t_{OE}				1	μs
$\overline{OE}$ hold time	t_{OEH}	—		2			μs

Note Corresponding μPD27C1001A symbol

(2) PROM read mode (T_A = 25 ±5 °C, V_{DD} = 5.0 ±0.5 V, V_{PP} = V_{DD} ±0.6 V)

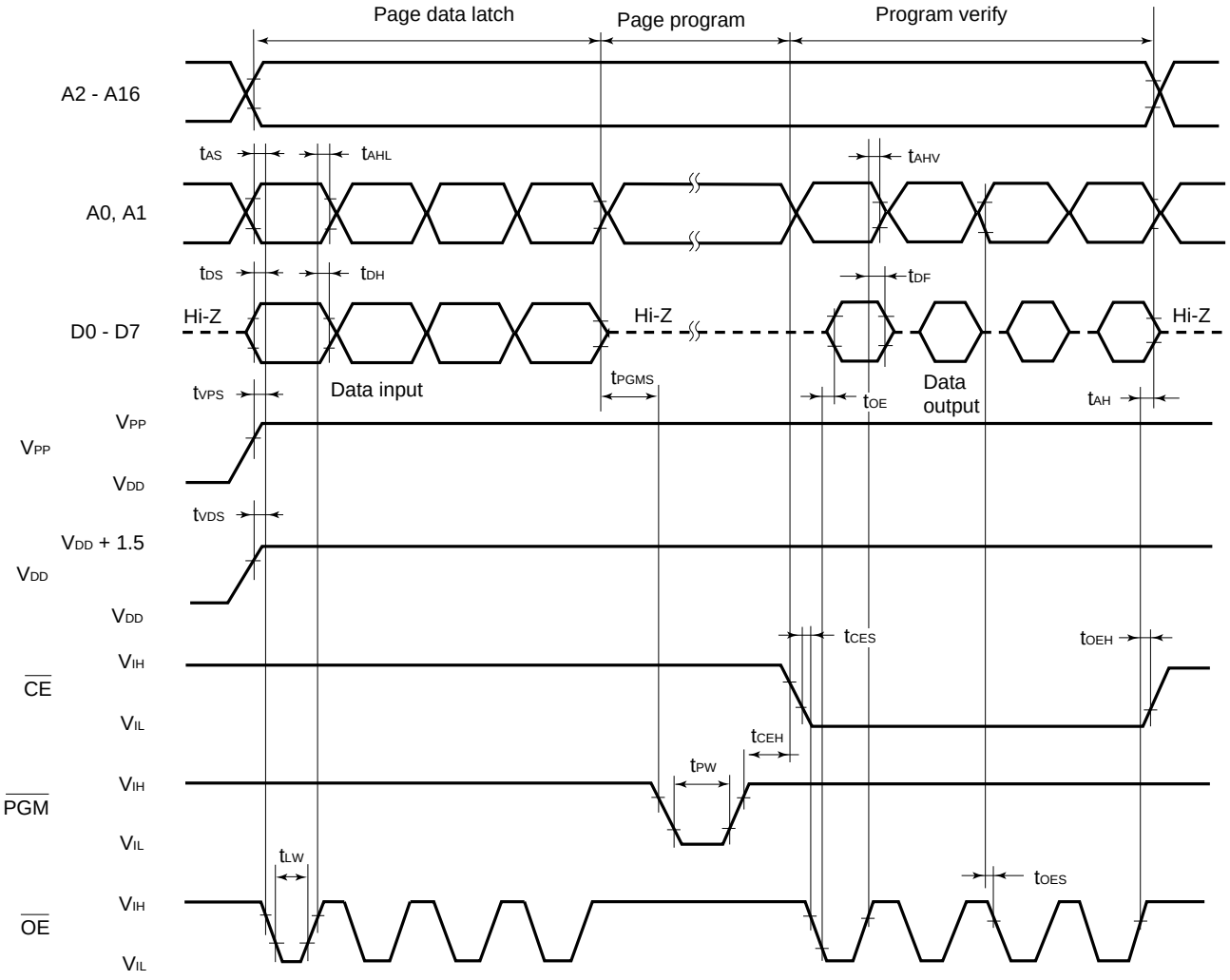
Parameter	Symbol	Symbol[Note]	Conditions	Min.	Typ.	Max.	Unit
Data output delay time from address	t_{ACC}	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}			800	ns
Data output delay time from $\overline{CE}$↓	t_{CE}	t_{CE}	$\overline{OE}$ = V_{IL}			800	ns
Data output delay time from $\overline{OE}$↓	t_{OE}	t_{OE}	$\overline{CE}$ = V_{IL}			200	ns
Data output float delay time from $\overline{OE}$∞	t_{DF}	t_{DF}	$\overline{CE}$ = V_{IL}	0		60	ns
Data hold time from address	t_{OH}	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0			ns

Note Corresponding μPD27C1001A symbol

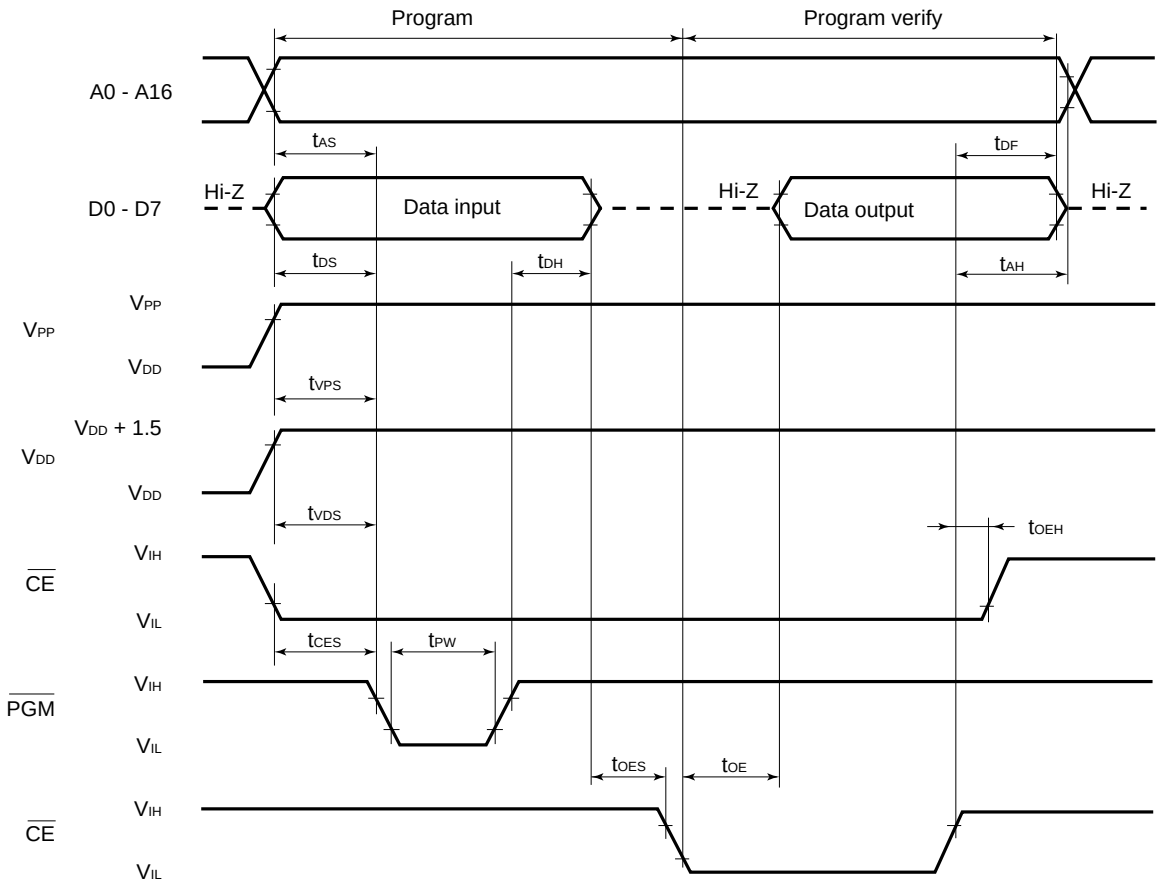
(3) PROM programming mode setting (T_A = 25 °C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
PROM programming mode setup time	t_{SMA}		10			μs

PROM Write Mode Timing (Page Program Mode)



PROM Write Mode Timing (Byte Program Mode)

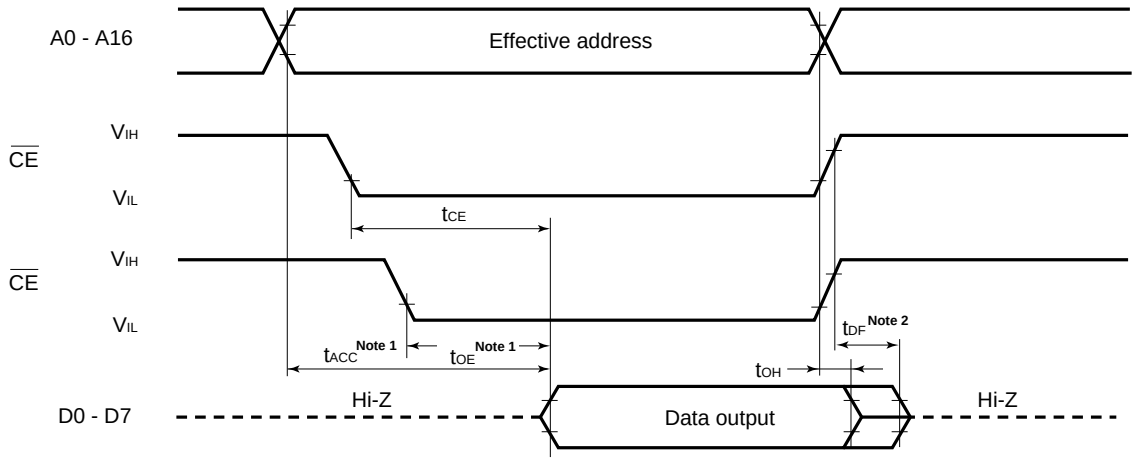


Cautions 1. V_{DD} should be applied before V_{PP}, and cut after V_{PP}.

2. V_{PP} should not exceed +13.5 V including overshoot.

3. Disconnection during application of +12.5V to V_{PP} may have an adverse effect on reliability.

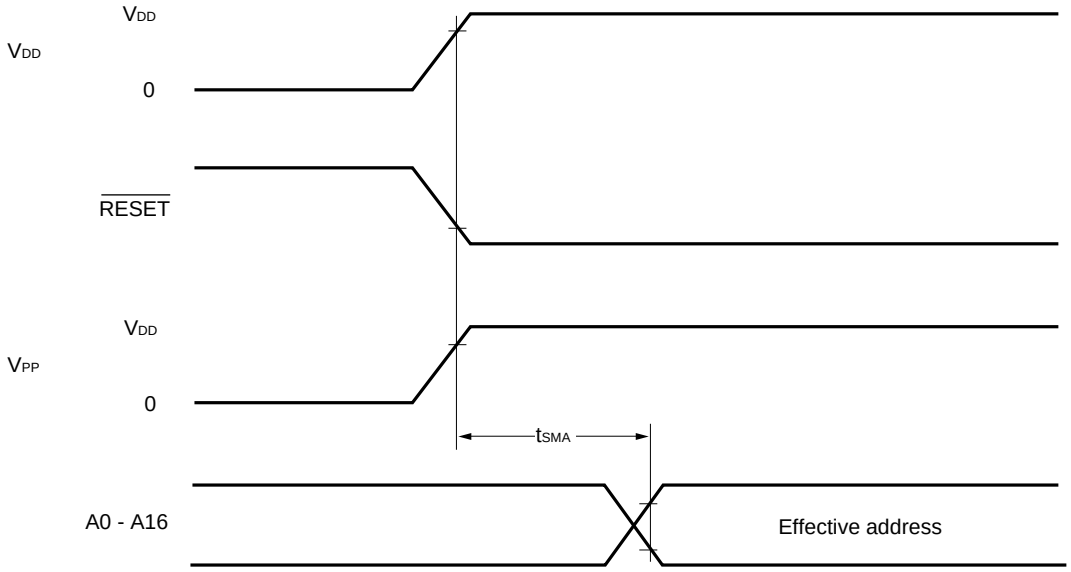
PROM Read Mode Timing



Notes 1. If you want to read within the t_{ACC} range, make the $\overline{OE}$ input delay time from the fall of $\overline{CE}$ a maximum of $t_{ACC} - t_{OE}$.

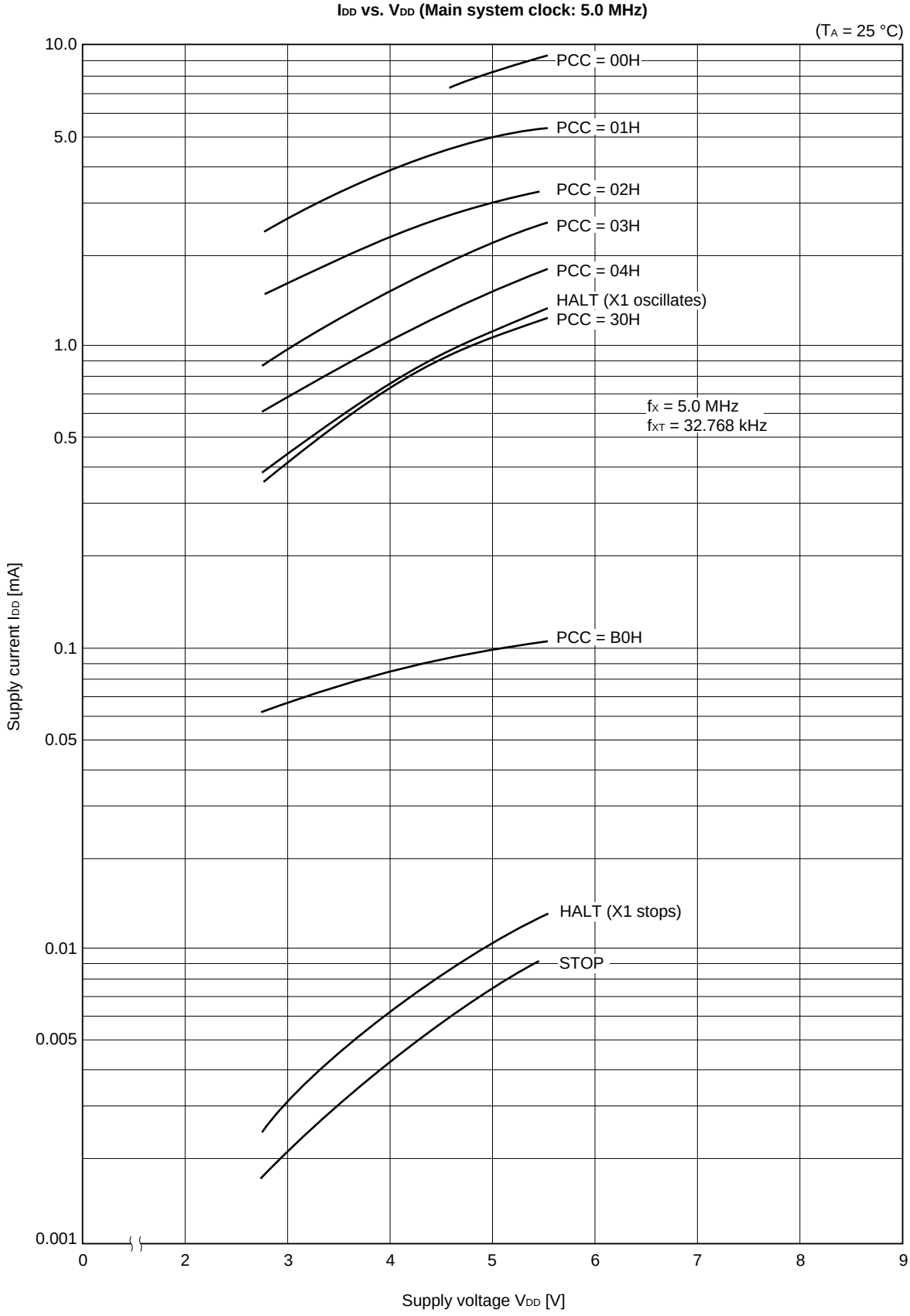
2. t_{DF} is the time from when either $\overline{OE}$ or $\overline{CE}$ first reaches V_{IH}.

PROM Programming Mode Setting Timing



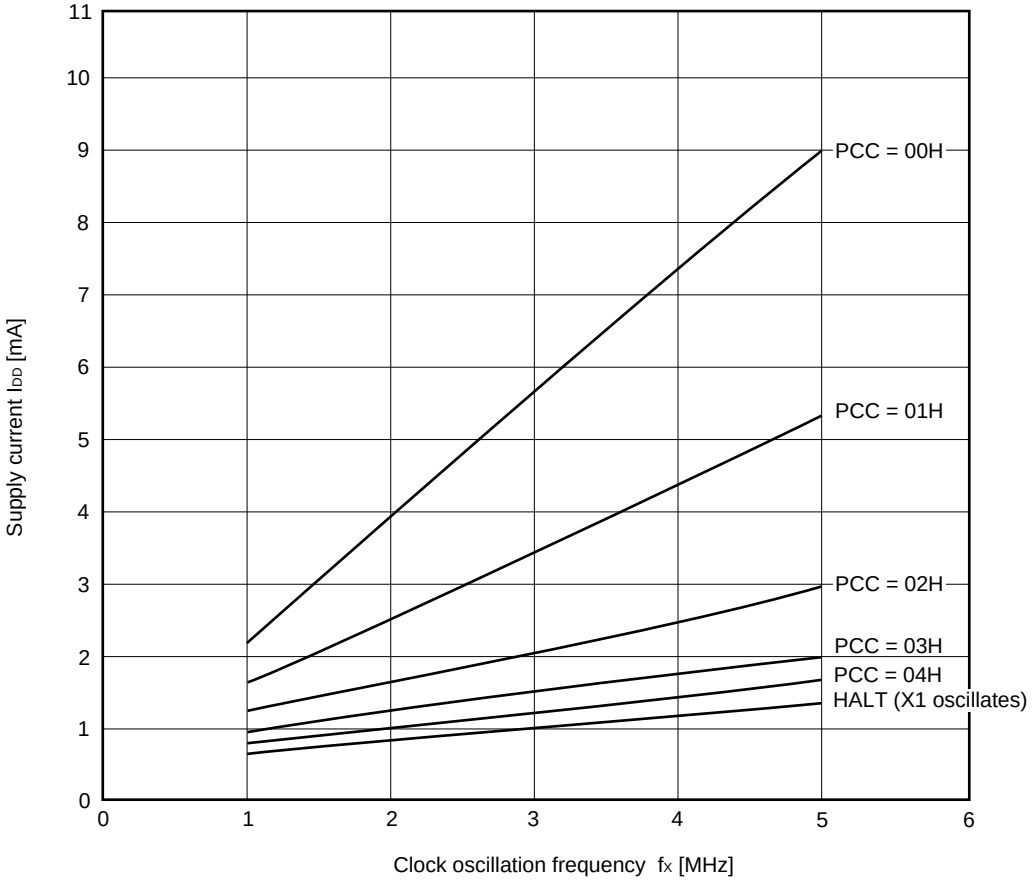
10. CHARACTERISTIC CURVE (REFERENCE VALUE) ★

I_{DD} vs. V_{DD} (Main system clock: 5.0 MHz)

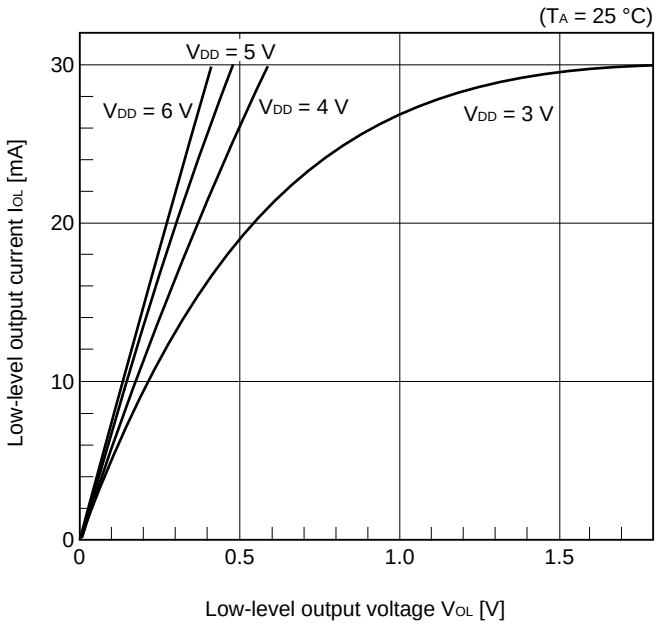


I_{DD} vs. f_X

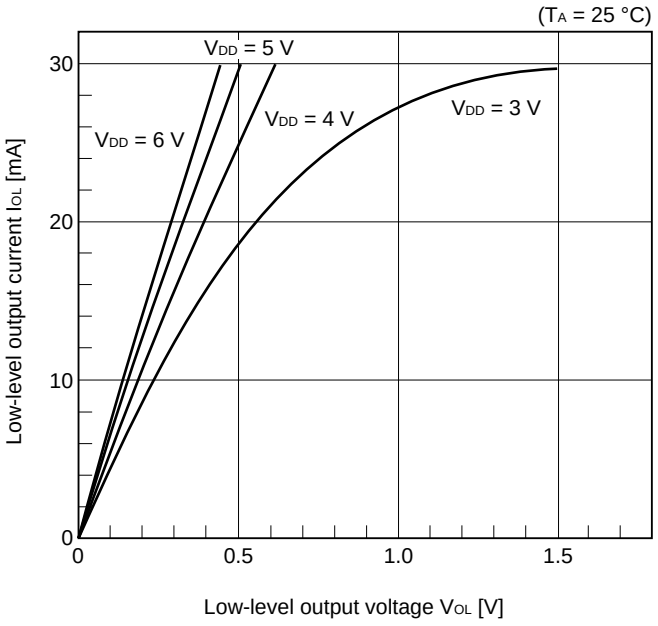
(V_{DD} = 5 V, T_A = 25 °C)



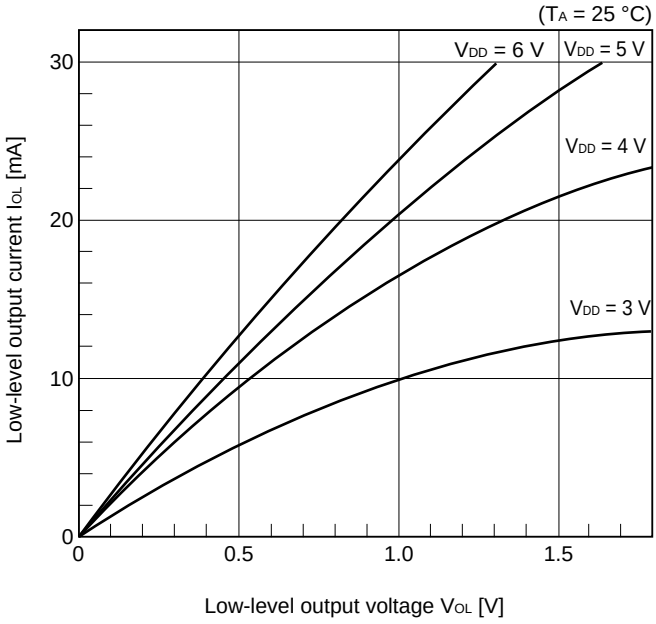
V_{OL} vs. I_{OL} (Port 1)



V_{OL} vs. I_{OL} (Ports 0, 2, 3)

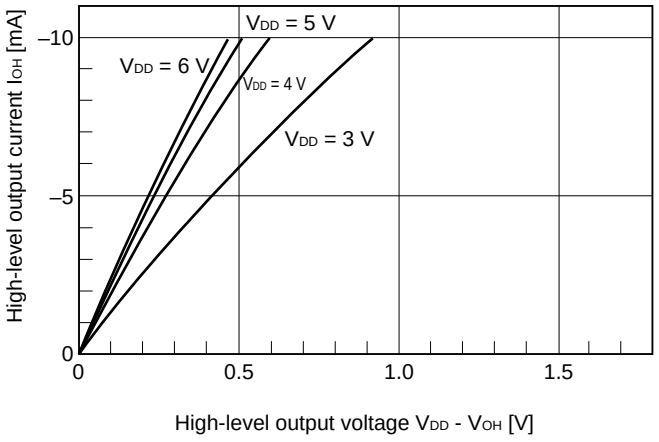


V_{OL} vs. I_{OL} (Port 7)



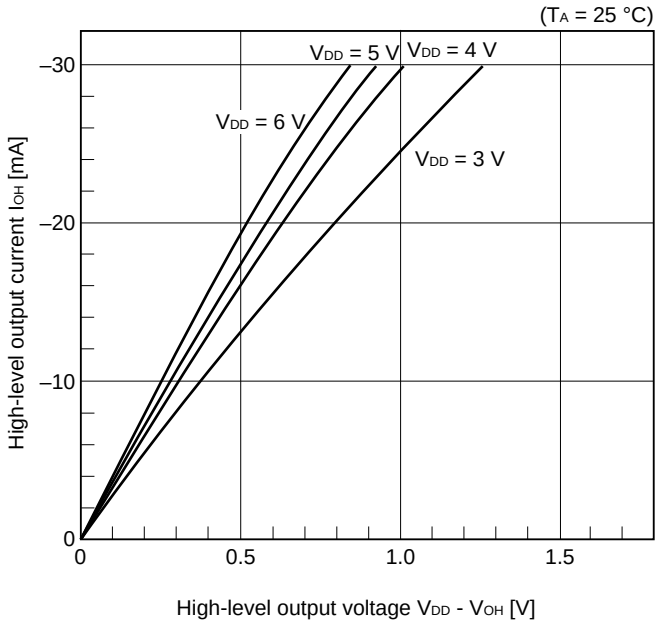
V_{DD} - V_{OH} vs. I_{OH} (Port 0 - Port 3)

(T_A = 25 °C)



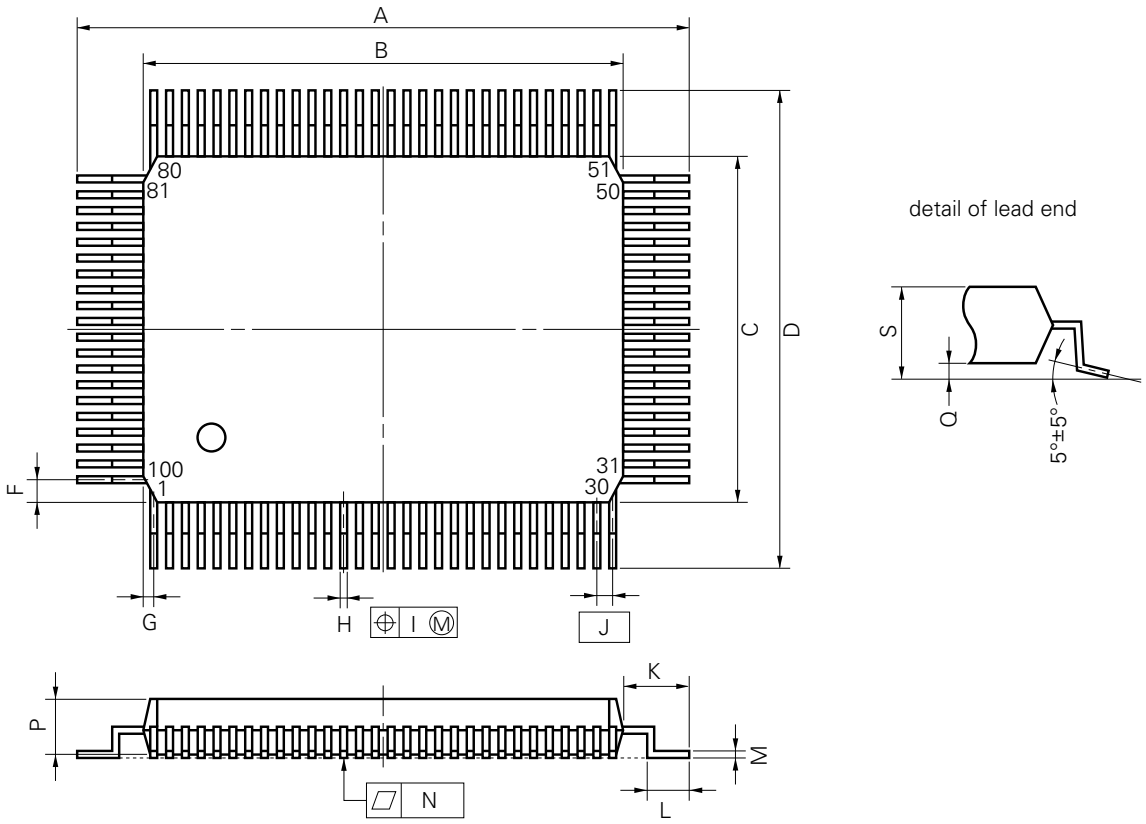
V_{DD} - V_{OH} vs. I_{OH} (Port 8 - Port 12)

(T_A = 25 °C)



11. PACKAGE DRAWINGS

100 PIN PLASTIC QFP (14 × 20)



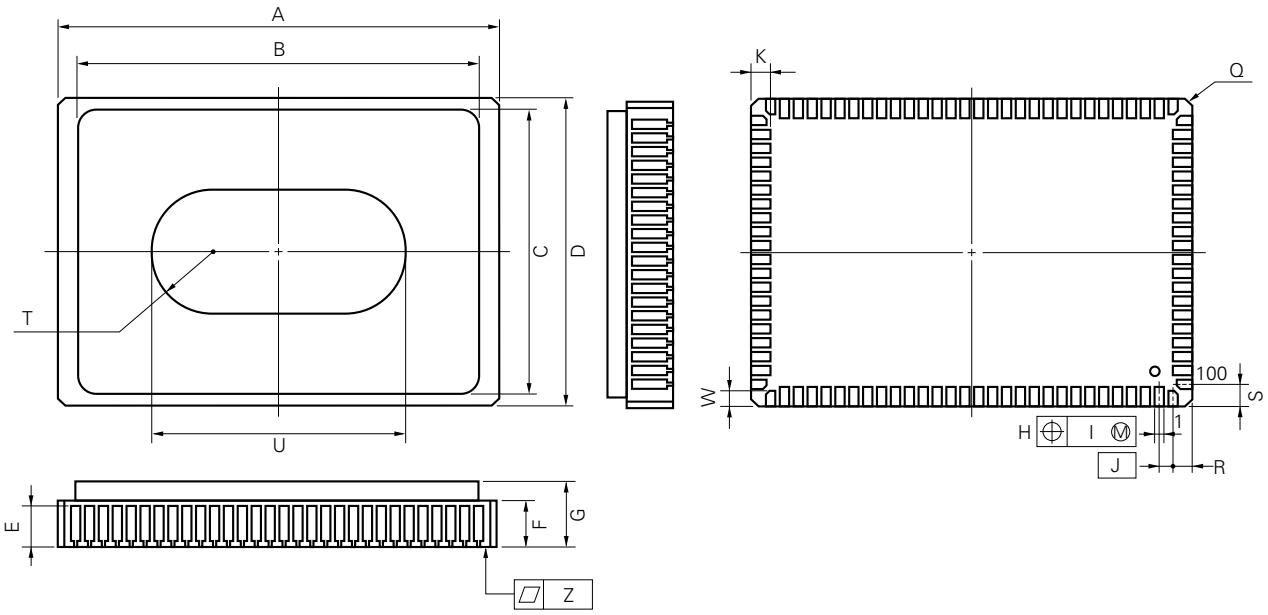
P100GF-65-3BA1-2

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

100 PIN CERAMIC WQFN



X100KW-65A-1

NOTE

Each lead centerline is located within 0.06 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	20.6±0.4	0.811±0.016
B	19.0	0.748
C	13.8	0.543
D	14.6±0.4	0.575±0.016
E	1.94	0.076
F	2.14	0.084
G	3.5 MAX,	0.138 MAX.
H	0.45±0.10	$0.018^{+0.004}_{-0.005}$
I	0.06	0.003
J	0.65	0.026
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
Q	C 0.3	C 0.012
R	0.875	0.034
S	1.125	0.044
T	R 3.17	R 0.125
U	12.0	0.472
W	0.75±0.2	$0.030^{+0.008}_{-0.009}$
Z	0.10	0.004

★ 12. RECOMMENDED SOLDERING CONDITIONS

The conditions listed below shall be met when soldering the μPD78P0208.

For details of the recommended soldering conditions, refer to our document *Semiconductor Device Mounting Technology Manual* (C10535E).

Please consult with our sales offices in case any other soldering process is used, or in case soldering is done under different conditions.

Table 12-1 Soldering Conditions for Surface-Mount Devices

μPD78P0208GF-3BA: 100-pin plastic QFP (14 × 20 mm)

Soldering process	Soldering conditions	Recommended conditions
Infrared ray reflow	Peak package's surface temperature: 235 °C Reflow time: 30 seconds or less (210 °C or more) Maximum allowable number of reflow processes: 2	IR35-00-2
VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or less (200 °C or more) Maximum allowable number of reflow processes: 2	VP15-00-2
Wave soldering	Solder temperature: 260 °C or less Flow time: 10 seconds or less Number of flow processes: 1 Preheating temperature : 120 °C max. (measured on the package surface)	WS60-00-1
Partial heating method	Terminal temperature: 300 °C or less Heat time: 3 seconds or less (for one side of a device)	–

Caution Do not apply two or more different soldering methods to one chip (except for partial heating method for terminal sections).

APPENDIX A DEVELOPMENT TOOLS

The following tools are available for development of systems using the μPD78P0208.

Language processing software

RA78K/0 **Notes 1, 2, 3, 4**	Assembler package common to 78K/0 series
CC78K/0 **Notes 1, 2, 3, 4**	C compiler package common to 78K/0 series
DF780208 **Notes 1, 2, 3, 4**	Device file for μPD780208 subseries
CC78K/0-L **Notes 1, 2, 3, 4**	C compiler library source file common to 78K/0 series

PROM writing tools

PG-1500	PROM programmer
PA-78P0208GF PA-78P0208KL-T	Programmer adapter connected to PG-1500
PG-1500 controller **Notes 1, 2**	Control program for PG-1500

Debugging tools

IE-78000-R	In-circuit emulator common to 78K/0 series	
IE-78000-R-A **Note 8**	In-circuit emulator common to 78K/0 series (for integrated debugger)	★
IE-78000-R-BK	Break board common to 78K/0 series	
IE-780208-R-EM	Emulation board for evaluating μPD780208 subseries	
EP-78064GF-R	Emulation probe common to μPD78064 subseries	
EV-9200GF-100	Socket mounted on target system created for 100-pin plastic QFP	
SM78K0 **Notes 5, 6, 7**	System simulator common to 78K/0 series	
ID78K0 **Notes 4, 5, 6, 7, 8**	Integrated debugger for IE-78000-R-A	★
SD78K/0 **Notes 1, 2**	Screen debugger for IE-78000-R	
DF780208 **Notes 1, 2, 5, 6, 7**	Device file for μPD780208 subseries	

Real-time OS

RX78K/0 **Notes 1, 2, 3, 4**	Real-time OS for 78K/0 series
MX78K0 **Notes 1, 2, 3, 4**	OS for 78K/0 series

Notes 1. PC-9800 series (MS-DOS™) based
2. IBM PC/AT™ and compatible (PC DOS™/IBM DOS™/MS-DOS) based
3. HP9000 series 300™ (HP-UX™) based
4. HP9000 series 700™ (HP-UX) based, SPARCstation™ (Sun OS™) based, EWS-4800 series (EWS-UX/V) based
5. PC-9800 series (MS-DOS + Windows™) based
6. IBM PC/AT and compatible (PC DOS/IBM DOS/MS-DOS + Windows) based
7. NEWS™ (NEWS-OS™) based ★
8. Under development

Remarks 1. Please refer to the *78K/0 Series Selection Guide* (U11126E) for information on third party development tools.
2. RA78K/0, CC78K/0, SD78K/0, ID78K0 and SM78K0 are used in combination with DF780208.

Fuzzy inference development support system

FE9000Note 1/FE9200Note 3	Fuzzy knowledge data creation tool
FT9080Note 1/FT9085Note 2	Translator
FI78K0Notes 1, 2	Fuzzy inference module
FD78K0Notes 1, 2	Fuzzy inference debugger

Notes 1. PC-9800 series (MS-DOS) based

2. IBM PC/AT and compatible (PC DOS/IBM DOS/MS-DOS) based

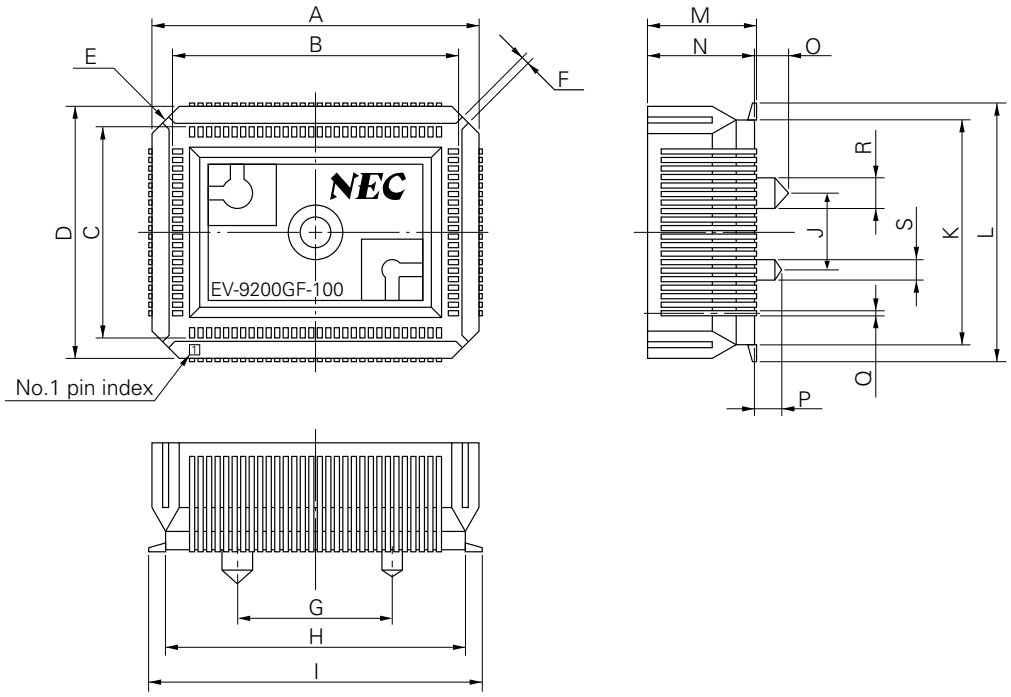
3. IBM PC/AT and compatible (PC DOS/IBM DOS/MS-DOS + Windows) based

Remark Please refer to the *78K/0 Series Selection Guide* (U11126E) for information on third party development tools.

Conversion socket (EV-9200GF-100) package drawings and recommended pattern to mount the socket

Fig. A-1 Package Drawings of EV-9200GF-100 (Reference) (Unit: mm)

Based on EV-9200GF-100
(1) Package drawing (in mm)

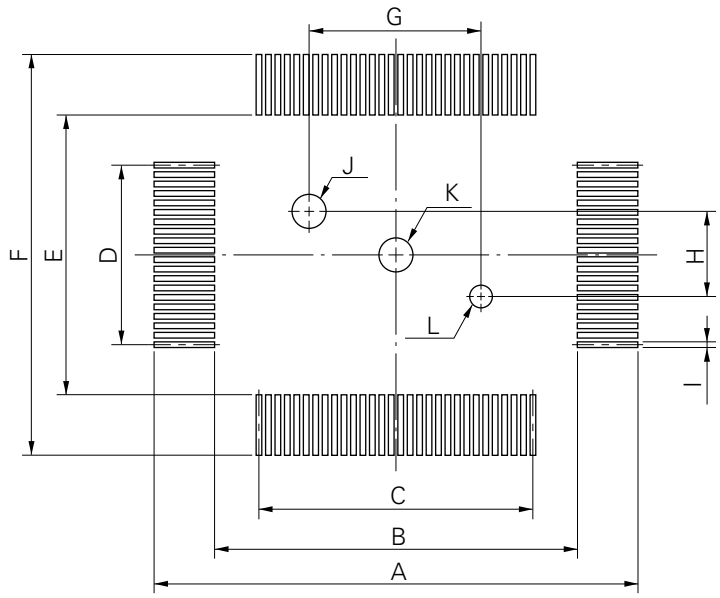


EV-9200GF-100-G0

ITEM	MILLIMETERS	INCHES
A	24.6	0.969
B	21	0.827
C	15	0.591
D	18.6	0.732
E	4-C 2	4-C 0.079
F	0.8	0.031
G	12.0	0.472
H	22.6	0.89
I	25.3	0.996
J	6.0	0.236
K	16.6	0.654
L	19.3	076
M	8.2	0.323
N	8.0	0.315
O	2.5	0.098
P	2.0	0.079
Q	0.35	0.014
R	φ2.3	φ0.091
S	φ1.5	φ0.059

Fig. A-2 Recommended Pattern to Mount EV-9200GF-100 on a Substrate (Reference) (Unit: mm)

Based on EV-9200GF-100
(2) Pad drawing (in mm)



EV-9200GF-100-P0

ITEM	MILLIMETERS	INCHES
A	26.3	1.035
B	21.6	0.85
C	$0.65\pm0.02\times29=18.85\pm0.05$	$0.026^{+0.001}_{-0.002}\times1.142=0.742^{+0.002}_{-0.002}$
D	$0.65\pm0.02\times19=12.35\pm0.05$	$0.026^{+0.001}_{-0.002}\times0.748=0.486^{+0.003}_{-0.002}$
E	15.6	0.614
F	20.3	0.799
G	12 ± 0.05	$0.472^{+0.003}_{-0.002}$
H	6 ± 0.05	$0.236^{+0.003}_{-0.002}$
I	0.35 ± 0.02	$0.014^{+0.001}_{-0.001}$
J	$\phi2.36\pm0.03$	$\phi0.093^{+0.001}_{-0.002}$
K	$\phi2.3$	$\phi0.091$
L	$\phi1.57\pm0.03$	$\phi0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

APPENDIX B RELATED DOCUMENTS

Documents related to devices

Document name	Document No.	
	Japanese	English
μPD780208 Subseries User's Manual	IEU-885	IEU-1413
μPD780204, 780205, 780206, 780208 Data Sheet	U10436J	U10436E ★
78K/0 Series User's Manual, Instruction	IEU-849	IEU-1372
78K/0 Series Instruction Set	U10903J	—
78K/0 Series Instruction Summary Sheet	U10904J	—
μPD780208 Subseries Special Function Registers Table	U10997J	—
78K/0 Series Application Note, Basic (II)	U10121J	U10121E

Documents related to development tools (user's manual)

Document name		Document No.	
		Japanese	English
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
CC78K/0 C Compiler Application Note	Programming Know-How	EEA-618	EEA-1208 ★
CC78K Series Library Source File		EEU-777	—
PG-1500 PROM Programmer		EEU-651	EEU-1335
PG-1500 Controller, PC-9800 Series (MS-DOS) Base		EEU-704	EEU-1291
PG-1500 Controller, IBM PC/AT (PC DOS) Base		EEU-5008	U10540E
IE-78000-R		EEU-810	EEU-1398
IE-78000-R-A		U10057J	U10057E ★
IE-78000-R-BK		EEU-867	EEU-1427
IE-780208-R-EM		EEU-977	EEU-1501
EP-78064		EEU-934	EEU-1469
SM78K0 System Simulator	Reference	EEU-5002	U10181E
SM78K Series System Simulator	External Parts User-Open Interface Specification	U10092J	U10092E ★
SD78K/0 Screen Debugger	Introduction	EEU-852	U10539E
PC-9800 Series (MS-DOS) Base	Reference	EEU-816	—
SD78K/0 Screen Debugger	Introduction	EEU-5024	EEU-1414
IBM PC/AT (PC DOS) Base	Reference	U11279J	EEU-1413

Caution The above documents may be revised without notice. Use the latest versions when you design an application system

Documents related to embedded software (user's manual)

Document name		Document No.	
		Japanese	English
78K/0 Series Real-time OS	Fundamental	EEU-912	—
	Installation	EEU-911	—
	Technical	EEU-913	—
★ 78K/0 Series OS MX78K0	Fundamental	EEU-5010	—
Tool for Creating Fuzzy Knowledge Data		EEU-829	EEU-1438
78K/0, 78K/II, and 87AD Series Fuzzy Inference Development Support System, Translator		EEU-862	EEU-1444
78K/0 Series Fuzzy Inference Development Support System, Fuzzy Inference Module		EEU-858	EEU-1441
78K/0 Series Fuzzy Inference Development Support System, Fuzzy Inference Debugger		EEU-921	EEU-1458

Other documents

Document name	Document No.	
	Japanese	English
Package Manual	IEI-635	IEI-1213
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Device	IEI-620	IEI-1209
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Electrostatic Discharge (ESD) Test	MEM-539	—
Guide to Quality Assurance for Semiconductor Device	MEI-603	MEI-1202
Guide for Products Related to Micro-Computer: Other Companies	MEI-604	—

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Cautions on CMOS Devices

☒ Countermeasures against static electricity for all MOSs

Caution When handling MOS devices, take care so that they are not electrostatically charged.

Strong static electricity may cause dielectric breakdown in gates. When transporting or storing MOS devices, use conductive trays, magazine cases, shock absorbers, or metal cases that NEC uses for packaging and shipping. Be sure to ground MOS devices during assembling. Do not allow MOS devices to stand on plastic plates or do not touch pins.

Also handle boards on which MOS devices are mounted in the same way.

☒ CMOS-specific handling of unused input pins

Caution Hold CMOS devices at a fixed input level.

Unlike bipolar or NMOS devices, if a CMOS device is operated with no input, an intermediate-level input may be caused by noise. This allows current to flow in the CMOS device, resulting in a malfunction. Use a pull-up or pull-down resistor to hold a fixed input level. Since unused pins may function as output pins at unexpected times, each unused pin should be separately connected to the V_{DD} or GND pin through a resistor.

If handling of unused pins is documented, follow the instructions in the document.

☒ Statuses of all MOS devices at initialization

Caution The initial status of a MOS device is unpredictable when power is turned on.

Since characteristics of a MOS device are determined by the amount of ions implanted in molecules, the initial status cannot be determined in the manufacture process. NEC has no responsibility for the output statuses of pins, input and output settings, and the contents of registers at power on. However, NEC assures operation after reset and items for mode setting if they are defined.

When you turn on a device having a reset function, be sure to reset the device first.

Some related documents may be preliminary versions. Note that, however, what documents are preliminary is not indicated in this document.

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