PRELIMINARY

VR4122 64-BIT MIPS RISC MICROPROCESSOR

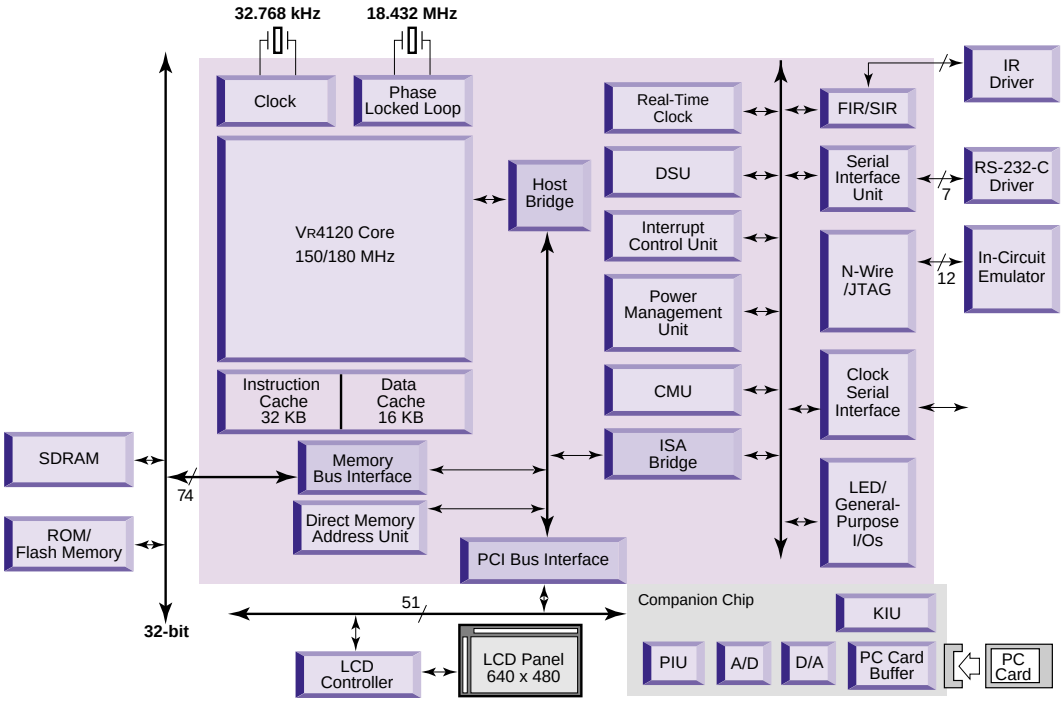
The 64-bit VR4122™ (μPD30122) microprocessor, a member of NEC's VR Series™ microprocessors, is designed especially for high-performance handheld portable computing devices and PCI-based systems such as network terminals, auto PCs, webphotos, and other embedded systems. It uses the MIPS® RISC architecture developed by MIPS Technologies and offers excellent power consumption and performance in a highly integrated, low-cost system on a chip.

The microprocessor uses the ultra-low-power-consuming VR4120™ CPU core based on advanced 0.18-micron technology. The VR4120 CPU has an optimized five-stage pipeline, 32-KB instruction cache, 16-KB data cache, multiply-and-accumulate (MAC) unit, and memory management unit (MMU) that enable high performance in a compact, low-cost chip. The integrated peripherals include a power management unit (PMU), direct memory address (DMA) unit, interrupt control unit, timers, real-time clock, 16550-compatible serial interface, IrDA® interface, and PCI bus controller.

The VR4122 microprocessor is compliant with the MIPS I, II, III instruction set architectures (ISAs) and MIPS16 application-specific extension (ASE). For MIPS16 ASE compliance, the VR4122 incorporates 16-bit instructions with conventional 32-bit instructions to allow compact code size, lower memory, and lower system cost.

The VR4122 microprocessor provides an easy choice for VR4121™ customers in terms of upgrade, since the VR4122 and VR4121 are software compatible. The VR4122 microprocessor's high speed, compact size, and low power consumption make it ideal for use in battery-driven, portable handheld systems.

BLOCK DIAGRAM



FEATURES

VR4120 CPU CORE
— MIPS I, II, III ISA-compliant
— MIPS16 ASE-compliant for compact code density (40% denser code than MIPS32)
— Five-stage pipeline running up to 180 MHz
— Single-cycle 32-bit MAC instruction for DSP operations

MEMORY MANAGEMENT UNIT
— 32-bit physical addressing range of 4 GB with 40-bit virtual address space
— 32 double-entry TLBs supporting 1~256 KB page size
— Up 128-MB SDRAM/EDO/fast-page DRAM and 128-MB SROM/flash memory/mask ROM

CACHE MEMORY UNIT
— 32-KB direct-mapped instruction cache
— 16-KB direct-mapped data cache

BUS CONTROL UNIT
— 32-bit and 16-bit addressing mode
— Dynamic bus sizing to support subset of ISA bus
— PCI bus support

SERIAL INTERFACE UNIT (16550-Compatible)
— RS-232C Compliant
— 1.5-Mbps data transfers
— Separate serial debugging port

PCI BUS INTERFACE UNIT
— Supports 32-bit 33 MHz PCI bus

OTHER
— **Power management unit** with four power-saving modes: full speed, standby, suspend, and hibernate
— **Clock generator unit** with built-in PLL for frequency multiplication
— **Real-time clock** with four built-in timers
— **Interrupt control unit** that supports both internal and external interrupts
— **DMA address unit and DMA control unit** that controls three different types of DMA
— **General-purpose I/O unit** that controls 31 general-purpose I/O pins
— **Fast infrared unit**: 0.5 to 4 Mbps IrDA 1.1 standard communication

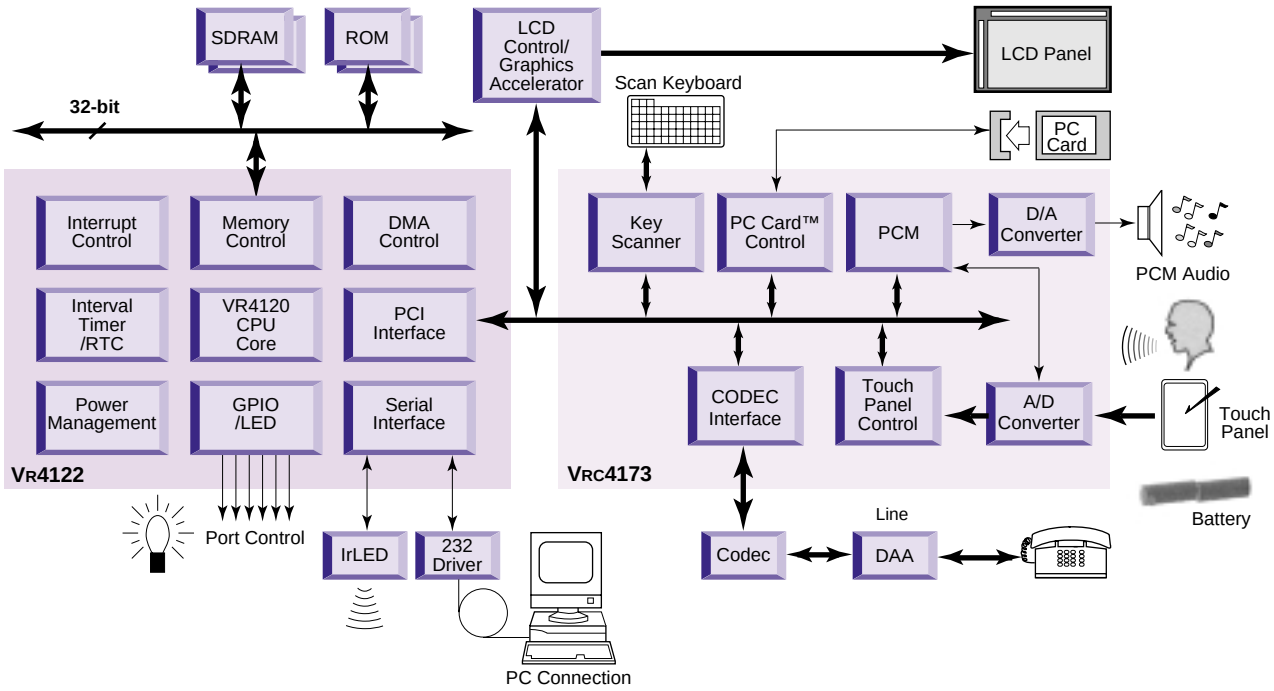
SPECIFICATIONS
— 180 MHz maximum frequency
— 1.8 V (CPU Core) and 3.3 V (I/O) operation
— 270 mW at 180 MHz typical power consumption (target)
— 224-pin FPBGA package (16 x 16 x 1.3 mm)
— 0.18-micron CMOS Process Technology

ORDERING INFORMATION

PART NUMBER	PACKAGE	MAXIMUM OPERATING FREQUENCY
μPD30122F1-150-GA1	224-pin FPBGA	150 MHz
μPD30122F1-180-GA1	224-pin FPBGA	180 MHz

EXAMPLE HANDHELD PC APPLICATION WITH THE VRC4173 COMPANION CHIP

NEC Next-Generation Solution for H/PC



VR4100 FAMILY COMPARISON

	VR4111	VR4121	VR4122
CPU Core	VR4110	VR4120	**VR4120A**
Max. Pipeline Clock	70 MHz	168 MHz	180 MHz
Cache Size	Instruction: 16 KB	Instruction: 16 KB	Instruction: **32 KB**
	Data: 8 KB	Data: 8 KB	Data: **16 KB**
Performance	85 Dhrystone MIPS	210 Dhrystone MIPS	**216** Dhrystone MIPS
Instruction Set	MIPS I, II, III, MIPS16	MIPS I, II, III, MIPS16	MIPS I, II, III, MIPS16
MAC Instruction	Single-cycle,16-bit	Single-cycle, 32-bit	Single-cycle, 32-bit
Operating Voltage	2.5 V (core); 3.3 V (I/O)	2.5 V (core); 3.3 V (I/O)	**1.8 V** (core); 3.3 V (I/O)
Bus Supported	Subset of ISA	Subset of ISA	**PCI**, subset of ISA
Memory Interface	64 MB DRAM	128 MB DRAM	128 MB DRAM
	64 MB ROM	128 MB ROM	128 MB ROM
Power Consumption	185 mW	350 mW	**270 mW**
Package	224-pin FPBGA	224-pin FPBGA	224-pin FPBGA
Temperature Range	–10~70°C	–10~70°C	–10~70°C
Process Technology	0.25-micron UC2 process	0.25-micron UR2 process	**0.18-micron** UC3 process

NEC

For literature, call **1-800-366-9782** 7 a.m. to 6 p.m. Pacific time
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