Standard Products

UT54LVDSC031 Quad Driver

Data Sheet

April 2, 2001

FEATURES

- >155.5 Mbps (77.7 MHz) switching rates
- ±340mV nominal differential signaling
- 5 V power supply
- Cold Spare LVDS outputs
- TTL compatible inputs
- Ultra low power CMOS technology
- 5.0ns maximum, propagation delay
- 3.0ns maximum, differential skew
- Radiation-hardened design; total dose irradiation testing to MIL-STD-883 Method 1019
  - Total-dose: 300 krad(Si)
  - Latchup immune (LET > 111 MeV-cm^2/mg)
- Packaging options:
  - 16-lead flatpack (dual in-line)
- Standard Microcircuit Drawing 5962-95833
  - QML Q and V compliant part
- Compatible with IEEE 1596.3SCI LVDS
- Compatible with ANSI/TIA/EIA 644-1996 LVDS Standard

INTRODUCTION

The UT54LVDSC031 Quad Driver is a quad CMOS differential line driver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 155.5 Mbps (77.7 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The UT54LVDSC031 accepts TTL input levels and translates them to low voltage (340mV) differential output signals. In addition, the driver supports a three-state function that may be used to disable the output stage, disabling the load current, and thus dropping the device to an ultra low idle power state.

The UT54LVDSC031 and companion quad line receiver UT54LVDSC032 provide new alternatives to high power pseudo-ECL devices for high speed point-to-point interface applications.

All LVDS pins have Cold Spare buffers. These buffers will be high impedance when V_{DD} is tied to V_{SS}.

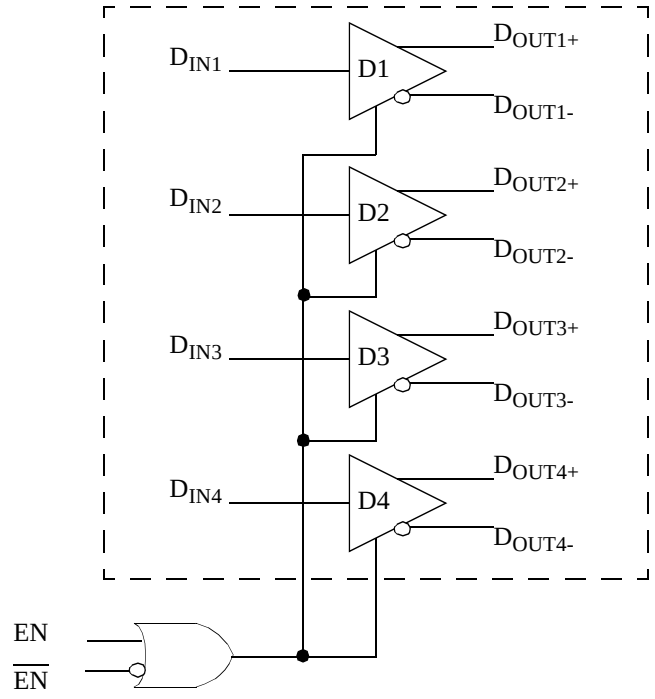


Figure 1. UT54LVDSC031 Quad Driver Block Diagram

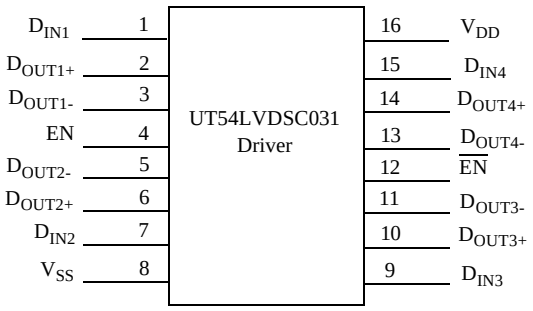


Figure 2. UT54LVDSC031 Pinout

TRUTH TABLE

Enables		Input	Output	
EN	$\overline{EN}$	D_{IN}	D_{OUT+}	D_{OUT-}
L	H	X	Z	Z
All other combinations of ENABLE inputs		L	L	H
		H	H	L

PIN DESCRIPTION

Pin No.	Name	Description
1, 7, 9, 15	D_{IN}	Driver input pin, TTL/CMOS compatible
2, 6, 10, 14	D_{OUT+}	Non-inverting driver output pin, LVDS levels
3, 5, 11, 13	D_{OUT-}	Inverting driver output pin, LVDS levels
4	EN	Active high enable pin, OR-ed with $\overline{EN}$
12	$\overline{EN}$	Active low enable pin, OR-ed with EN
16	V_{DD}	Power supply pin, +5V $\pm$ 10%
8	V_{SS}	Ground pin

APPLICATIONS INFORMATION

The UT54LVDSC031 driver's intended use is primarily in an uncomplicated point-to-point configuration as is shown in Figure 3. This configuration provides a clean signaling environment for quick edge rates of the drivers. The receiver is connected to the driver through a balanced media such as a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media and is located as close to the receiver input pins as possible. The termination resistor converts the current sourced by the driver into voltages that are detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities, as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

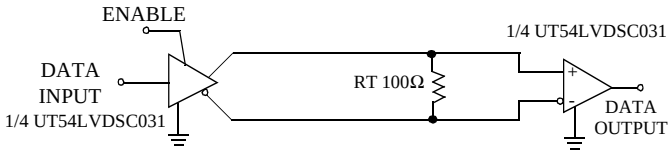
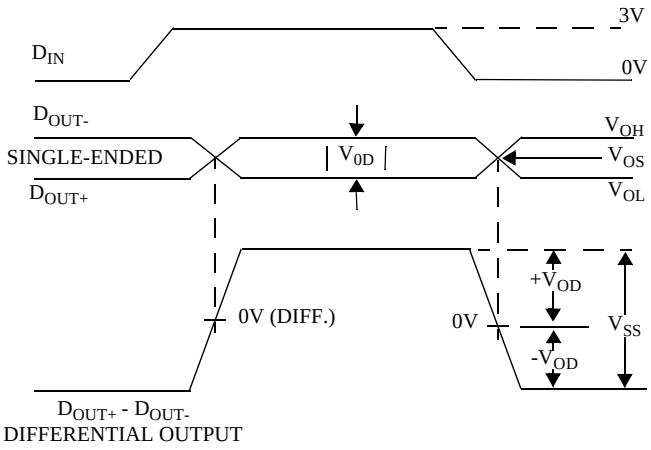


Figure 3. Point-to-Point Application

The UT54LVDSC031 differential line driver is a balanced current source design. A current mode driver, has a high output impedance and supplies a constant current for a range of loads (a voltage mode driver on the other hand supplies a constant voltage for a range of loads). Current is switched through the load in one direction to produce a logic state and in the other direction to produce the other logic state. The current mode **requires** (as discussed above) that a resistive termination be employed to terminate the signal and to complete the loop as shown in Figure 3. AC or unterminated configurations are not allowed. The 3.4mA loop current will develop a differential voltage of 340mV across the 100Ω termination resistor which the receiver detects with a 240mV minimum differential noise margin neglecting resistive line losses (driven signal minus receiver threshold (340mV - 100mV = 240mV)). The signal is centered around +1.2V (Driver Offset, V_{OS}) with respect to ground as shown in Figure 4. **Note:** The steady-state voltage (V_{SS}) peak-to-peak swing is twice the differential voltage (V_{OD}) and is typically 680mV.



Note: The footprint of the UT54LVDSC031 is the same as the industry standard Quad Differential (RS-422) Driver.

Figure 4. Driver Output Levels

The current mode driver provides substantial benefits over voltage mode drivers, such as an RS-422 driver. Its quiescent current remains relatively flat versus switching frequency. Whereas the RS-422 voltage mode driver increases exponentially in most cases between 20 MHz - 50 MHz. This is due to the overlap current that flows between the rails of the device when the internal gates switch. Whereas the current mode driver switches a fixed current between its output without any substantial overlap current. This is similar to some ECL and PECL devices, but without the heavy static I_{CC} requirements of the ECL/PECL design. LVDS requires 80% less current than similar PECL devices. AC specifications for the driver are a tenfold improvement over other existing RS-422 drivers.

The Three-State function allows the driver outputs to be disabled, thus obtaining an even lower power state when the transmission of data is not required.

ABSOLUTE MAXIMUM RATINGS[1]

(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS
V_{DD}	DC supply voltage	-0.3 to 6.0V
$V_{I/O}$	Voltage on any pin	-0.3 to (V_{DD} + 0.3V)
T_{STG}	Storage temperature	-65 to +150°C
P_D	Maximum power dissipation	1.25 W
T_J	Maximum junction temperature[2]	+150°C
Θ_{JC}	Thermal resistance, junction-to-case[3]	10°C/W
I_I	DC input current	±10mA

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Maximum junction temperature may be increased to +175°C during burn-in and steady-static life.
3. Test per MIL-STD-883, Method 1012.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
V_{DD}	Positive supply voltage	4.5 to 5.5V
T_C	Case temperature range	-55 to +125°C
V_{IN}	DC input voltage	0V to V_{DD}

DC ELECTRICAL CHARACTERISTICS[1, 2]

(V_{DD} = 5.0V ±10%; -55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V_{IH}	High-level input voltage	(TTL)	2.0	V_{DD}	V
V_{IL}	Low-level input voltage	(TTL)	V_{SS}	0.8	V
V_{OL}	Low-level output voltage	R_L = 100Ω	0.90		V
V_{OH}	High-level output voltage	R_L = 100Ω		1.60	V
I_{IN}[4]	Input leakage current	$V_{IN} = V_{DD}$	-10	+10	µA
I_{CSOUT}	Cold Spare Leakage LVDS Outputs	V_{IN}=5.5V, V_{DD}=V_{SS}	-10	+10	µA
V_{OD}[1]	Differential Output Voltage	R_L = 100Ω(figure 5)	250	400	mV
ΔV_{OD}[1]	Change in Magnitude of V_{OD} for Complementary Output States	R_L = 100Ω(figure 5)		10	mV
V_{OS}	Offset Voltage	R_L = 100Ω, $\left(Vos = \frac{Voh + Vol}{2}\right)$	1.125	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States	R_L = 100Ω(figure 5)		25	mV
V_{CL}[3]	Input clamp voltage	I_{CL} = -18mA		-1.5	V
I_{OS}[3]	Output Short Circuit Current	V_{OUT} = 0V[2]		5.0	mA
I_{OZ}[4]	Output Three-State Current	EN = 0.8V and $\overline{EN}$ = 2.0 V, V_{OUT} = 0V or V_{DD}	-10	+10	µA
I_{CCL}[4]	Loaded supply current drivers enabled	R_L = 100Ω all channels $V_{IN} = V_{DD}$ or V_{SS}(all inputs)		25.0	mA
I_{CCZ}[4]	Loaded supply current drivers disabled	$D_{IN} = V_{DD}$ or V_{SS} EN = V_{SS}, $\overline{EN} = V_{DD}$		10.0	mA

Notes:

1. Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except differential voltages.
2. Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.
3. Guaranteed by characterization.
4. Devices are tested @ V_{DD} = 5.5V only.

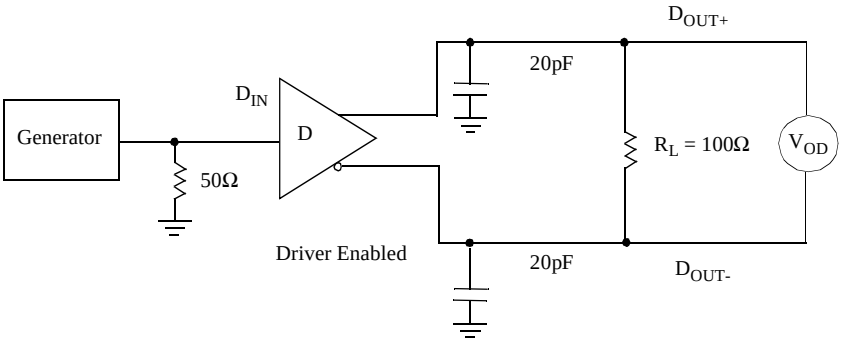


Figure 5. Driver V_{OD} and V_{OS} Test Circuit or Equivalent Circuit

AC SWITCHING CHARACTERISTICS[1, 2, 3, 4]

(V_{DD} = +5.0V ± 10%, T_A = -55 °C to +125 °C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{PHLD}	Differential Propagation Delay High to Low (figures 6 and 7)	0.5	5.0	ns
t_{PLHD}	Differential Propagation Delay Low to High (figures 6 and 7)	0.5	5.0	ns
t_{SKD}[4]	Differential Skew (t_{PHLD} - t_{PLHD}) (figures 6 and 7)	0	3.0	ns
t_{SK1}[4]	Channel-to-Channel Skew[1] (figures 6 and 7)	0	3.0	ns
t_{SK2}[4]	Chip-to-Chip Skew[5] (figure 6 and 7)		4.5	ns
t_{TLH}[4]	Rise Time (figures 6 and 7)		2.0	ns
t_{THL}[4]	Fall Time (figures 6 and 7)		2.0	ns
t_{PHZ}[4]	Disable Time High to Z (figures 8 and 9)		10	ns
t_{PLZ}[4]	Disable Time Low to Z (figures 8 and 9)		10	ns
t_{PZH}[4]	Enable Time Z to High (figures 8 and 9)		10	ns
t_{PZL}[4]	Enable Time Z to Low (figures 8 and 9)		10	ns

Notes:
1. Channel-to-Channel Skew is defined as the difference between the propagation delay of the channel and the other channels in the same chip with an event on the inputs.
2. Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50, $t_r \leq$ 6 ns, and $t_f \leq$ 6 ns.
3. C_L includes probe and jig capacitance.
4. Guaranteed by characterization
5. Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.

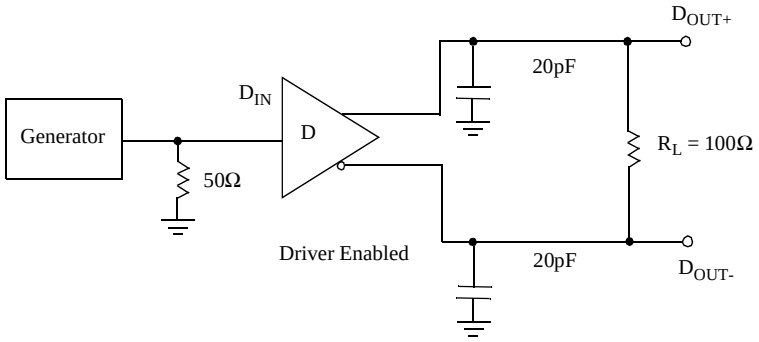


Figure 6. Driver Propagation Delay and Transition Time Test Circuit or Equivalant Circuit

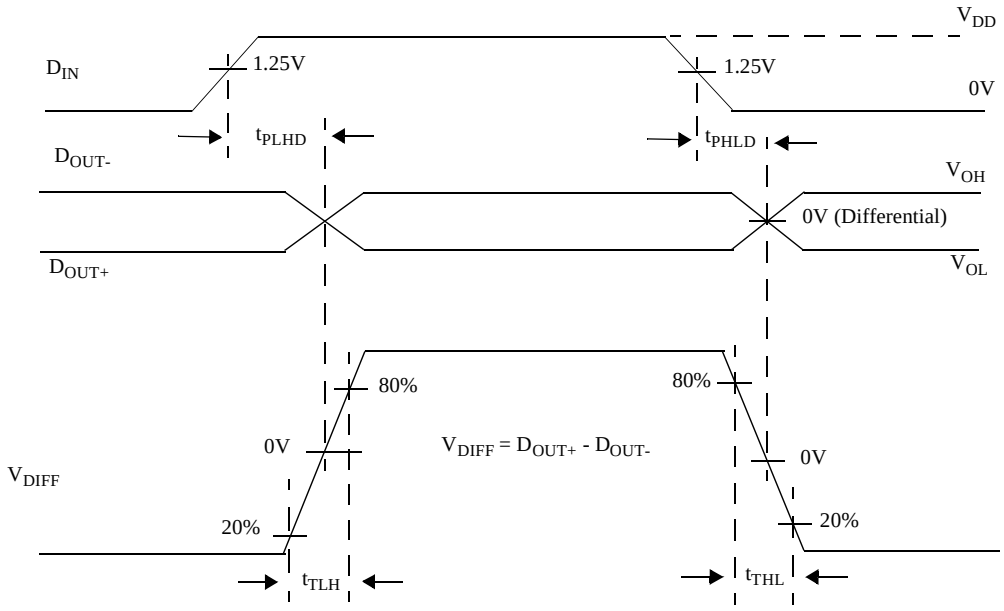


Figure 7. Driver Propagation Delay and Transition Time Waveforms

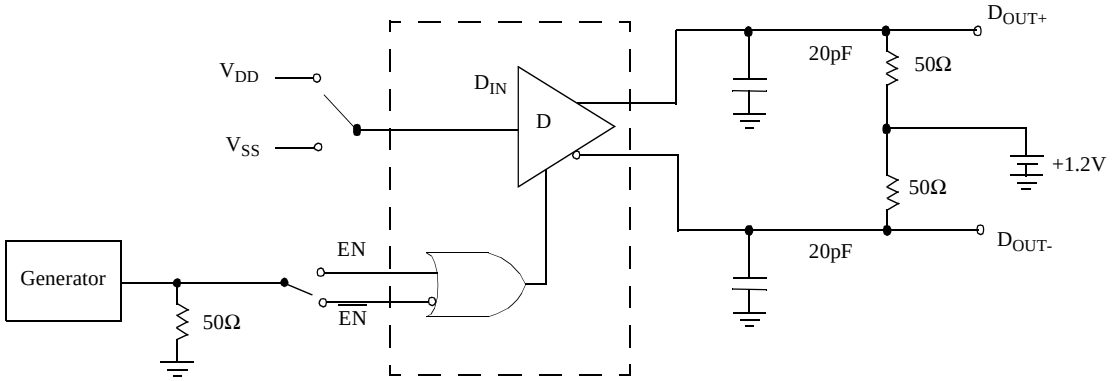


Figure 8. Driver Three-State Delay Test Circuit or Equivalant Circuit

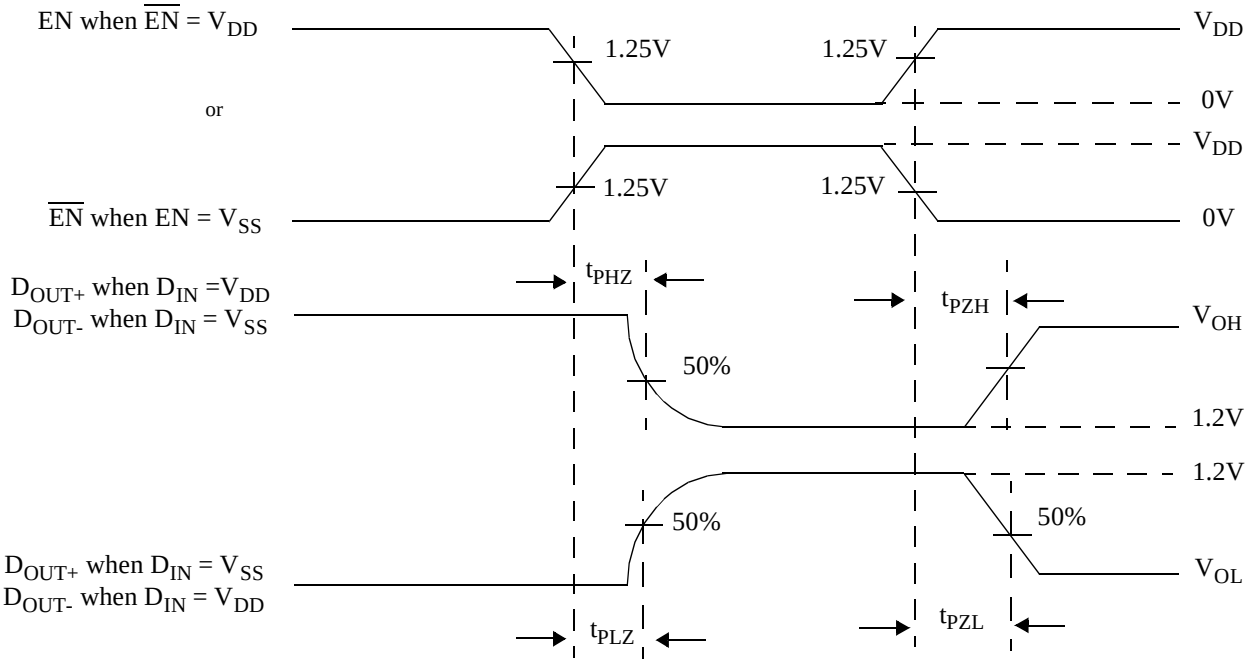
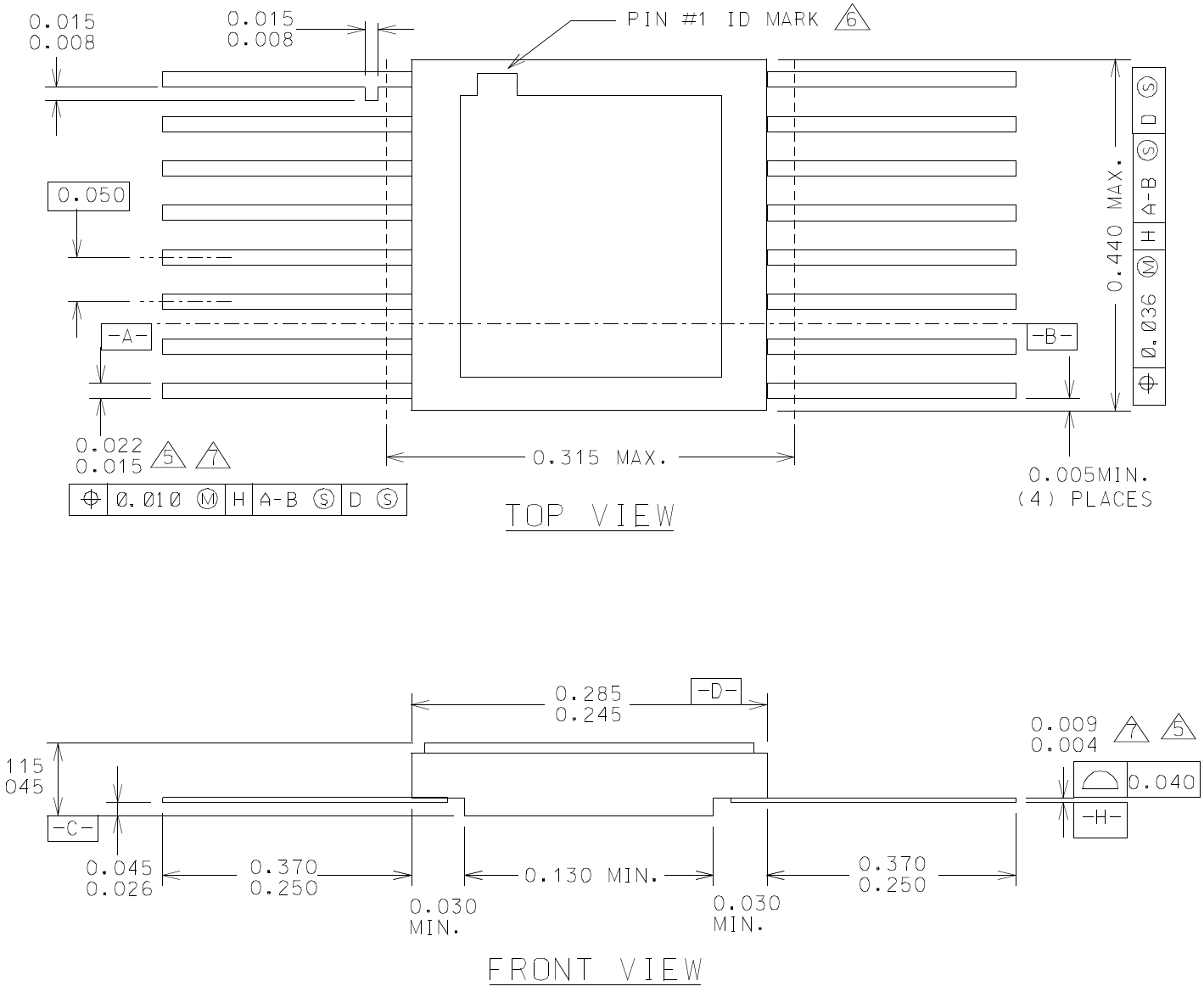


Figure 9. Driver Three-State Delay Waveform

PACKAGING



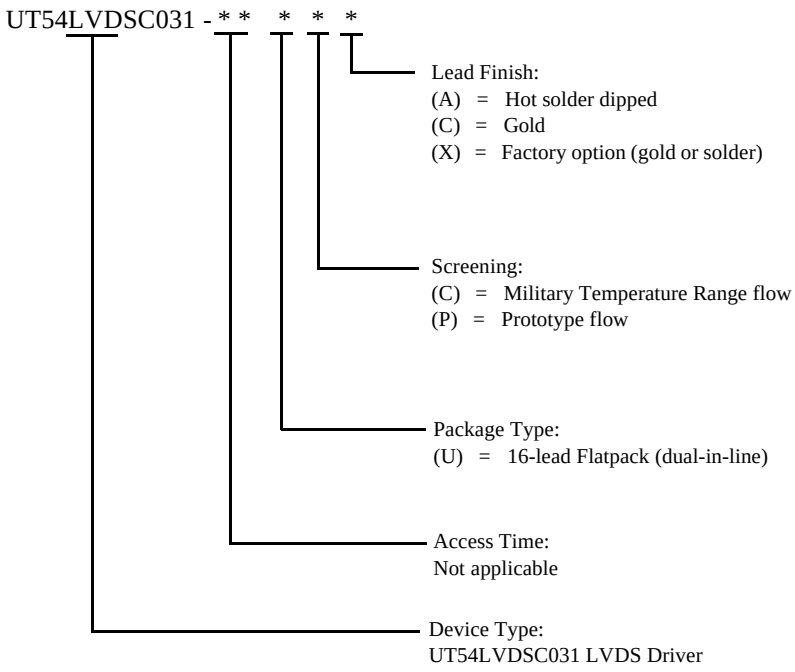
Notes:

1. All exposed metalized areas are gold plated over electroplated nickel per MIL-PRF-38535.
2. The lid is electrically connected to VSS.
3. Lead finishes are in accordance to MIL-PRF-38535.
4. Package dimensions and symbols are similar to MIL-STD-1835 variation F-5A.
5. Lead position and coplanarity are not measured.
6. ID mark symbol is vendor option.
7. With solder, increase maximum by 0.003.

Figure 10. 16-pin Ceramic Flatpack

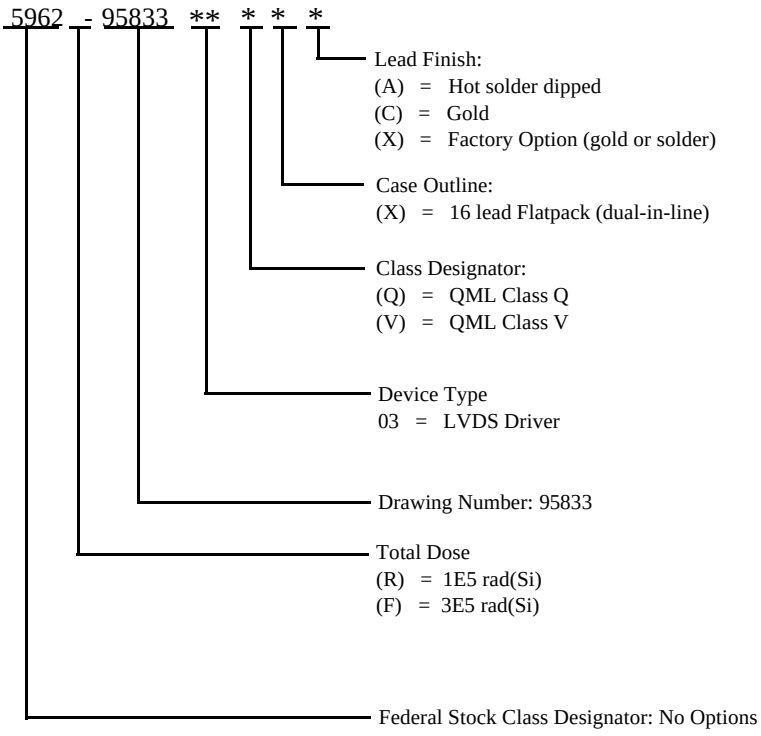
ORDERING INFORMATION

UT54LVDSC031 QUAD DRIVER:



Notes:
1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Prototype flow per UTMC Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY. Radiation neither tested nor guaranteed.
4. Military Temperature Range flow per UTMC Manufacturing Flows Document. Devices are tested at -55°C, room temp, and 125°C. Radiation neither tested nor guaranteed.

UT54LVDSC031 QUAD DRIVER: SMD



Notes:
1.Lead finish (A,C, or X) must be specified.
2.If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3.Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.