PowerStore 128K x 8 nvSRAM

Features

- High-performance CMOS non-volatile static RAM 1024x1024 bits
- 25 ns Access Time
- 10 ns Output Enable Access Times
- I_{CC} = 15 mA at 200 ns Cycle Time
- Unlimited Read and Write to SRAM
- Automatic STORE to EEPROM on Power Down
- Hardware or Software initiated STORE (t_{STORE} < 10 ms)
- Automatic STORE Timing
- 10^6 STORE cycles to EEPROM
- 100 years data retention in EEPROM
- Automatic RECALL on Power Up
- Software RECALL Initiation (t_{RECALL} < 20 µs)
- Unlimited RECALL cycles from EEPROM
- Single 5 V ± 10 % Operation
- Operating temperature ranges
    0 to 70 °C
    -40 to 85 °C
- CECC 90000 Quality Standard
- ESD protection > 2000 V (MIL STD 883C M3015.7)
- Packages: SOP32 (450 mil)
    PDIP32 (600 mil)

Description

The U632H1708 has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as an ordinary static RAM. In nonvolatile operation, data is transferred in parallel from SRAM to EEPROM or from EEPROM to SRAM. In this mode SRAM functions are disabled.

The U632H1708 is a fast static RAM (25 ns), with a nonvolatile electrically erasable PROM (EEPROM) element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent nonvolatile data resides in EEPROM.

Data transfers from the SRAM to the EEPROM (the STORE operation) take place automatically upon power down using charge stored in an external 100 µF capacitor. Transfers from the EEPROM to the SRAM (the RECALL operation) take place automatically on

power up. The U632H1708 combines the high performance and ease of use of a fast SRAM with nonvolatile data integrity.

STORE cycles also may be initiated under user control via a software sequence or via a single pin (HSB). Once a STORE cycle is initiated, further input or output are disabled until the cycle is completed.

Because a sequence of addresses is used for STORE initiation, it is important that no other read or write accesses intervene in the sequence or the sequence will be aborted.

RECALL cycles may also be initiated by a software sequence.

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells.

The RECALL operation in no way alters the data in the EEPROM cells. The nonvolatile data can be recalled an unlimited number of times.

Pin Configuration

Top View
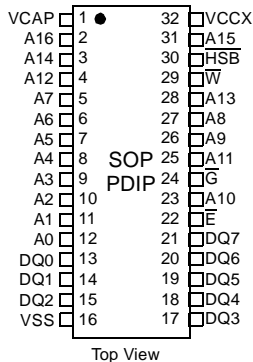
Signal Name	Signal Description
A0 - A16	Address Inputs
DQ0 - DQ7	Data In/Out
E̅	Chip Enable
G̅	Output Enable
W̅	Write Enable
VCCX	Power Supply Voltage
VSS	Ground
VCAP	Capacitor
H̅S̅B̅	Hardware Store/Busy

Logic Block Diagram

ZMD
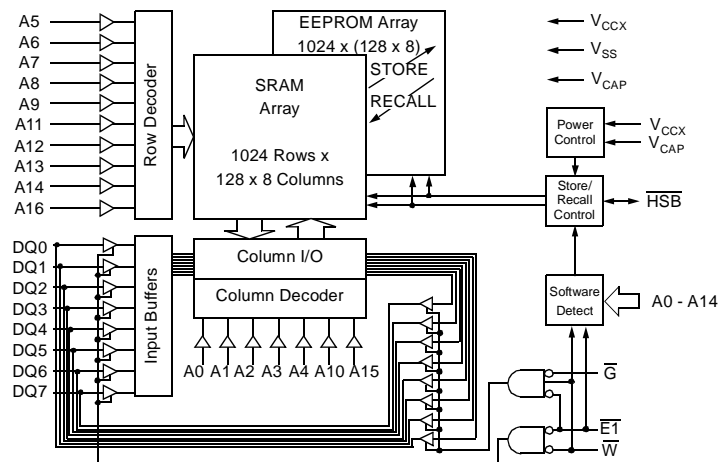
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