SoftStore 64 x 4 nvSRAM

Features

- High-performance CMOS non-volatile static RAM 64 x 4 bits
- 25 and 45 ns Access Times
- 12 and 25 ns Output Enable Times
- I_{CC} = 10 mA at 200 ns Cycle Time
- Unlimited Read and Write to SRAM
- Software STORE Initiation (STORE Cycle Time < 4 ms)
- Automatic STORE Timing
- 10^5 STORE cycles to EEPROM
- 10 year data retention in EEPROM
- Automatic RECALL on Power Up
- Software RECALL Initiation (RECALL Cycle Time < 10 µs)
- Unlimited RECALL cycles from EEPROM
- Single 5 V ± 10 % Operation
- Operating temperature ranges
  0 to 70 °C
  -40 to 85 °C
- CECC 90000 Quality Standard
- ESD characterization according MIL STD 883C M3015.7-HBM
- Package: SOP14 (150 mil)

Description

The U631H0604 has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as an ordinary static RAM. In nonvolatile operation, data is transferred in parallel from SRAM to EEPROM or from EEPROM to SRAM. In this mode SRAM functions are disabled.

The U631H0604 is a fast static RAM (25 and 45 ns), with a nonvolatile electrically erasable PROM (EEPROM) element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent nonvolatile data resides in EEPROM.

Data transfers from the SRAM to the EEPROM (the STORE operation), or from the EEPROM to the SRAM (the RECALL operation) are initiated through software sequences.

The U631H0604 combines the high performance and ease of use of a fast SRAM with nonvolatile data integrity.

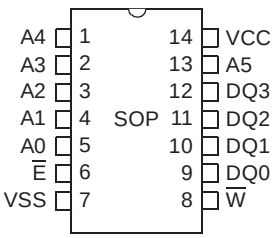
Once a STORE cycle is initiated, further input or output are disabled until the cycle is completed.

Because a sequence of addresses is used for STORE initiation, it is important that no other read or write accesses intervene in the sequence or the sequence will be aborted.

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells.

The RECALL operation in no way alters the data in the EEPROM cells. The nonvolatile data can be recalled an unlimited number of times.

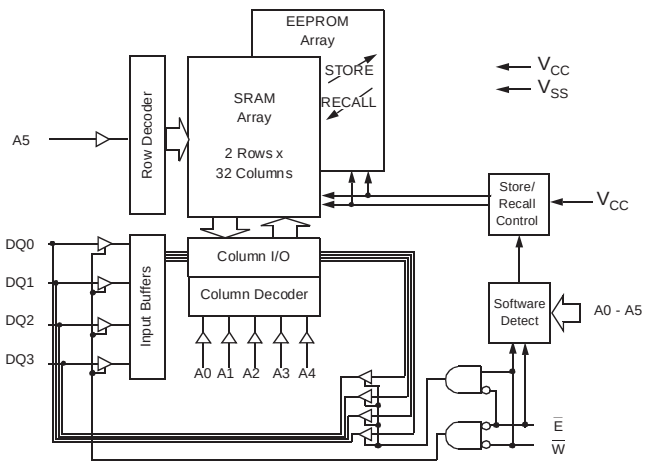
Pin Configuration



Top View

Signal Name	Signal Description
A0 - A4	Address Inputs
DQ0 - DQ3	Data In/Out
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
VCC	Power Supply Voltage
VSS	Ground

Logic Block Diagram



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