

μ PD4516421A, 4516821A, 4516161A for Rev. P

16M-bit Synchronous DRAM

Description

The μ PD4516421A, 4516821A, 4516161A are high-speed 16,777,216-bit synchronous dynamic random-access memories, organized as 2,097,152 × 4 × 2, 1,048,576 × 8 × 2 and 524,288 × 16 × 2 (word × bit × bank), respectively.

The synchronous DRAMs achieve high-speed data transfer using the pipeline architecture.

All inputs and outputs are synchronized with the positive edge of the clock.

The synchronous DRAMs are compatible with Low Voltage TTL (LVTTL).

The synchronous DRAMs are packaged in 44-pin TSOP (II) (x4, x8) and 50-pin TSOP (II) (x16).

Features

- Fully Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- · Pulsed interface
- · Possible to assert random column address in every cycle
- Dual internal banks controlled by A11 (Bank Select)
- Programmable burst-length (1, 2, 4, 8, Full Page)
- Programmable wrap sequence (Sequential/Interleave)
- Programmable CAS latency (2, 3)
- Automatic precharge and controlled precharge
- · CBR (Auto) refresh and self refresh
- ×4, ×8, ×16 organization
- Single + 3.3 \pm 0.3 V power supply
- LVTTL compatible
- Byte control (×16) by LDQM and UDQM
- 2,048 refresh cycles/32 ms
- · Burst termination by Burst Stop command and Precharge command

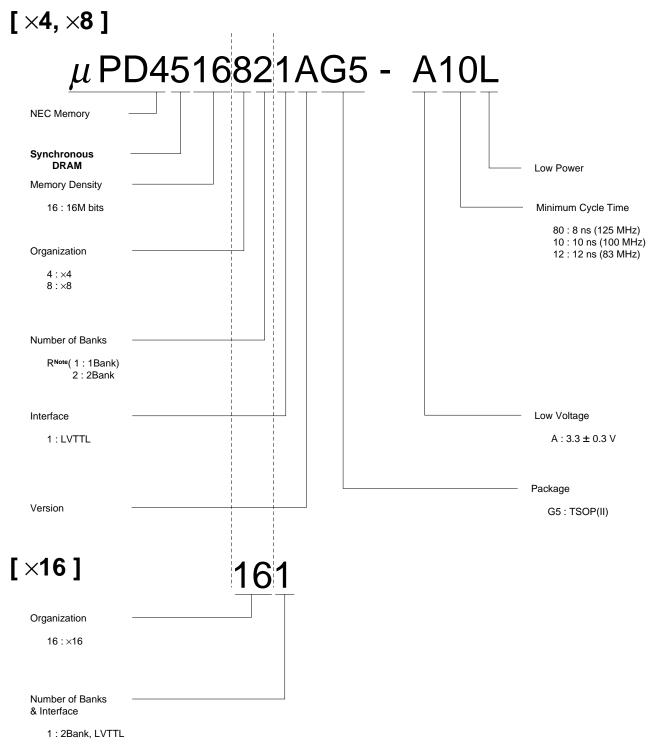
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Ordering Information

Part number	Organization (word \times bit \times bank)	Clock frequency MHz (MAX.)	Package	
μPD4516421AG5-A80-9NF		125		
μPD4516421AG5-A10-9NF	0.140	100	44-pin Plastic TSOP(II)	
μPD4516421AG5-A10B-9NF	2 M × 4 × 2	100	(400 mil)	
μPD4516421AG5-A12-9NF		83		
μPD4516821AG5-A80-9NF		125		
μPD4516821AG5-A10-9NF	4.14.	100	44-pin Plastic TSOP(II)	
μPD4516821AG5-A10B-9NF	1 M × 8 × 2	100	(400 mil)	
μPD4516821AG5-A12-9NF		83		
μPD4516161AG5-A80-9NF		125		
μPD4516161AG5-A10-9NF	540 1/2 40 0	100	50-pin Plastic TSOP(II)	
μPD4516161AG5-A10B-9NF	512 K × 16 × 2	100	(400 mil)	
μPD4516161AG5-A12-9NF		83		
μPD4516421AG5-A80L-9NF		125		
μPD4516421AG5-A10L-9NF	0.140	100	44-pin Plastic TSOP(II)	
μPD4516421AG5-A10BL-9NF	2 M × 4 × 2	100	(400 mil)	
μPD4516421AG5-A12L-9NF		83		
μPD4516821AG5-A80L-9NF		125		
μPD4516821AG5-A10L-9NF	1	100	44-pin Plastic TSOP(II)	
μPD4516821AG5-A10BL-9NF	1 M × 8 × 2	100	(400 mil)	
μPD4516821AG5-A12L-9NF	1	83		
μPD4516161AG5-A80L-9NF		125		
μPD4516161AG5-A10L-9NF	540 1/2 40 0	100	50-pin Plastic TSOP(II)	
μPD4516161AG5-A10BL-9NF	512 K × 16 × 2	100	(400 mil)	
μPD4516161AG5-A12L-9NF	1	83		

Part Number



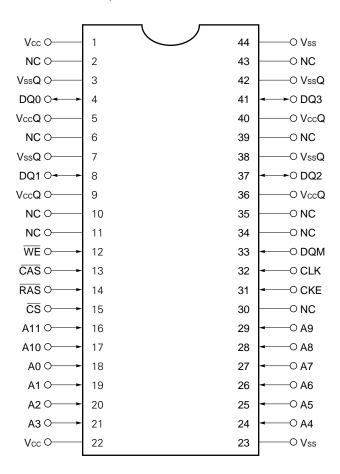
Note R: Reserved



Pin Configurations

[µPD4516421A]

44-pin Plastic TSOP(II) (400 mil) μ PD4516421AG5-9NF



A0 to A11Note: Address inputs
DQ0 to DQ3: Data inputs/outputs
CLK: System clock input
CKE: Clock enable
CS: Chip select

RAS : Row address strobe
CAS : Column address strobe

WE : Write enable

DQM : DQ mask enable

Vcc : Supply voltage

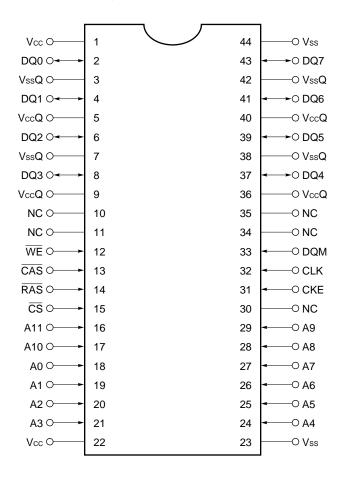
Vss : Ground

VccQ: Supply voltage for DQNoteA0 to A10: Row address inputsVssQ: Ground for DQA0 to A9 : Column address inputs

NC : No connection A11 : Bank select

[µPD4516821A]

44-pin Plastic TSOP(II) (400 mil) μ PD4516821AG5-9NF



A0 to A11 Note: Address inputs
DQ0 to DQ7 : Data inputs/outputs
CLK : System clock input
CKE : Clock enable
CS : Chip select

RAS : Row address strobe
CAS : Column address strobe

WE : Write enable
DQM : DQ mask enable
Vcc : Supply voltage

Vss : Ground

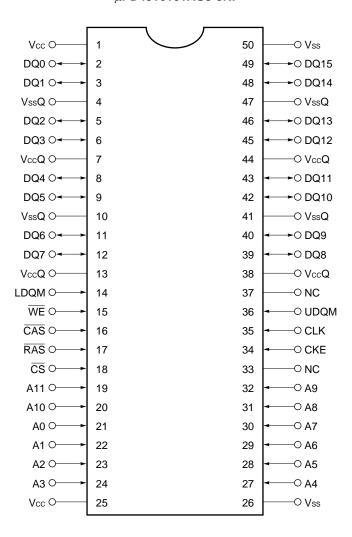
VccQ: Supply voltage for DQNoteA0 to A10: Row address inputsVssQ: Ground for DQA0 to A8 : Column address inputs

NC : No connection A11 : Bank select



[µPD4516161A]

50-pin Plastic TSOP(II) (400 mil) μ PD4516161AG5-9NF



A0 to A11 Note: Address inputs

DQ0 to DQ15: Data inputs/outputs

CLK: System clock input

CKE: Clock enable

CS: Chip select

RAS : Row address strobe
CAS : Column address strobe

WE : Write enable

UDQM : Upper DQ mask enable LDQM : Lower DQ mask enable

Vcc : Supply voltage

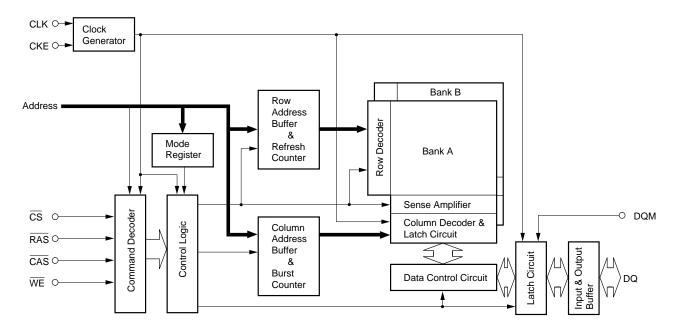
Vss : Ground

VccQ: Supply voltage for DQNoteA0 to A10: Row address inputsVssQ: Ground for DQA0 to A7 : Column address inputs

NC : No connection A11 : Bank select



Block Diagram





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1. Input/Output Pin Function

Pin name	Input/Output	Function
CLK	Input	CLK is the master clock input. Other inputs signals are referenced to the CLK rising edge.
CKE	Input	CKE determine validity of the next CLK (clock). If CKE is high, the next CLK rising edge is valid; otherwise it is invalid. If the CLK rising edge is invalid, the internal clock is not issued and the μ PD4516 $\times\times$ A suspends operation. When the μ PD4516 $\times\times$ A is not in burst mode and CKE is negated, the device enters power down mode. During power down mode, CKE must remain low.
CS	Input	$\overline{\text{CS}}$ low starts the command input cycle. When $\overline{\text{CS}}$ is high, commands are ignored but operations continue.
RAS, CAS, WE	Input	RAS, CAS and WE have the same symbols on conventional DRAM but different functions. For details, refer to the command table.
A0 - A11	Input	Row Address is determined by A0 - A10 at the CLK (clock) rising edge in the activate command cycle. It does not depend on the bit organization. Column Address is determined by A0 - A9 at the CLK rising edge in the read or write command cycle. It depends on the bit organization: A0 - A9 for ×4 device, A0 - A8 for ×8 device and A0 - A7 for ×16 device. A11 is the bank select signal (BS). In command cycle, A11 low selects bank A and A11 high selects bank B. A10 defines the precharge mode. When A10 is high in the precharge command cycle, both banks are precharged; when A10 is low, only the bank selected by A11 is precharged. When A10 high in read or write command cycle, the precharge start automatically after the burst access.
DQM UDQM LDQM	Input	DQM controls I/O buffers. In ×16 products, UDQM and LDQM control upper byte and lower byte I/O buffers, respectively. In read mode, DQM controls the output buffers like a conventional OE pin. DQM high and DQM low turn the output buffers off and on, respectively. The DQM latency for the read is two clocks. In write mode, DQM controls the word mask. Input data is written to the memory cell if DQM is low but not if DQM is high. The DQM latency for the write is zero.
DQ0 - DQ15	Input/Output	DQ pins have the same function as I/O pins on a conventional DRAM.
Vcc Vss VccQ VssQ	(Power supply)	Vcc and Vss are power supply pins for internal circuits. VccQ and VssQ are power supply pins for the output buffers.

2. Commands

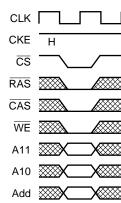
Mode register set command

 $(\overline{CS}, \overline{RAS}, \overline{CAS}, \overline{WE} = Low)$

The μ PD4516xxxA has a mode register that defines how the device operates. In this command, A0 through A11 are the data input pins. After power on, the mode register set command must be executed to initialize the device.

The mode register can be set only when both banks are in idle state. During 2CLK (trsc) following this command, the μ PD4516×××A cannot accept any other commands.

Fig. 1 Mode register set command



Activate command

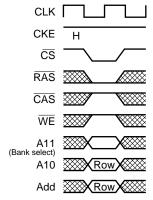
$$(\overline{CS}, \overline{RAS} = Low, \overline{CAS}, \overline{WE} = High)$$

The μ PD4516×××A has two banks, each with 2,048 rows.

This command activates the bank selected by A11 (BS) and a row address selected by A0 through A10.

This command corresponds to a conventional DRAM's RAS falling.

Fig. 2 Row address strobe and bank active command



Precharge command

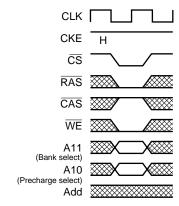
$$(\overline{CS}, \overline{RAS}, \overline{WE} = Low, \overline{CAS} = High)$$

This command begins precharge operation of the bank selected by A11 (BS). When A10 is High, both banks are precharged, regardless of A11. When A10 is Low, only the bank selected by A11 is precharged. A11 low selects bank A and A11 high selects bank B.

After this command, the μ PD4516×××A can't accept the activate command to the precharging bank during trap (precharge to activate command period).

This command corresponds to a conventional DRAM's RAS rising.

Fig. 3 Precharge command



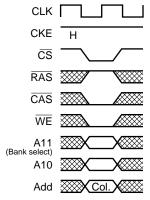


Write command

$$(\overline{CS}, \overline{CAS}, \overline{WE} = Low, \overline{RAS} = High)$$

If the mode register is in the burst write mode, this command sets the burst start address given by the column address to begin the burst write operation. The first write data in burst can be input with this command with subsequent data on following clocks.

Fig. 4 Column address and write command

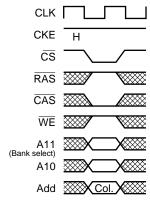


Read command

$$(\overline{CS}, \overline{CAS} = Low, \overline{RAS}, \overline{WE} = High)$$

Read data is available after $\overline{\text{CAS}}$ latency requirements have been met. This command sets the burst start address given by the column address.

Fig. 5 Column address and read command



CBR (auto) refresh command

$$(\overline{CS}, \overline{RAS}, \overline{CAS} = Low, \overline{WE}, CKE = High)$$

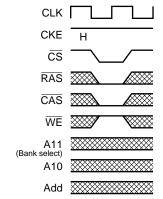
This command is a request to begin the CBR refresh operation. The refresh address is generated internally.

Before executing CBR refresh, both banks must be precharged.

After this cycle, both banks will be in the idle (precharged) state and ready for a row activate command.

During tRC period (from refresh command to refresh or activate command), the μ PD4516×××A cannot accept any other command.

Fig. 6 Auto refresh command



Self refresh entry command

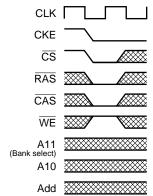
$$(\overline{CS}, \overline{RAS}, \overline{CAS}, CKE = Low, \overline{WE} = High)$$

After the command execution, self refresh operation continues while CKE remains low. When CKE goes to high, the μ PD4516×××A exits the self refresh mode.

During self refresh mode, refresh interval and refresh operation are performed internally, so there is no need for external control.

Before executing self refresh, both banks must be precharged.

Fig. 7 Self refresh entry command

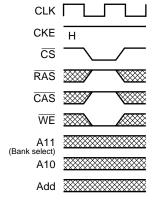


Burst stop command

$$(\overline{CS}, \overline{WE} = Low, \overline{RAS}, \overline{CAS} = High)$$

This command terminates the current burst operation.

Fig. 8 Burst stop command in Full Page mode

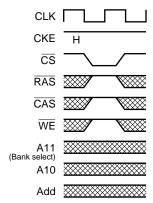


No operation

$$(\overline{CS} = Low, \overline{RAS}, \overline{CAS}, \overline{WE} = High)$$

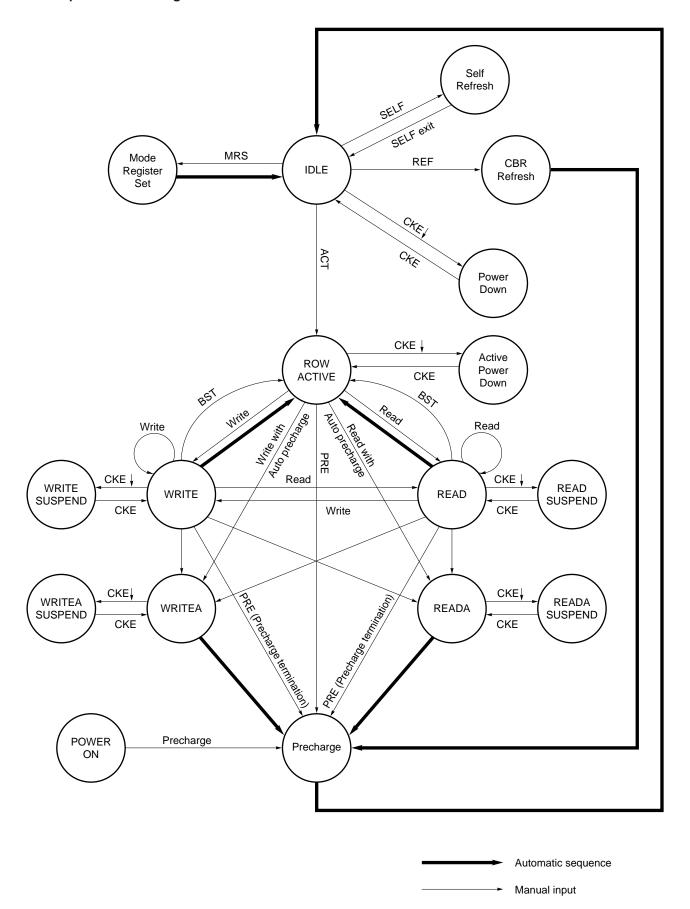
This command is not a execution command. No operations begin or terminate by this command.

Fig. 9 No operation





3. Simplified State Diagram



4. Truth Table

4.1 Command Truth Table

Function	Symbol	Ck	(E	cs	RAS	CAS	WE	A11	A10	A9-
Function	Symbol	n-1	n	CS	KAS	CAS	VVE	AII	ATO	A0
Device deselect	DESL	Н	×	Н	×	×	×	×	×	×
No operation	NOP	Н	×	L	Н	Н	Н	×	×	×
Burst stop	BST	Н	×	L	Н	Н	L	×	×	×
Read	READ	Н	×	L	Н	L	Н	V	L	V
Read with auto precharge	READA	Н	×	L	Н	L	Н	V	Н	٧
Write	WRIT	Н	×	L	Н	L	L	V	L	٧
Write with auto precharge	WRITA	Н	×	L	Н	L	L	V	Н	V
Bank activate	ACT	Н	×	L	L	Н	Н	V	V	V
Precharge select bank	PRE	Н	×	L	L	Н	L	V	L	×
Precharge all banks	PALL	Н	×	L	L	Н	L	×	Н	×
Mode register set	MRS	Н	×	L	L	L	L	L	L	V

4.2 DQM Truth Table

Function	Symbol	Cł	ΚE	DQM			
Function	Symbol	n-1	n	U	Г		
Data write/output enable	ENB	Н	×		L		
Data mask/output disable	MASK	Н	× H				
Upper byte write enable/output enable	ENBU	Н	×	L	×		
Lower byte write enable/output enable	ENBL	Н	×	×	L		
Upper byte write inhibit/output disable	MASKU	Н	×	Н	×		
Lower byte write inhibit/output disable	MASKL	Н	×	×	Н		

4.3 CKE Truth Table

Current state	Function	Symbol	Cł	ΚE	- CS	RAS	CAS	WE	Add-
Current state	Function	Symbol	n-1	n	CS	RAS	CAS	VVE	ress
Activating	Clock suspend mode entry		Н	L	×	×	×	×	×
Any	Clock suspend		L	L	×	×	×	×	×
Clock suspend	Clock suspend mode exit		L	Н	×	×	×	×	×
Idle	CBR refresh command	REF	Н	Н	L	L	L	Н	×
Idle	Self refresh entry	SELF	Н	L	L	L	L	Н	×
Self refresh	Self refresh exit		L	Н	L	Н	Н	Н	×
			L	Н	Н	×	×	×	×
Idle	Power down entry		Н	L	×	×	×	×	×
Power down	Power down exit		L	Н	×	×	×	×	×

H: High level, L: Low level

×: High or Low level (Don't care), V: Valid Data input



4.4 Operative Command Table Notes1, 2

(1/3)

Current state	cs	RAS	CAS	WE	Address	Command	Action	Notes
Idle	Н	×	×	×	×	DESL	Nop or Power down	3
	L	Н	Н	×	×	NOP or BST	Nop or Power down	3
	L	Н	L	Н	BA, CA, A10	READ/READA	ILLEGAL	4
	L	Н	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	4
	L	L	Н	Н	BA, RA	ACT	Row activating	
	L	L	Н	L	BA, A10	PRE/PALL	Nop	
	L	L	L	Н	×	REF/SELF	Refresh or Self refresh	5
	L	L	L	L	Op-Code	MRS	Mode register accessing	
Row active	Н	×	×	×	×	DESL	Nop	
	L	Н	Н	×	×	NOP or BST	Nop	
	L	Н	L	Н	BA, CA, A10	READ/READA	Begin read:Determine AP	6
	L	Н	L	L	BA, CA, A10	WRIT/WRITA	Begin write:Determine AP	6
	L	L	Н	Н	BA, RA	ACT	ILLEGAL	4
	L	L	Н	L	BA, A10	PRE/PALL	Precharge	7
	L	L	L	Н	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Read	Н	×	×	×	×	DESL	Continue burst to end → Row active	
	L	Н	Н	Н	×	NOP	Continue burst to end → Row active	
	L	Н	Н	L	×	BST	Burst stop → Row active	
	L	Н	L	Н	BA, CA, A10	READ/READA	Term burst, new read:Determine AP	8
	L	Н	L	L	BA, CA, A10	WRIT/WRITA	Term burst, start write:Determine AP	8, 9
	L	L	Н	Н	BA, RA	ACT	ILLEGAL	4
	L	L	Н	L	BA, A10	PRE/PALL	Term burst, precharging	
	L	L	L	Н	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write	Н	×	×	×	×	DESL	Continue burst to end → Write recovering	
	L	Н	Н	Н	×	NOP	Continue burst to end → Write recovering	
	L	Н	Н	L	×	BST	Burst stop → Row active	
	L	Н	L	н	BA, CA, A10	READ/READA	Term burst, start read:Determine AP	8, 9
	L	Н	L	L	BA, CA, A10	WRIT/WRITA	Term burst, new write:Determine AP	8
	L	L	Н	Н	BA, RA	ACT	ILLEGAL	4
	L	L	Н	L	BA, A10	PRE/PALL	Term burst, precharging	10
	L	L	L	Н	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	

(2/3)

Current state	cs	RAS	CAS	WE	Address	Command	Action	Notes
Read with auto	Н	×	×	×	×	DESL	Continue burst to end $ ightarrow$ Precharging	
precharge	L	Н	Н	Н	×	NOP	Continue burst to end $ ightarrow$ Precharging	
	L	Н	Н	L	×	BST	ILLEGAL	
	L	Н	L	Н	BA, CA, A10	READ/READA	ILLEGAL	4
	L	Н	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	4
	L	L	Н	Н	BA, RA	ACT	ILLEGAL	4
	L	L	Н	L	BA, A10	PRE/PALL	ILLEGAL	4
	L	L	L	Н	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write with auto precharge	Н	×	×	×	×	DESL	Continue burst to end → Write recovering with auto precharge	
	L	Н	Н	Н	×	NOP	Continue burst to end → Write recovering with auto precharge	
	L	Н	Н	L	×	BST	ILLEGAL	
	L	Н	L	Н	BA, CA, A10	READ/READA	ILLEGAL	4
	L	Н	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	4
	L	L	Н	Н	BA, RA	ACT	ILLEGAL	4
	L	L	Н	L	BA, A10	PRE/PALL	ILLEGAL	4
	L	L	L	Н	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Precharging	Н	×	×	×	×	DESL	$Nop \to Enter$ idle after trp	
	L	Н	Н	Н	×	NOP	$Nop \to Enter$ idle after trp	
	L	Н	Н	L	×	BST	$Nop \to Enter$ idle after trp	
	L	Н	L	Н	BA, CA, A10	READ/READA	ILLEGAL	4
	L	Н	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	4
	L	L	Н	Н	BA, RA	ACT	ILLEGAL	4
	L	L	Н	L	BA, A10	PRE/PALL	$Nop \to Enter$ idle after trp	
	L	L	L	Н	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Row activating	Н	×	×	×	×	DESL	$Nop \to Enter$ row active after t_RCD	
	L	Н	Н	Н	×	NOP	Nop → Enter row active after t _{RCD}	
	L	Н	Н	L	×	BST	Nop → Enter row active after t _{RCD}	
	L	Н	L	Н	BA, CA, A10	READ/READA	ILLEGAL	4
	L	Н	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	4
	L	L	Н	Н	BA, RA	ACT	ILLEGAL	4, 11
	L	L	Н	L	BA, A10	PRE/PALL	ILLEGAL	4
	L	L	L	Н	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	

(3/3)

Current state	cs	RAS	CAS	WE	Address	Command	Action	Notes
Write	Н	×	×	×	×	DESL	Nop → Enter row active after t _{DPL}	
recovering	L	Н	Н	Н	×	NOP	Nop → Enter row active after t _{DPL}	
	L	Н	Н	L	×	BST	Nop → Enter row active after t _{DPL}	
	L	Н	L	Н	BA, CA, A10	READ/READA	Start read, Determine AP	9
	L	Н	L	L	BA, CA, A10	WRIT/WRITA	New write, Determine AP	
	L	L	Н	Н	BA, RA	ACT	ILLEGAL	4
	L	L	Н	L	BA, A10	PRE/PALL	ILLEGAL	4
	L	L	L	Н	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write	Н	×	×	×	×	DESL	Nop → Enter precharge after t _{DPL}	
recovering with	L	Н	Н	Н	×	NOP	Nop → Enter precharge after t _{DPL}	
auto precharge	L	Н	Н	L	×	BST	Nop → Enter precharge after t _{DPL}	
	L	Н	L	Н	BA, CA, A10	READ/READA	ILLEGAL	4, 9
	L	Н	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	4
	L	L	Н	Н	BA, RA	ACT	ILLEGAL	4
	L	L	Н	L	BA, A10	PRE/PALL	ILLEGAL	4
	L	L	L	Н	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Refreshing	Н	×	×	×	×	DESL	Nop → Enter idle after t _{RC}	
	L	Н	Н	×	×	NOP/BST	Nop → Enter idle after t _{RC}	
	L	Н	L	×	×	READ/WRIT	ILLEGAL	
	L	L	Н	×	×	ACT/PRE/PALL	ILLEGAL	
	L	L	L	×	×	REF/SELF/MRS	ILLEGAL	
Mode register	Н	×	×	×	×	DESL	Nop → Enter idle after t _{RSC}	
accessing	L	Н	Н	Н	×	NOP	Nop → Enter idle after trsc	
	L	Н	Н	L	×	BST	ILLEGAL	
	L	Н	L	×	×	READ/WRITE	ILLEGAL	
	L	L	×	×	×	ACT/PRE/PALL/ REF/SELF/MRS	ILLEGAL	

- Notes 1. H: High level, L: Low level, x: High or Low level (Don't care), V: Valid data input
 - 2. All entries assume that CKE was active (High level) during the preceding clock cycle.
 - **3.** If both banks are idle, and CKE is inactive (Low level), μPD4516×××A will enter Power down mode. All input buffers except CKE will be disabled.
 - **4.** Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
 - **5.** If both banks are idle, and CKE is inactive (Low level), μPD4516×××A will enter Self refresh mode. All input buffers except CKE will be disabled.
 - 6. Illegal if tRCD is not satisfied.
 - 7. Illegal if tras is not satisfied.
 - **8.** Must satisfy burst interrupt condition.
 - **9.** Must satisfy bus contention, bus turn around, and/or write recovery requirements.
 - 10. Must mask preceding data which don't satisfy topl.
 - 11. Illegal if trrd is not satisfied.

4.5 Command Truth Table for CKE^{Note 1}

Current state	CKE n-1	CKE n	cs	RAS	CAS	WE	Address	Action	Notes
Self refresh	Н	×	×	×	×	×	×	INVALID, CLK(n-1) would exit S.R.	
(S.R.)	L	Н	Н	×	×	×	×	S.R. Recovery	
	L	Н	L	Н	Н	×	×	S.R. Recovery	
	L	Н	L	Н	L	×	×	ILLEGAL	
	L	Н	L	L	×	×	×	ILLEGAL	
	L	L	×	×	×	×	×	Maintain S.R.	
Self refresh	Н	Н	Н	×	×	×	×	Idle after tro	
recovery	Н	Н	L	Н	Н	×	×	Idle after t _{RC}	
	Н	Н	L	Н	L	×	×	ILLEGAL	
	Н	Н	L	L	×	×	×	ILLEGAL	
	Н	L	Н	×	×	×	×	ILLEGAL	
	Н	L	L	Н	Н	×	×	ILLEGAL	
	Н	L	L	Н	L	×	×	ILLEGAL	
	Н	L	L	L	×	×	×	ILLEGAL	
Power down	Н	×	×	×	×	×		INVALID, CLK(n-1) would exit P.D.	
(P.D.)	L	Н	×	×	×	×	×	EXIT P.D. → Idle	
	L	L	×	×	×	×	×	Maintain power down mode	
Both banks idle	Н	Н	Н	×	×	×		Refer to operations in Operative Command Table	
	Н	Н	L	Н	×	×		Refer to operations in Operative Command Table	
	Н	Н	L	L	Н	×		Refer to operations in Operative Command Table	
	Н	Н	L	L	L	Н	×	Refresh	
	Н	Н	L	L	L	L	Op-Code	Refer to operations in Operative Command Table	
	Н	L	Н	×	×	×		Refer to operations in Operative Command Table	
	Н	L	L	Н	×	×		Refer to operations in Operative Command Table	
	Н	L	L	L	Н	×		Refer to operations in Operative Command Table	
	Н	L	L	L	L	Н	×	Self refresh	2
	Н	L	L	L	L	L	Op-Code	Refer to operations in Operative Command Table	
	L	×	×	×	×	×	×	Power down	2
Row active	Н	×	×	×	×	×		Refer to operations in Operative Command Table	
	L	×	×	×	×	×		Power down	3
Any state other	Н	Н	×	×	×	×	×	Refer to operations in Operative Command Table	
than listed	Н	L	×	×	×	×	×	Begin clock suspend next cycle	3
above	L	Н	×	×	×	×	×	Exit clock suspend next cycle	
	L	L	×	×	×	×	×	Maintain clock suspend	

- Notes 1. H: High level, L: Low level, X: High or low level (Don't care)
 - 2. Self refresh can be entered only from the both banks idle state. Power down can be entered from the both banks idle state or row active state.
 - 3. Must be legal command as defined in Operative Command Table.



4.6 Command Truth Table for Two Banks Operation Notes 1, 2

cs	RAS	CAS	WE	BA	A10	A9 - A0	Action	"FROM" State Note 3	"TO" State Note 4
Н	×	×	×	×	×	×	NOP	Any	Any
L	Н	Н	Н	×	×	×	NOP	Any	Any
L	Н	Н	L	×	×	×	BST	(R/W/A)0(I/A)1	A0(I/A)1
								I0(I/A)1	I0(I/A)1
								(R/W/A)1(I/A)0	A1(I/A)0
								I1(I/A)0	I1(I/A)0
L	Н	L	Н	Н	Н	CA	Read	(R/W/A)1(I/A)0	RP1(I/A)0
				Н	Н	CA		A1(R/W)0	RP1A0
				Н	L	CA		(R/W/A)1(I/A)0	R1(I/A)0
				Н	L	CA		A1(R/W)0	R1A0
				L	н	CA		(R/W/A)0(I/A)1	RP0(I/A)1
				L	Н	CA		A0(R/W)1	RP0A1
				L	L	CA		(R/W/A)0(I/A)1	R0(I/A)1
				L	L	CA		A0(R/W)1	R0A1
L	Н	L	L	Н	Н	CA	Write	(R/W/A)1(I/A)0	WP1(I/A)0
				Н	Н	CA		A1(R/W)0	WP1A0
				Н	L	CA		(R/W/A)1(I/A)0	W1(I/A)0
				Н	L	CA		A1(R/W)0	W1A0
				L	н	CA		(R/W/A)0(I/A)1	WP0(I/A)1
				L	Н	CA		A0(R/W)1	WP0A1
				L	L	CA		(R/W/A)0(I/A)1	W0(I/A)1
				L	L	CA		A0(R/W)1	W0A1
L	L	Н	Н	Н	RA		Activate Row	I1Any0	A1Any0
				L	RA			I0Any1	A0Any1
L	L	Н	L	×	Н	×	Precharge	(R/W/A/I)0(I/A)1	1011
				×	Н	×		(R/W/A/I)1(I/A)0	1110
				Н	L	×		(R/W/A/I)1(I/A)0	I1(I/A)0
				Н	L	×		(I/A)1(R/W/A/I)0	I1(R/W/A/I)0
				L	L	×		(R/W/A/I)0(I/A)1	I0(I/A)1
				L	L	×		(I/A)0(R/W/A/I)1	I0(R/W/A/I)1
L	L	L	Н	×	×	×	Refresh	1011	1011
L	L	L	L	Op-Code			Mode Register Access	1011	1011

Notes 1. Logic level abbreviations

H: High level, L: Low level, x: High or low level (Don't care)

Pin name abbreviation

BA: Bank address (A11)

2. State abbreviations

I = Idle

A = Row active

R = Read with No precharge (No precharge is posted)

W = Write with No precharge (No precharge is posted)

RP = Read with auto precharge (Precharge is posted)

WP = Write with auto precharge (Precharge is posted)

Any = Any State

X0Y1 = Y1X0 = Bank A is in state "X", Bank B is in state "Y"

(X/Y)0Z1 = Z1(X/Y)0 = Bank A is in state "X" or "Y", Bank B is in state "Z"

- 3. If the μ PD4516×××A is in a state other than above listed in the "From State" column, the command is illegal.
- **4.** The states listed under "To" might not be entered on the next clock cycle. Timing restrictions apply.

5. Initialization

The synchronous DRAM is initialized in the power-on sequence according to the following.

- (1) To stabilize internal circuits, when power is applied, a $100-\mu s$ or longer pause must precede any signal toggling.
- (2) After the pause, both banks must be precharged using the Precharge command (The Precharge all banks command is convenient).
- (3) Once the precharge is completed and the minimum trp is satisfied, the mode register can be programmed. After the mode register set cycle, trsc (2CLK minimum) pause must be satisfied as well.
- (4) Two or more CBR (Auto) refresh must be performed.
 - Remarks 1. The sequence of Mode register programming and Refresh above may be transposed.
 - 2. CKE and DQM must be held high until the Precharge command is issued to ensure data bus Hi-Z.



6. Programming the Mode Register

The mode register is programmed by the Mode register set command using address bits A11 through A0 as data inputs. The register retains data until it is reprogrammed or the device loses power.

The mode register has four fields;

Options : A11 through A7 CAS latency: A6 through A4

Wrap type : A3

Burst length: A2 through A0

Following mode register programming, no command can be issued before at least 2CLK have elapsed.

CAS Latency

CAS latency is the most critical of the parameters being set. It tells the device how many clocks must elapse before the data will be available.

The value is determined by the frequency of the clock and the speed grade of the device. The table on page 43 shows the relationship of $\overline{\text{CAS}}$ latency to the clock period and the speed grade of the device.

Burst Length

Burst Length is the number of words that will be output or input in a read or write cycle. After a read burst is completed, the output bus will become Hi-Z.

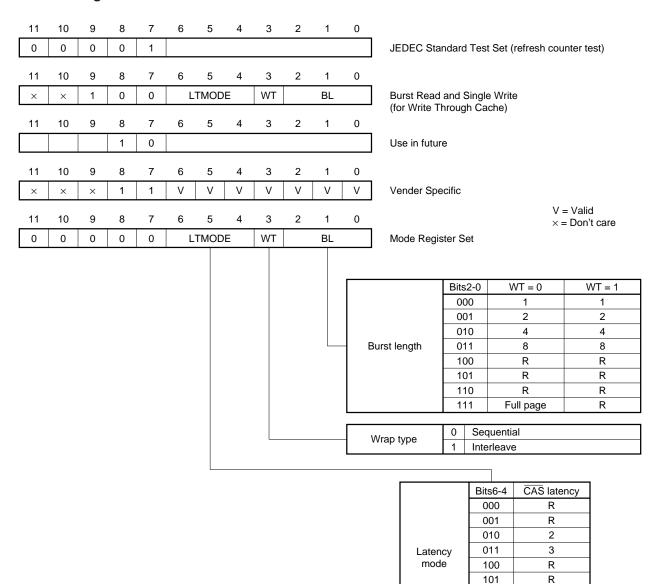
The burst length is programmable as 1, 2, 4, 8 or full page.

Wrap Type (Burst Sequence)

The wrap type specifies the order in which the burst data will be addressed. This order is programmable as either "Sequential" or "Interleave". The method chosen will depend on the type of CPU in the system.

Some microprocessor cache system are optimized for sequential addressing and others for interleaved addressing. The table on the page 24 shows the addressing sequence for each burst length using them. Both sequences support bursts of 1, 2, 4 and 8. Additionally, sequential sequence supports the full page length.

7. Mode Register



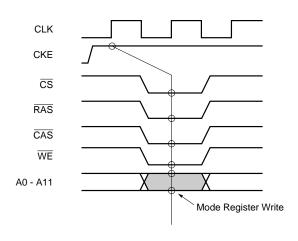
Remark R: Reserved

110

111

R R

Mode Register Write Timing





7.1 Burst Length and Sequence

[Burst of Two]

Starting Address (column	Sequential Addressing	Interleave Addressing		
address A0, binary)	Sequence (decimal)	Sequence (decimal)		
0	0, 1	0, 1		
1	1, 0	1, 0		

[Burst of Four]

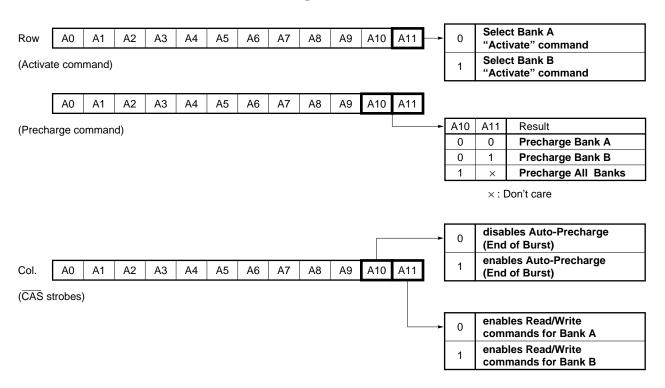
Starting Address (column	Sequential Addressing	Interleave Addressing
address A1 - A0, binary)	Sequence (decimal)	Sequence (decimal)
00	0, 1, 2, 3	0, 1, 2, 3
01	1, 2, 3, 0	1, 0, 3, 2
10	2, 3, 0, 1	2, 3, 0, 1
11	3, 0, 1, 2	3, 2, 1, 0

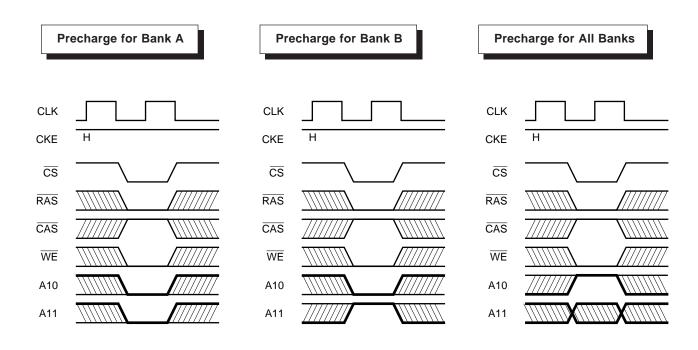
[Burst of Eight]

Starting Address (column	Sequential Addressing	Interleave Addressing
address A2 - A0, binary)	Sequence (decimal)	Sequence (decimal)
000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

Full page burst is an extension of the above tables of Sequential Addressing, with the length being 512 (for 2 M \times 8 device), 1,024 (for 4 M \times 4 device) and 256 (for 1 M \times 16 device).

8. Address Bits of Bank-Select and Precharge





9. Precharge

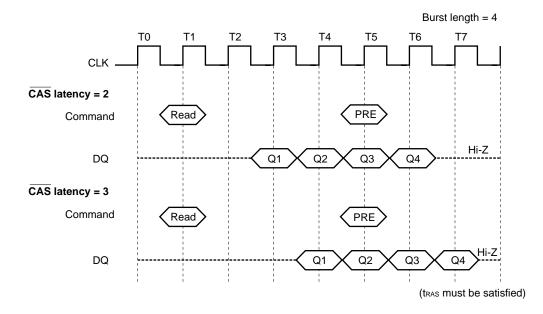
The precharge command can be issued anytime after tras(MIN.) is satisfied.

Soon after the precharge command is issued, precharge operation performed and the synchronous DRAM enters the idle state after trp is satisfied. The parameter trp is the time required to perform the precharge.

The earliest timing in a read cycle that a precharge command can be issued without losing any data in the burst is as follows.

CAS latency = 2: One clock earlier than the last read data.

CAS latency = 3: Two clocks earlier than the last read data.



In order to write all data to the memory cell correctly, the asynchronous parameter "tdpl" must be satisfied. The tdpl(MIN.) specification defines the earliest time that a precharge command can be issued. Minimum number of clocks are calculated by dividing tdpl (MIN.) with clock cycle time.

In summary, the precharge command can be issued relative to reference clock that indicates the last data word is valid. In the following table, minus means clocks before the reference; plus means time after the reference.

CAS latency	Read	Write
2	-1	+tdpl (MIN.)
3	-2	+tDPL (MIN.)

10. Auto Precharge

During a read or write command cycle, A10 controls whether auto precharge is selected. A10 high in the Read or Write command (Read with Auto precharge command or Write with Auto precharge command), auto precharge is selected and precharge begins automatically.

The tras must be satisfied with a read with auto precharge or a write with auto precharge operation. In addition, the next activate command to the bank being precharged cannot be executed until the precharge cycle ends.

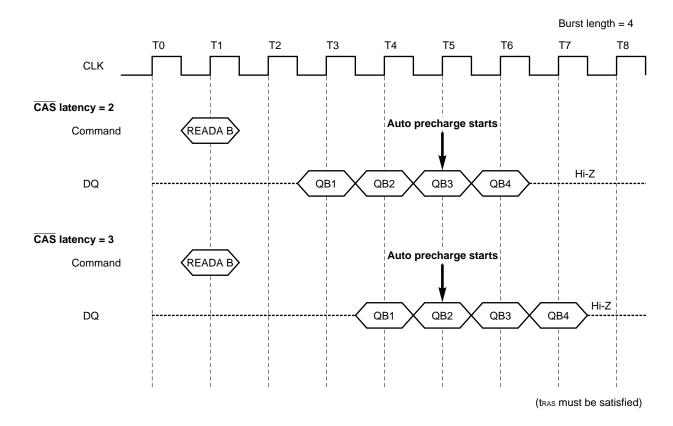
In read cycle, once auto precharge has started, an activate command to the bank can be issued after tRP has been satisfied.

In write cycle, the tDAL must be satisfied to issue the next activate command to the bank being precharged.

The timing that begins the auto precharge cycle depends on both the $\overline{\text{CAS}}$ latency programmed into the mode register and whether read or write cycle.

10.1 Read with Auto Precharge

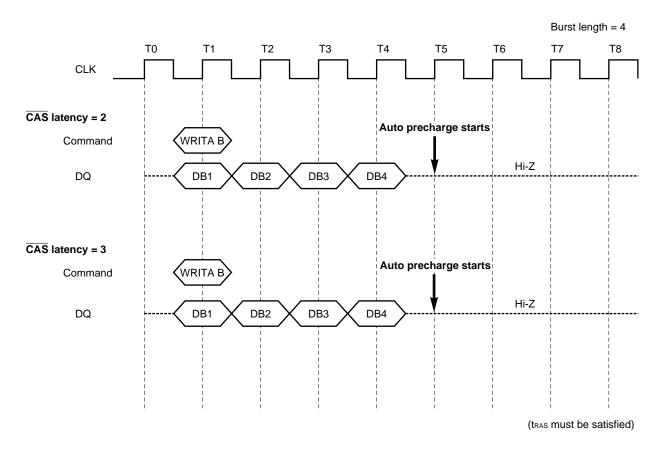
During a read cycle, the auto precharge begins one clock earlier (\overline{CAS} latency of 2) or two clocks earlier (\overline{CAS} latency of 3) the last data word output.



Remark READA means Read with Auto precharge

10.2 Write with Auto Precharge

During a write cycle, the auto precharge begins one clock after the last data word input to the device (\overline{CAS} latency of 2 or 3).



Remark WRITA means Write with Auto precharge

In summary, the auto precharge cycle begins relative to a reference clock that indicates the last data word is valid. In the table below, minus means clocks before the reference; plus means clocks after the reference.

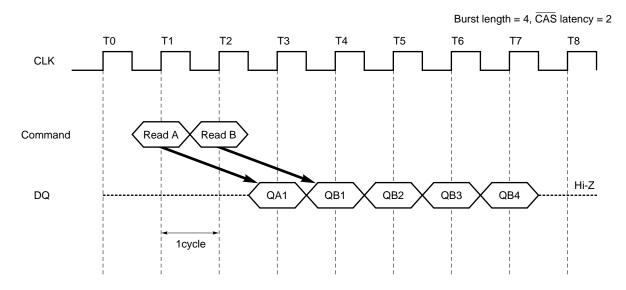
CAS latency	Read	Write					
2	-1	+1					
3	-2	+1					

11. Read/Write Command Interval

11.1 Read to Read Command Interval

During a read cycle, when new Read command is issued, it will be effective after $\overline{\text{CAS}}$ latency, even if the previous READ operation does not completed. READ will be interrupted by another READ.

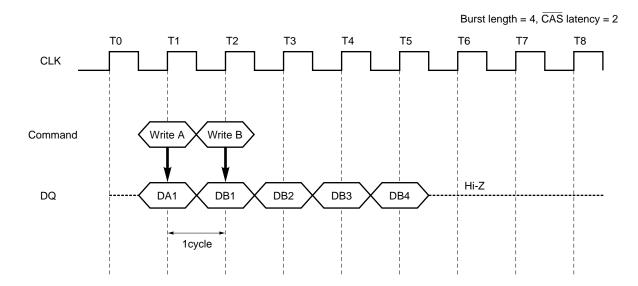
The interval between the commands is 1 cycle minimum. Each Read command can be issued in every clock without any restriction.



11.2 Write to Write Command Interval

During a write cycle, when new Write command is issued, the previous burst will terminate and the new burst will begin with a new Write command. WRITE will be interrupted by another WRITE.

The interval between the commands is minimum 1. Each Write command can be issued in every clock without any restriction.



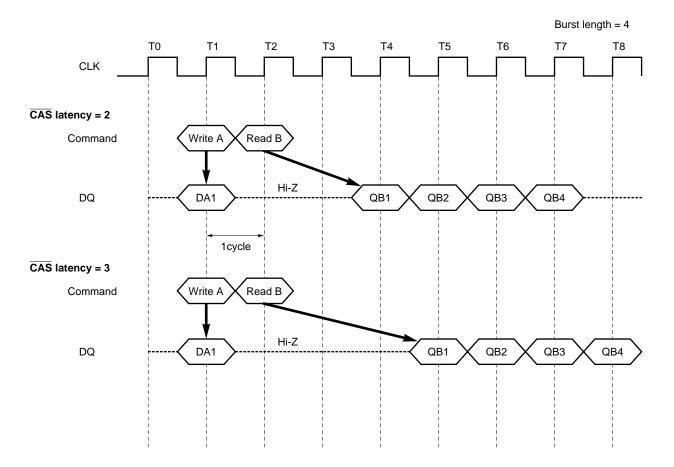


11.3 Write to Read Command Interval

Write command and Read command interval is also 1 cycle.

Only the write data before Read command will be written.

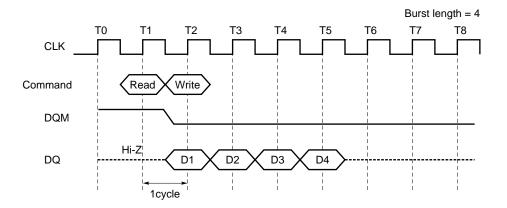
The data bus must be Hi-Z at least one cycle prior to the first Dout.



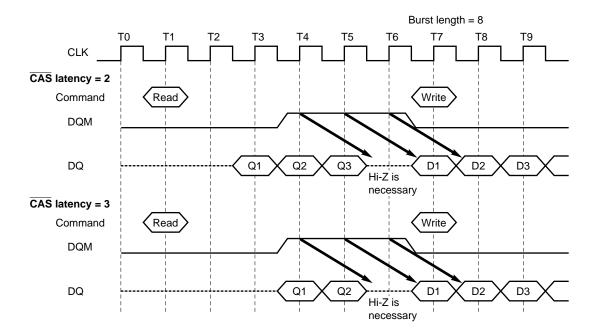
11.4 Read to Write Command Interval

During a read cycle, READ can be interrupted by WRITE.

The Read and Write command interval is 1 cycle minimum. There is a restriction to avoid data conflict. The data bus must be Hi-Z using DQM before WRITE.



READ can be interrupted by WRITE. DQM must be High at least 3 clocks prior to the Write command.



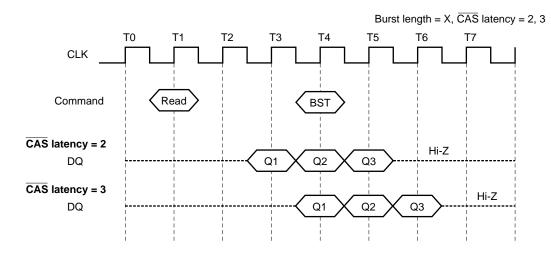


12. Burst Termination

There are two methods to terminate a burst operation other than using a Read or a Write command. One is the burst stop command and the other is the precharge command.

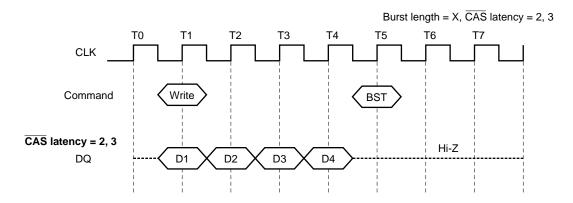
12.1 Burst Stop Command

During a read cycle, when the burst stop command is issued, the burst read data are terminated and the data bus goes to Hi-Z after the $\overline{\text{CAS}}$ latency from the burst stop command.



Remark BST: Burst stop command

During a write cycle, when the burst stop command is issued, the burst write data are terminated and data bus goes to Hi-Z at the same clock with the burst stop command.



Remark BST: Burst stop command

12.2 Precharge Termination

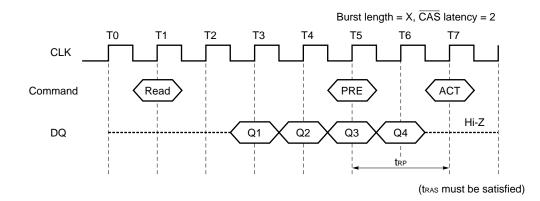
12.2.1 Precharge Termination in READ Cycle

During a read cycle, the burst read operation is terminated by a precharge command.

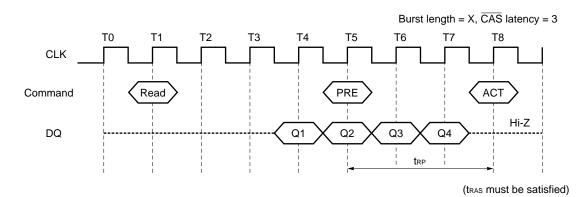
When the precharge command is issued, the burst read operation is terminated and precharge starts.

The same bank can be activated again after tRP from the precharge command.

When CAS latency is 2, the read data will remain valid until one clock after the precharge command.



When CAS latency is 3, the read data will remain valid until two clocks after the precharge command.



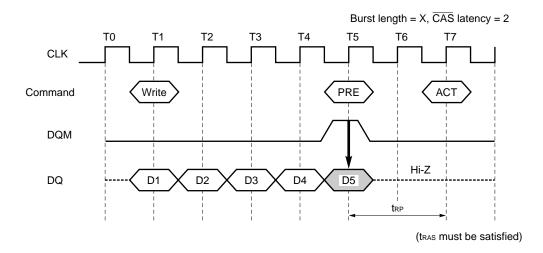
12.2.2 Precharge Termination in WRITE Cycle

During a write cycle, the burst write operation is terminated by a precharge command.

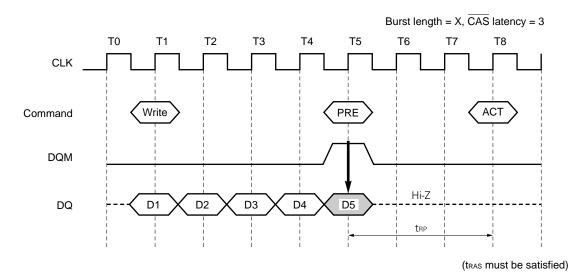
When the precharge command is issued, the burst write operation is terminated and precharge starts.

The same bank can be activated again after tRP from the precharge command.

When \overline{CAS} latency is 2, the write data written prior to the precharge command will be correctly stored. However, invalid data may be written at the same clock as the precharge command. To prevent this from happening, DQM must be high at the same clock as the precharge command. This will mask the invalid data.



When $\overline{\text{CAS}}$ latency is 3, the write data written prior to the precharge command will be correctly stored. However, invalid data may be written at the same clock as the precharge command. To prevent this from happening, DQM must be high at the same clock as the precharge command. This will mask the invalid data.



13. Electrical Specifications

- All voltage are referenced to Vss (GND).
- After power up, wait more than 100 μs and then, execute **Power on sequence and Auto Refresh** before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	Vcc, VccQ		-1.0 to +4.6	V
Voltage on input pin relative to GND	VT		-1.0 to +4.6	V
Short circuit output current	lo		50	mA
Power dissipation	Pp		1	W
Operating ambient temperature	TA		0 to +70	°C
Storage temperature	Tstg		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	Vcc		3.0	3.3	3.6	V
High level input voltage	Vih		2.0		Vcc + 0.3 ^{Note 1}	V
Low level input voltage	VIL		-0.3Note 2		+0.8	V
Operating ambient temperature	TA		0		70	°C

Notes 1. Vih (MAX.) = Vcc + 2.0 V (Pulse width $\leq 3 ns$)

2. V_{IL} (MIN.) = -2.0 V (Pulse width ≤ 3 ns)

Capacitance ($T_A = 25$ °C, f = 1 MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	Cıı	A0 to A11	2.5		4	pF
	C ₁₂	CLK, CKE, CS, RAS, CAS, WE, DQM, UDQM, LDQM	2.5		4	pF
Data input/output capacitance	C _{I/O}	DQ0 to DQ15	4		6	pF



DC Characteristics 1 (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Symbol Test condition	CAS	Grade	Ма	aximu	Linit	Notos	
Farameter	Symbol	rest condition	latency	Grade	×4	×8	×16	Unit	Notes
Operating current	Icc1	Burst length=1	CL = 2	-80		105			
		trc ≥ trc (MIN.)		-10	100	105	110	-	
		lo = 0 mA		-10B	85	90	95		
		One bank active		-12	85	90	95		1
			CL = 3	-80	110	115	120	mA	'
				-10	110	115	120		
				-10B	90	95	100		
				-12	90	95	100		
Precharge standby current	Icc2P	CKE ≤ VIL (MAX.) tck = 15 ns	I	1	3	3	3		
in Power down mode	Icc2PS	CKE ≤ VIL (MAX.) tck = ∞			2	2	2	mA	
Precharge standby current	Icc2N	CKE ≥ Vih (Min.) tck = 15 ns			25	25	25		
in Non power down mode		CS ≥ VIH (MIN.)							
		Input signals are changed one time during 30	ns.					mA	
	Icc2NS	CKE ≥ ViH (MIN.) tck = ∞			6	6	6		
	ļ. <u>-</u>	Input signals are stable.			_	_	_		-
Active standby current in Power down mode	ІссзР	CKE ≤ VIL (MAX.) tck = 15 ns			3	3	3	mA	
Tower down mode	IccзPS	CKE ≤ VIL (MAX.) tck = ∞			2	2	2		
Active standby current	ІссзN	$\frac{\text{CKE} \ge \text{ViH (MIN.) tck} = 15 \text{ ns}}{2.00 \text{ s. Vid}}$				28	30		
in Non power down mode		CS ≥ V _{IH (MIN.)} Input signals are changed one time during 30 ns.						mA	
	Icc3NS	CKE ≥ ViH (MIN.) tck = ∞				12	15		
	ICC3IVO	Input signals are stable.			12 12 15				
Operating current	Icc4	$tck \ge tck \text{ (MIN.)}$ $Io = 0 \text{ mA}$ All banks active	CL = 2	-80	95	105	110	90	
(Burst mode)				-10	75	85	90		
				-10B	75		90		
				-12		75	80		
			CL = 3	-80		120		mA	2
			OL = 3	-10		100			
								ł	
				-10B		100		-	
Defined accuracy		400	01 0	-12		90	95		
Refresh current	Iccs	trc = 100 ns tcк = MIN.	CL = 2	-80	90		90	mA	3
		ter – Willy.		-10	90		90		
				-10B	90	90	90		
				-12	90	90	90		
			CL = 3	-80	90	90	90		
				-10	90	90	90		
				-10B	90	90	90		
				-12	90	90	90		
Self refresh Current	Icc6	CKE ≤ 0.2V		-**	1	1	1	mA	
				_**L	250	250	250	иΑ	1

- **Notes 1.** Icc1 depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, Icc1 is measured on condition that addresses are changed only one time during tck (MIN.).
 - 2. Icc4 depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, Icc4 is measured on condition that addresses are changed only one time during tck (MIN.).
 - 3. Iccs is measured on condition that addresses are changed only one time during tck (MIN.).

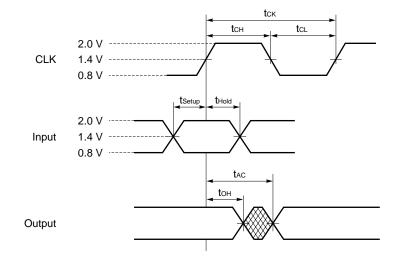
DC Characteristics 2 (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		TYP.	MAX.	Unit
Input leakage current	lı (L)	$0 \le V_1 \le V_{CC}$, $V_{CC}Q = V_{CC}$, all other pins not under test = 0 V	-1.0		+1.0	μΑ
Output leakage current	I _{O(L)}	Douт is disabled, 0 ≤ Vo ≤ VccQ	-1.5		+1.5	μΑ
High level output voltage	Vон	Io = -4 mA	2.4			V
Low level output voltage	Vol	Io = +4 mA			0.4	V

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

Test Conditions

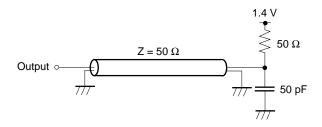
- AC measurements assume $t_T = 1$ ns.
- Reference level for measuring timing of input signals is 1.4 V. Transition times are measured between V_{IH} and V_{IL}.
- If tT is longer than 1 ns, reference level for measuring timing of input signals is VIH (MIN.) and VIL (MAX.).
- An access time is measured at 1.4 V.



Synchronous Characteristics

Parameter		Comple al	-80		-10		-10B		-12		Unit	Note
		Symbol	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Onit	Note
Clock cycle time	CAS latency = 3	tскз	8	(125 MHz)	10	(100 MHz)	10	(100 MHz)	12	(83 MHz)	ns	
	CAS latency = 2	tck2	10	(100 MHz)	13	(77 MHz)	13	(77 MHz)	15	(67 MHz)	ns	
Access time from	CAS latency = 3	t _{AC3}		6		6		7		8	ns	1
CLK	CAS latency = 2	t _{AC2}		6		8		8		8	ns	1
CLK high level width		tсн	3		3		3.5		4		ns	
CLK low level width	CLK low level width		3		3		3.5		4		ns	
Data-out hold time		tон	3		3		3		3		ns	1
Data-out low-imped	ance time	tız	0		0		0		0		ns	
Data-out high-	CAS latency = 3	t _{HZ3}	3	6	3	6	3	7	3	8	ns	
impedance time	CAS latency = 2	tHZ2	3	6	3	8	3	8	3	8	ns	
Data-in setup time		tos	2.0		2.0		2.5		3.0		ns	
Data-in hold time		tон	1.0		1.0		1.0		1.5		ns	
Address setup time		tas	2.0		2.0		2.5		3.0		ns	
Address hold time		t AH	1.0		1.0		1.0		1.5		ns	
CKE setup time		t cks	2.0		2.0		2.5		3.0		ns	
CKE hold time	CKE hold time		1.0		1.0		1.0		1.5		ns	
CKE setup time (Power down exit)		tcksp	2.0		2.0		2.5		3.0		ns	
Command (CS, RAS, CAS, WE, DQM) setup time		tсмs	2.0		2.0		2.5		3.0		ns	
Command (CS, RAS, CAS, WE, DQM) hold time		tсмн	1.0		1.0		1.0		1.5		ns	

Notes 1. Output load



*

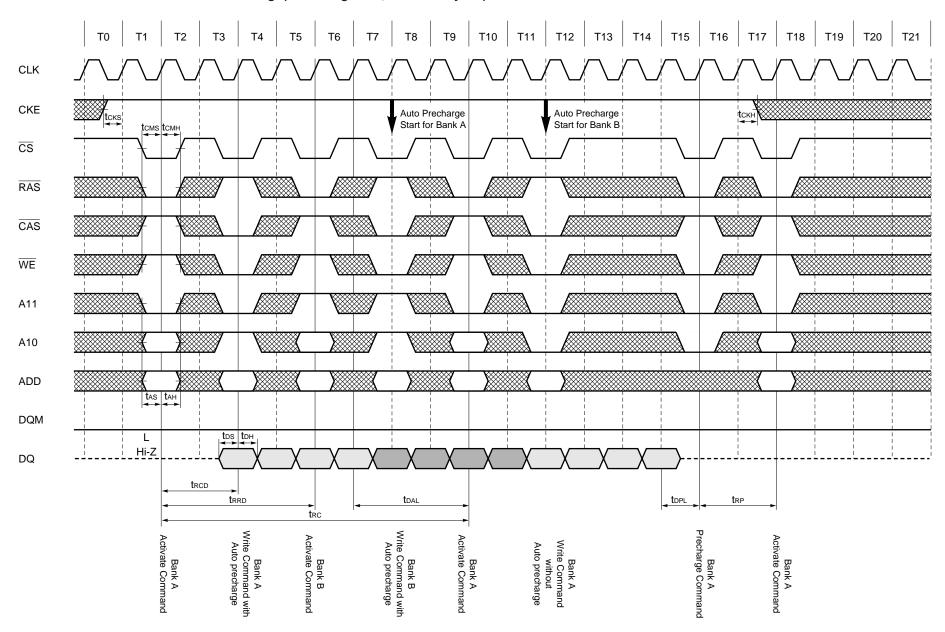
39

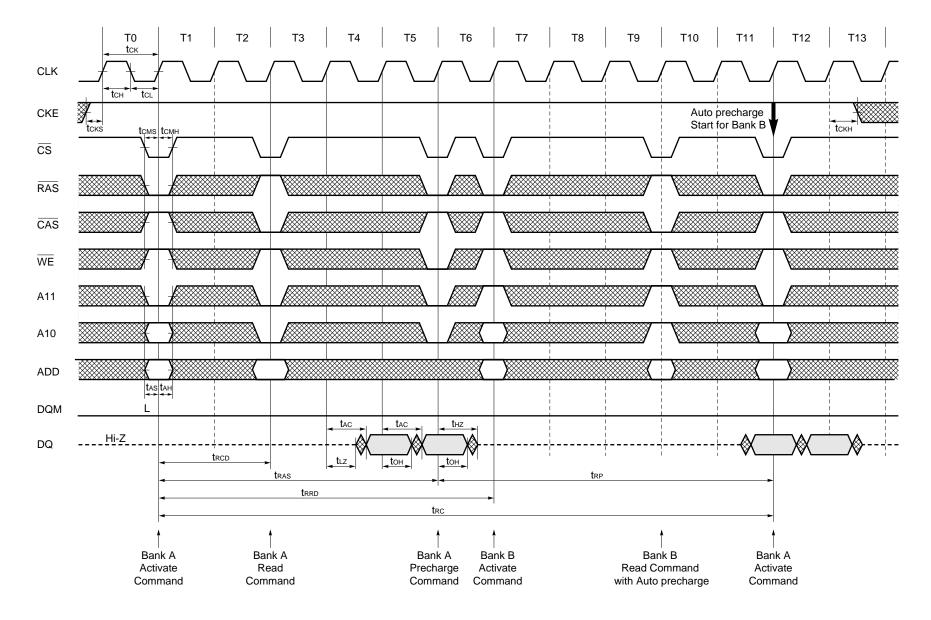


Asynchronous Characteristics

Parameter		0	-80		-10		-10B		-12		11.2	Nista
		Symbol	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Unit	Note
REF to REF/ACT Command period		trc	70		70		90		90		ns	
ACT to PRE Command period		tras	48	120,000	50	120,000	60	120,000	60	120,000	ns	
PRE to ACT Command period		trp	20		20		26		30		ns	
Delay time ACT to READ/WRITE Command		trcd	20		20		26		30		ns	
ACT(0) to ACT(1) Command period		trrd	16		20		20		24		ns	
Data-in to PRE Command period		t DPL	8		10		10		12		ns	
Data-in to ACT (REF)	CAS latency = 3	t _{DAL3}	1CLK + 20		1CLK + 20		1CLK + 26		1CLK + 30		ns	
Command (Auto precharge) period	CAS latency = 2	tDAL2	1CLK + 20		1CLK + 20		1CLK + 26		1CLK + 30		ns	
Mode register set cycle time		trsc	2		2		2		2		CLK	
Transition time		t⊤	0.5	30	1	30	1	30	1	30	ns	
Refresh time	_**	tref		32		32		32		32	ms	
	_**L			64		64		64		64	ms	

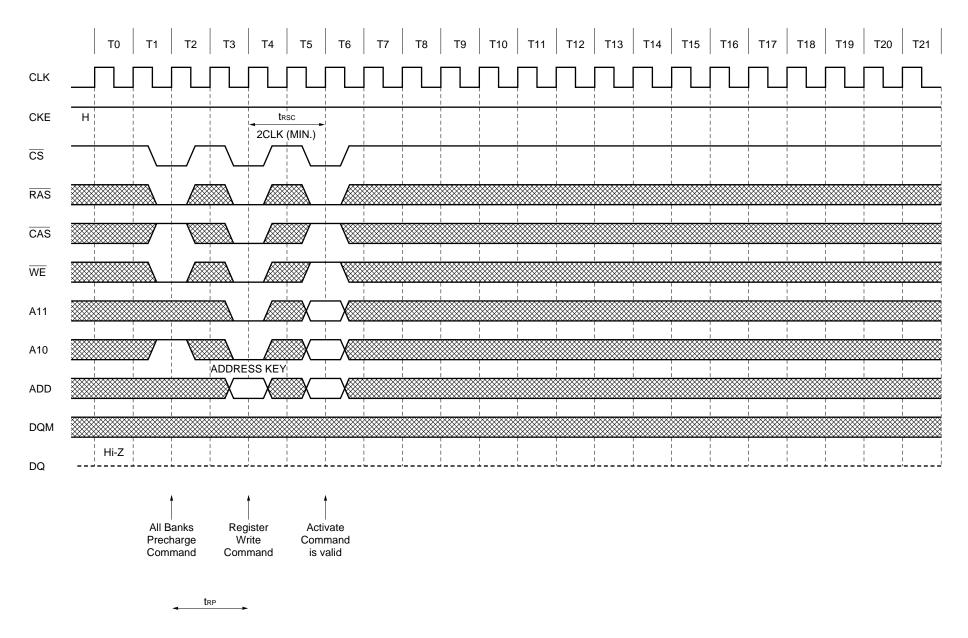
13.1 AC Parameters for Write Timing (Burst length = 4, \overline{CAS} latency = 2)



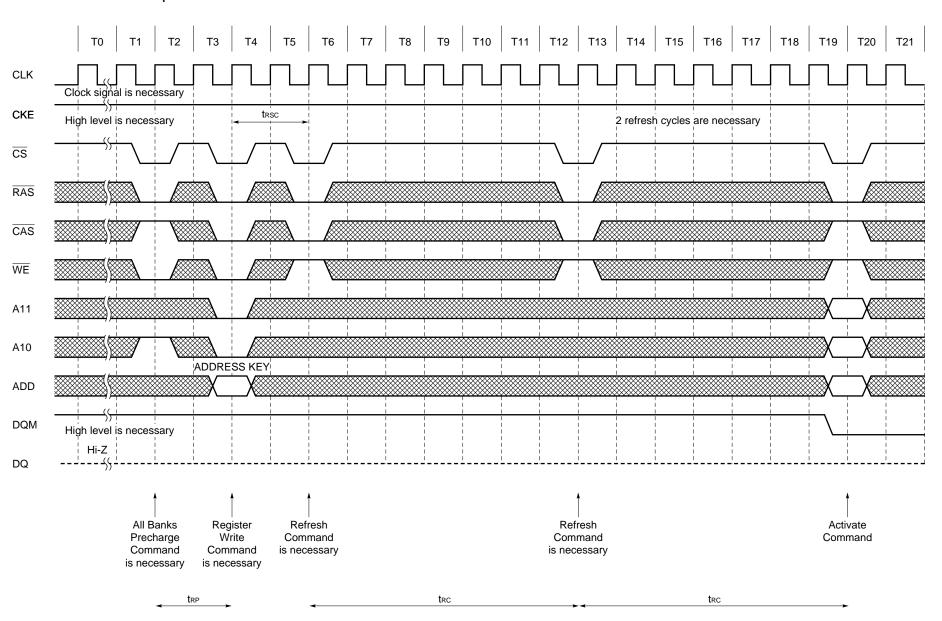


13.3 Relationship between Frequency and Latency

Speed version	-8	30	-10		-10B		-12	
Clock cycle time [ns]	8	10	10	13	10	13	12	15
Frequency [MHz]	125	100	100	77	100	77	83	67
CAS latency	3	2	3	2	3	2	3	2
[trcd]	3	2	2	2	3	2	3	2
RAS latency (CAS latency + [trcb])	6	4	5	4	6	4	6	4
[trc]	9	7	7	6	9	7	8	6
[tras]	6	5	5	4	6	5	5	4
[trrd]	2	2	2	2	2	2	2	2
[tre]	3	2	2	2	3	2	3	2
[topl]	1	1	1	1	1	1	1	1
[tdal]	4	3	3	3	4	3	4	3
[trsc]	2	2	2	2	2	2	2	2

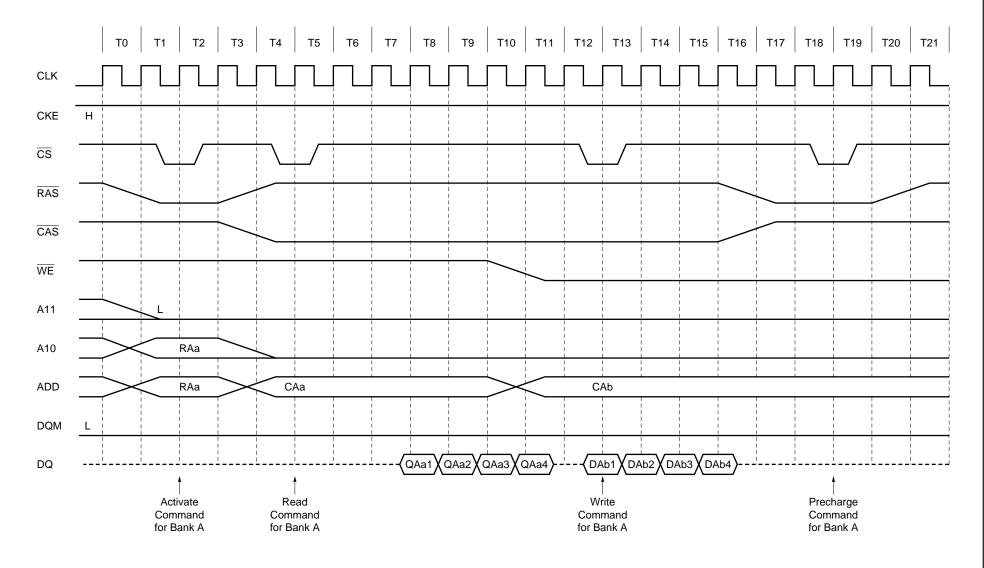


13.5 Power on Sequence and Auto Refresh

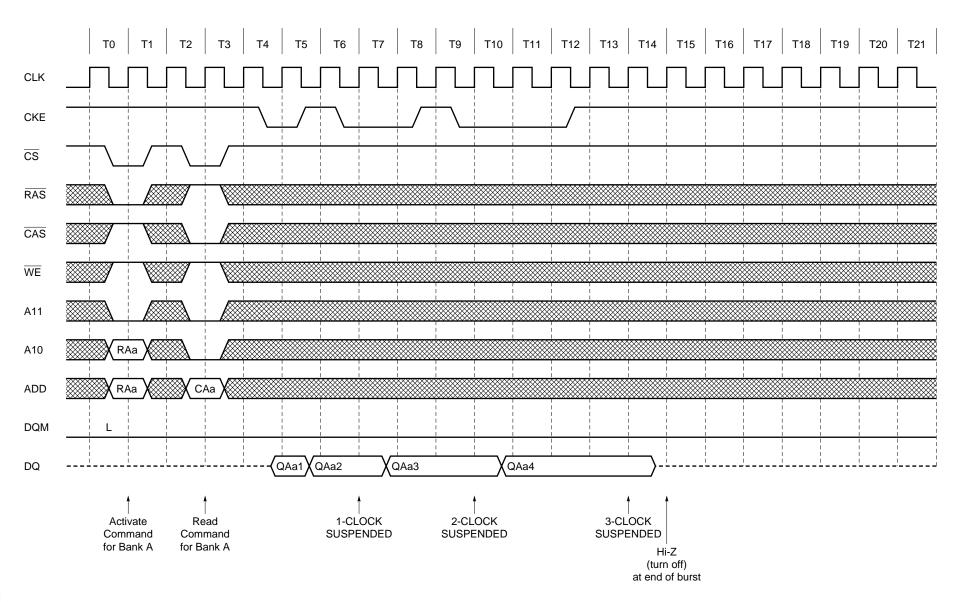


13.6 $\overline{\text{CS}}$ Function (at 100 MHz, Burst length = 4, $\overline{\text{CAS}}$ latency = 3)

Only $\overline{\text{CS}}$ signal needs to be issued at minimum rate

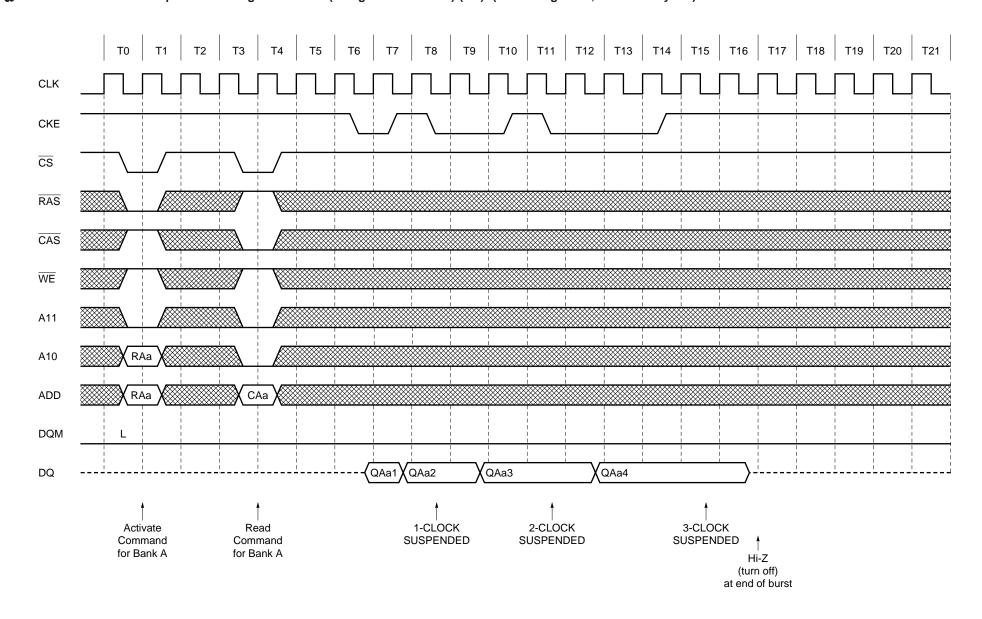


13.7 Clock Suspension during Burst Read (using CKE Function) (1/2) (Burst length = 4, CAS latency = 2)

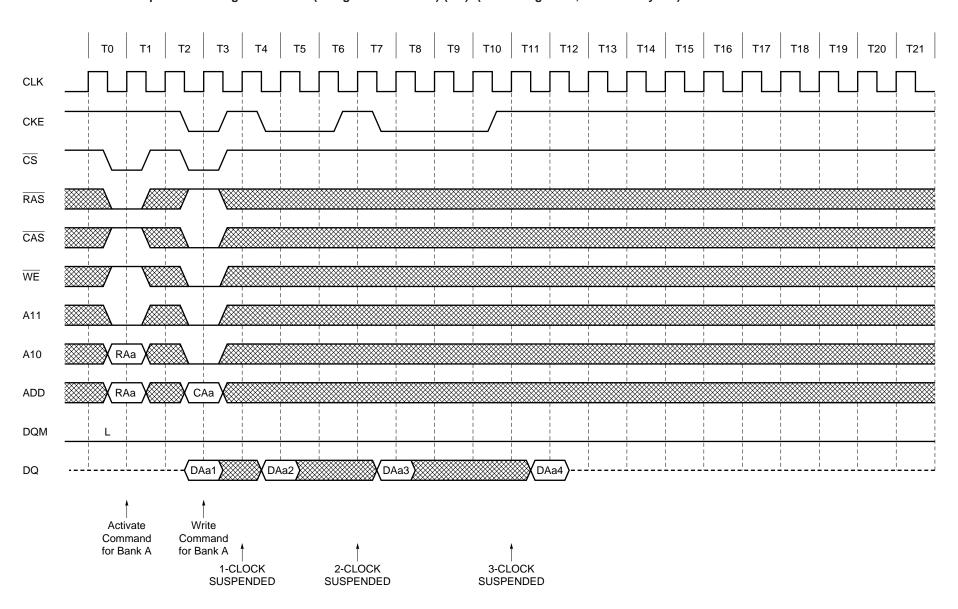


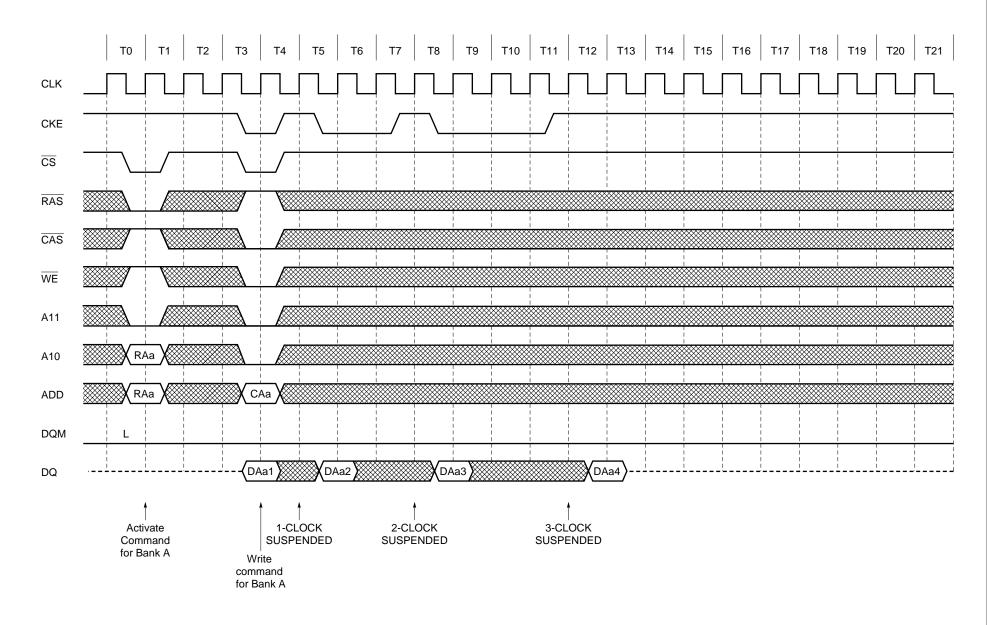
U

NEC

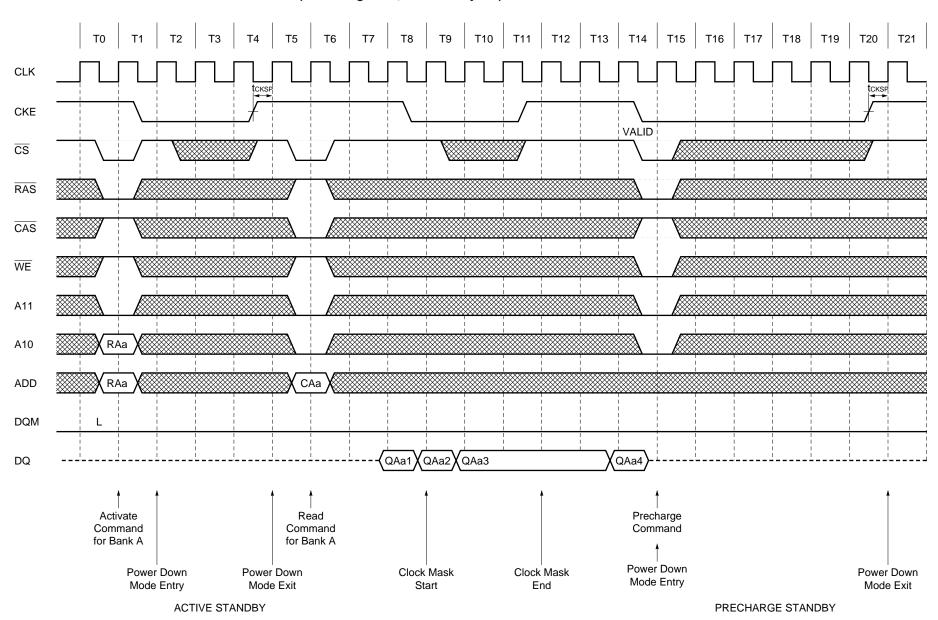


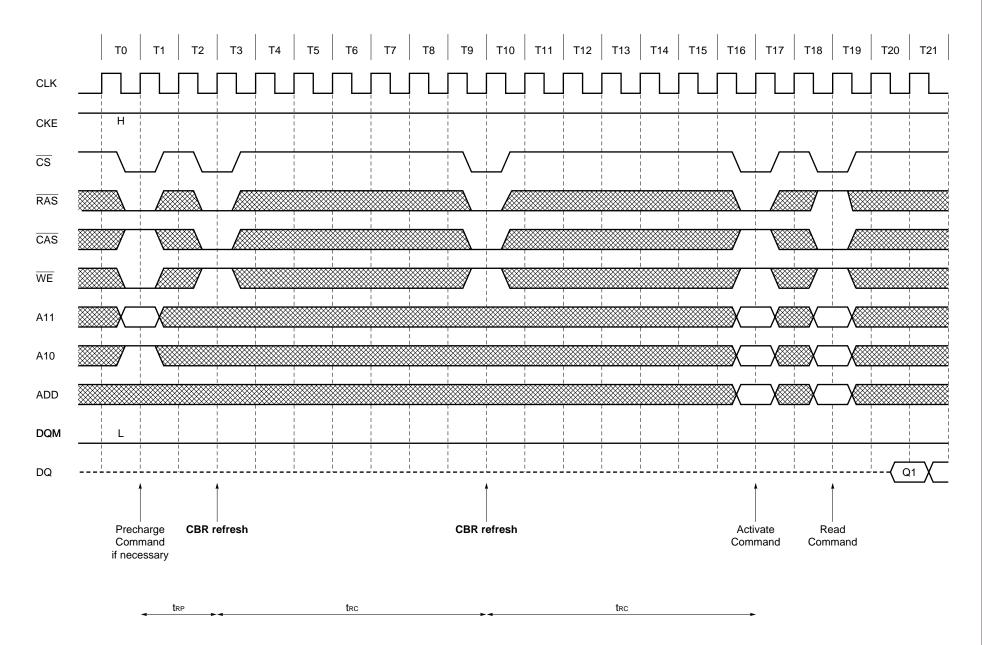
13.8 Clock Suspension during Burst Write (using CKE Function) (1/2) (Burst length = 4, CAS latency = 2)



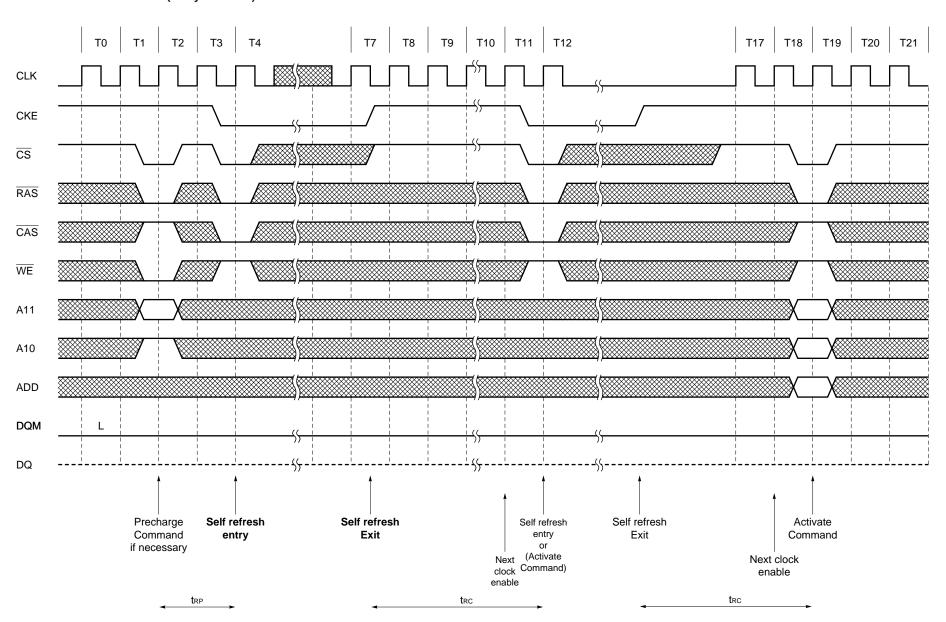


13.9 Power Down Mode and Clock Mask (Burst length = 4, CAS latency = 2)

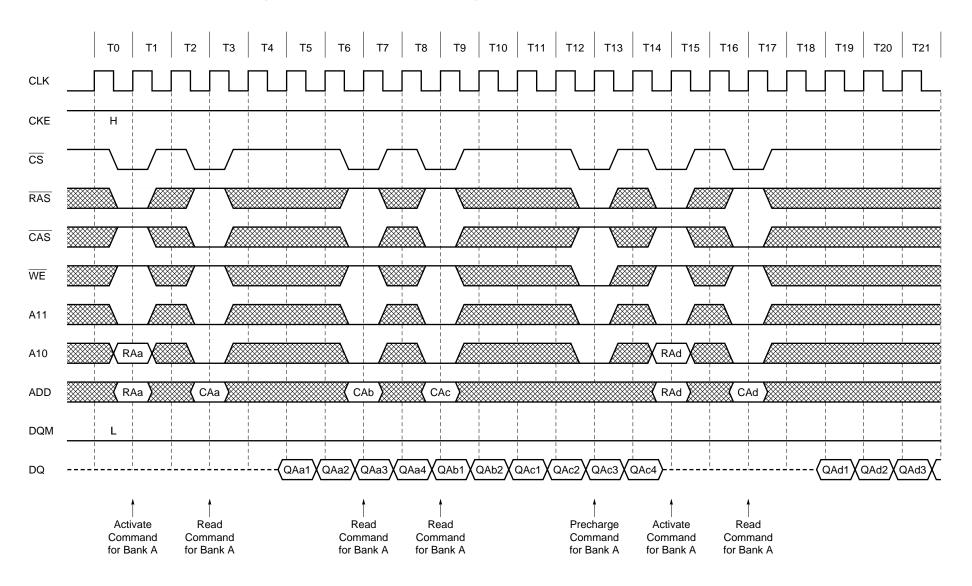




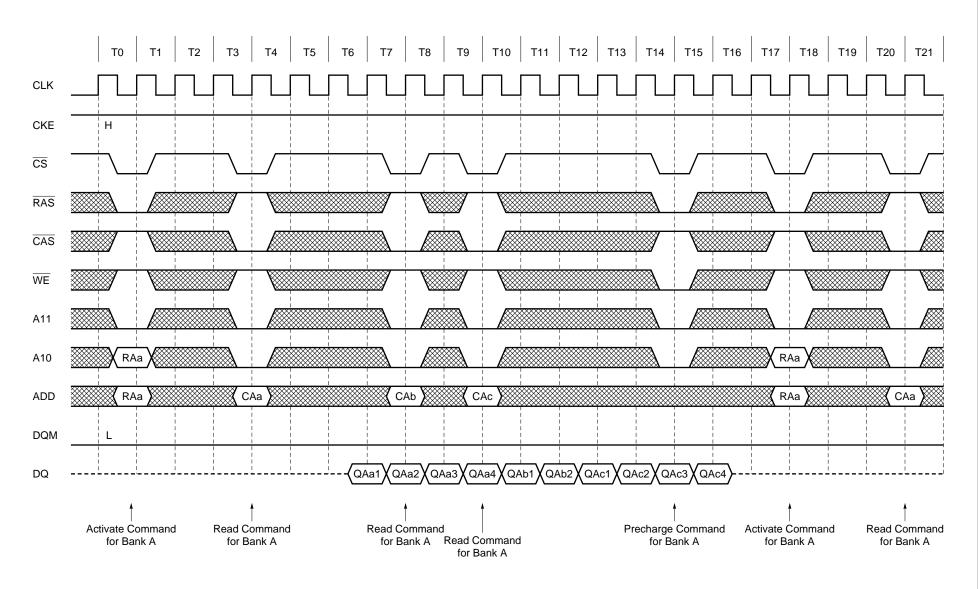
13.11 Self Refresh (entry and exit)

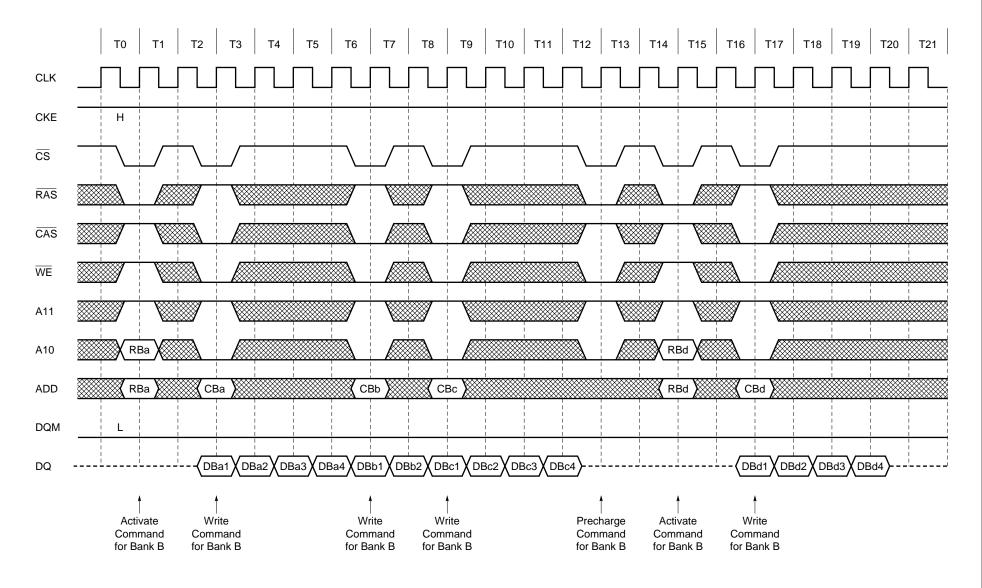


NEC

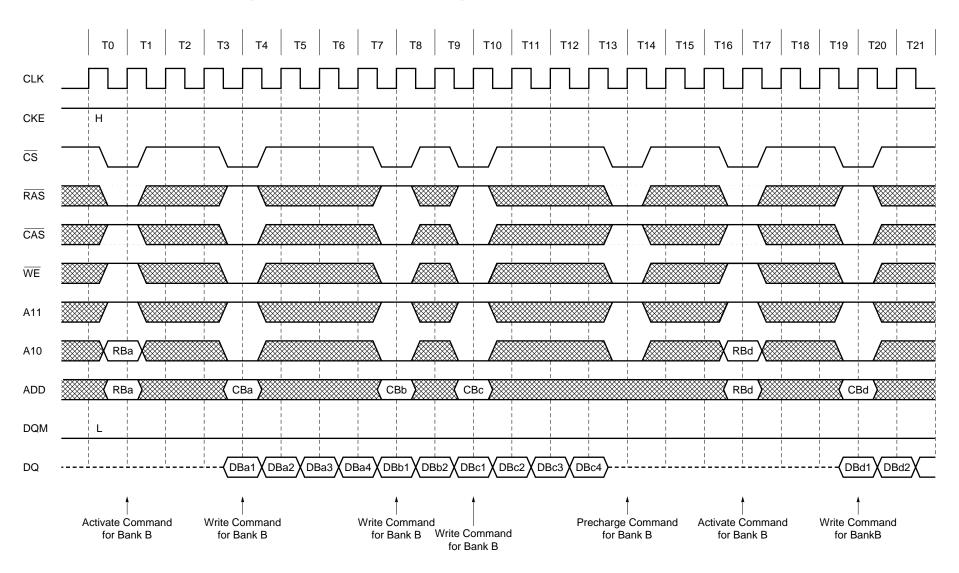


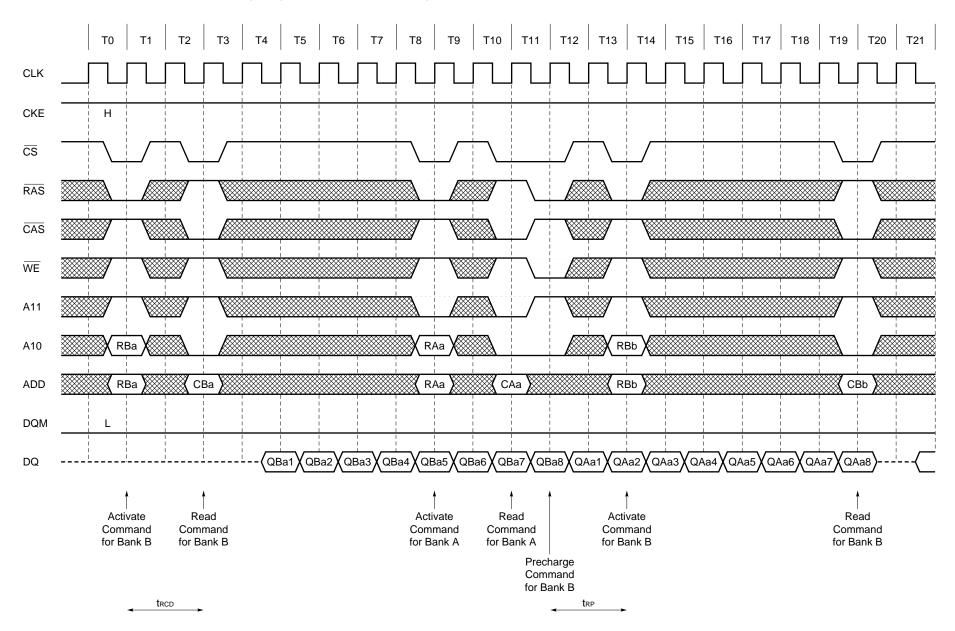
Random Column Read (Page with same bank) (2/2) (Burst length = 4, CAS latency = 3)



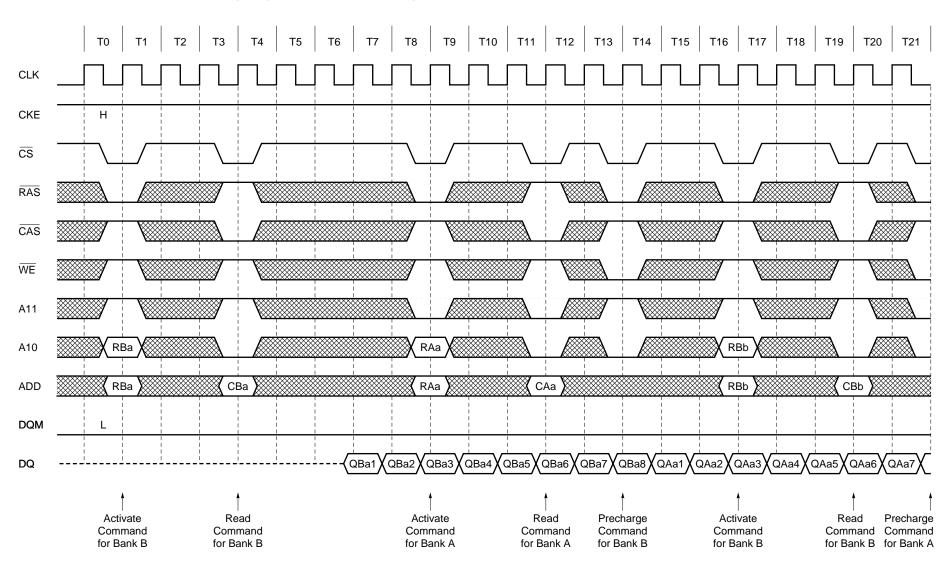


Random Column Write (Page with same bank) (2/2) (Burst length = 4, CAS latency = 3)



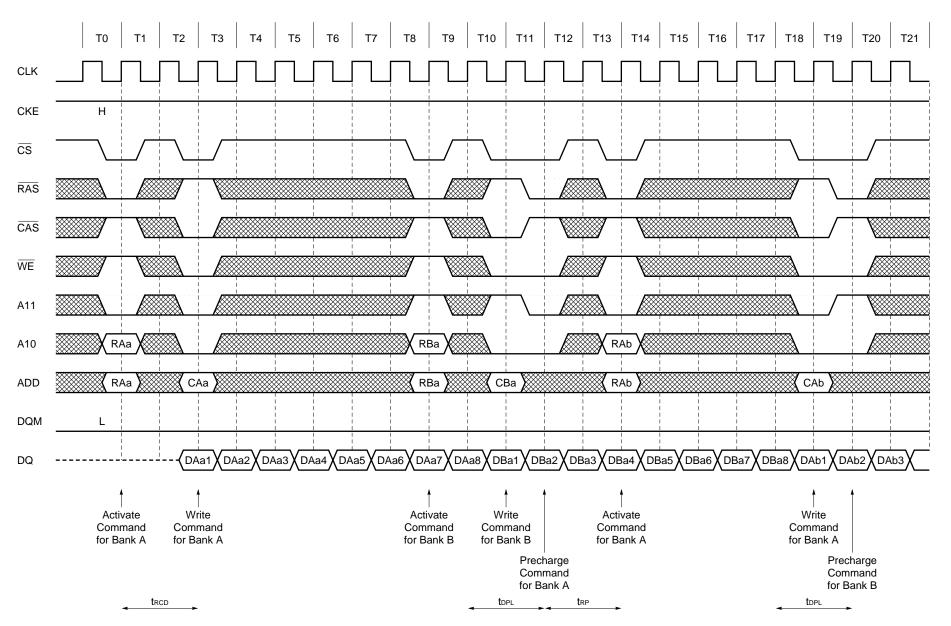


Random Row READ (Pingpong banks) (2/2) (Burst length = 8, CAS latency = 3)

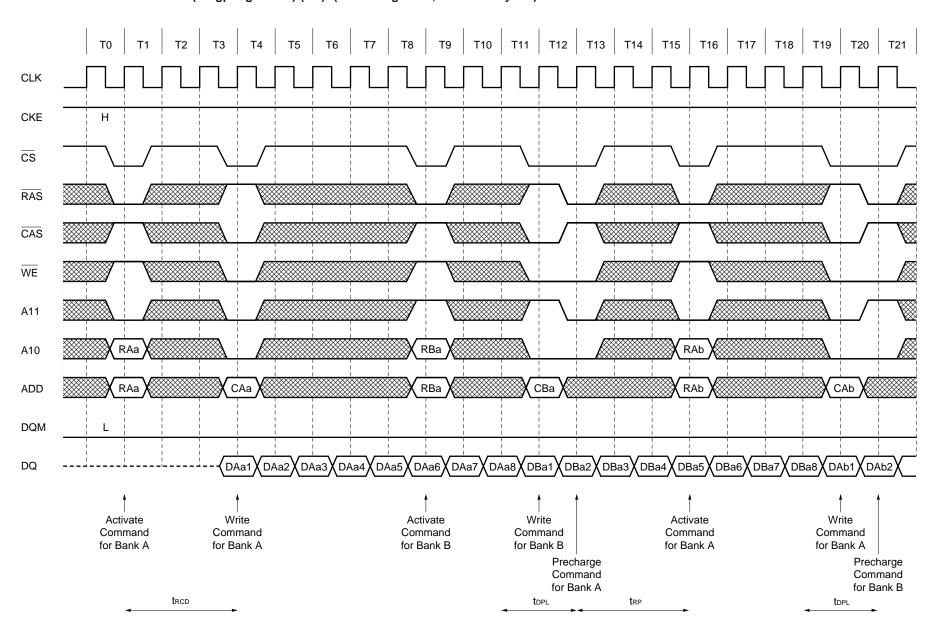


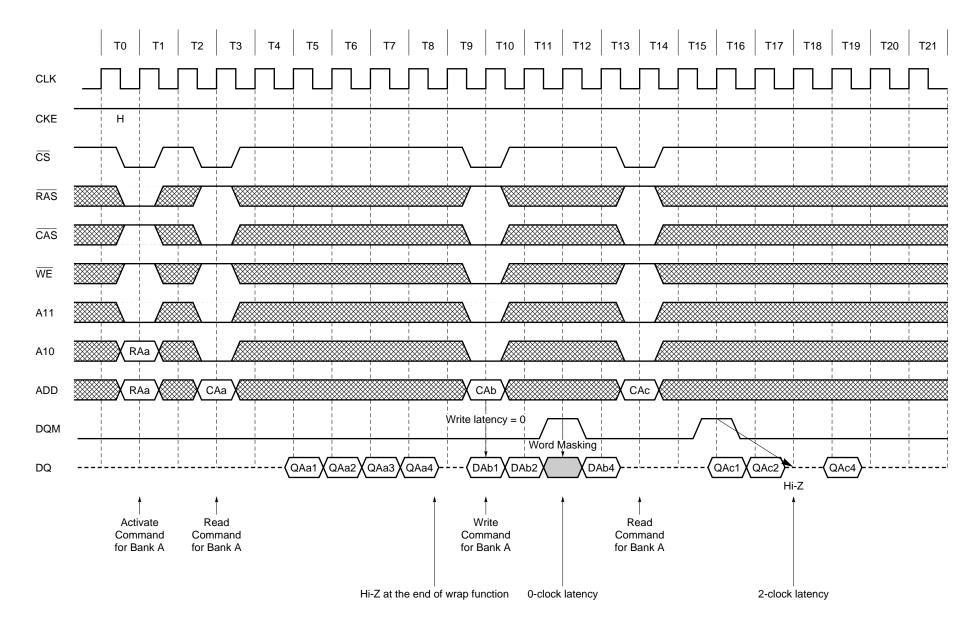
tRP

tRCD

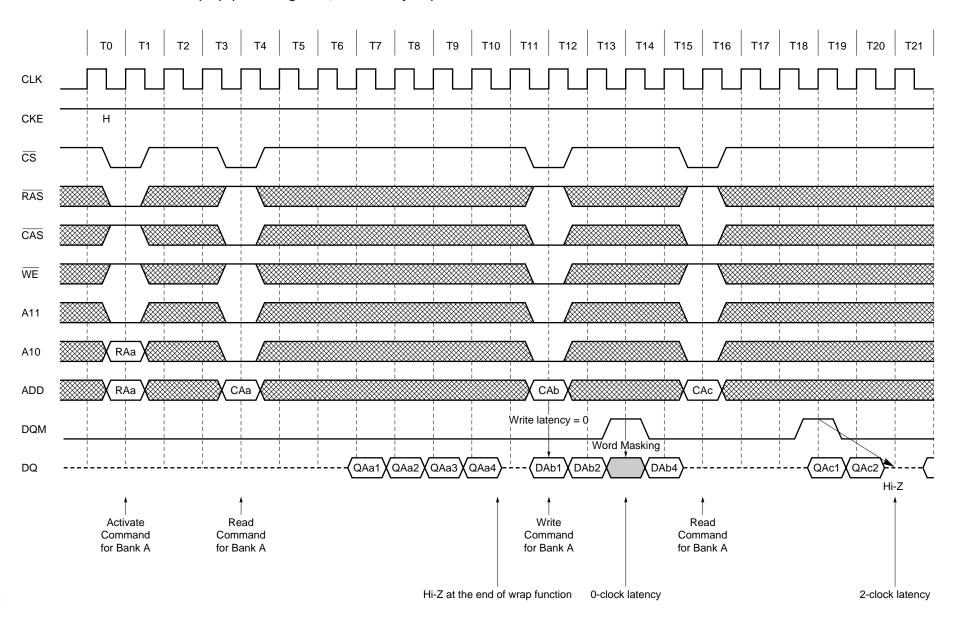


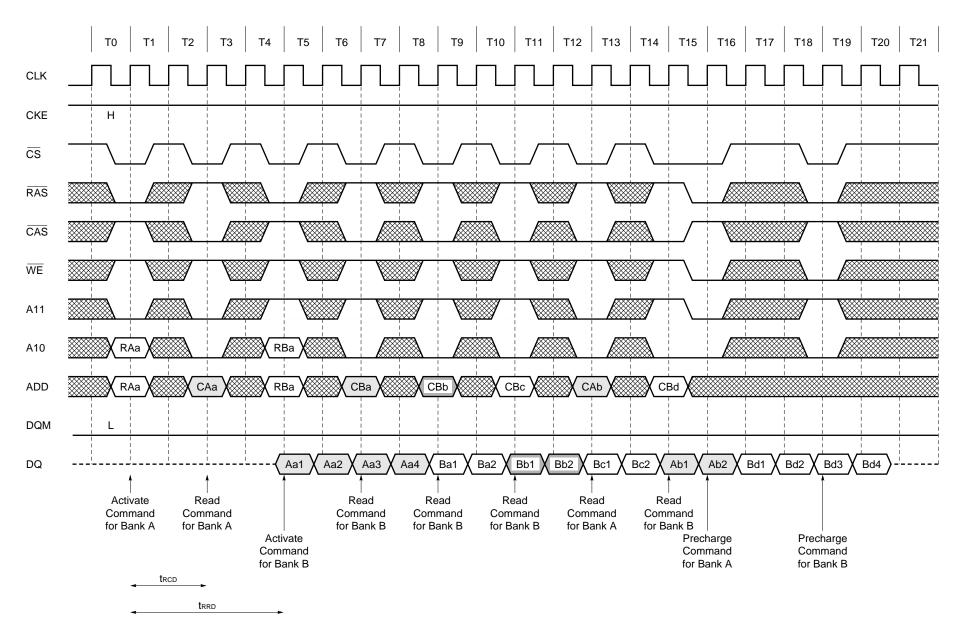
Random Row Write (Pingpong banks) (2/2) (Burst length = 8, CAS latency = 3)



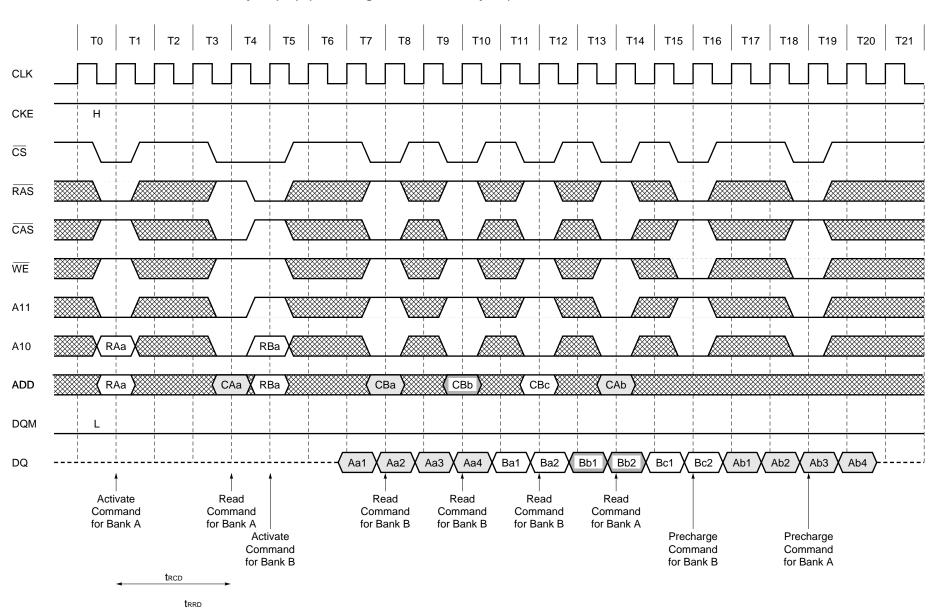


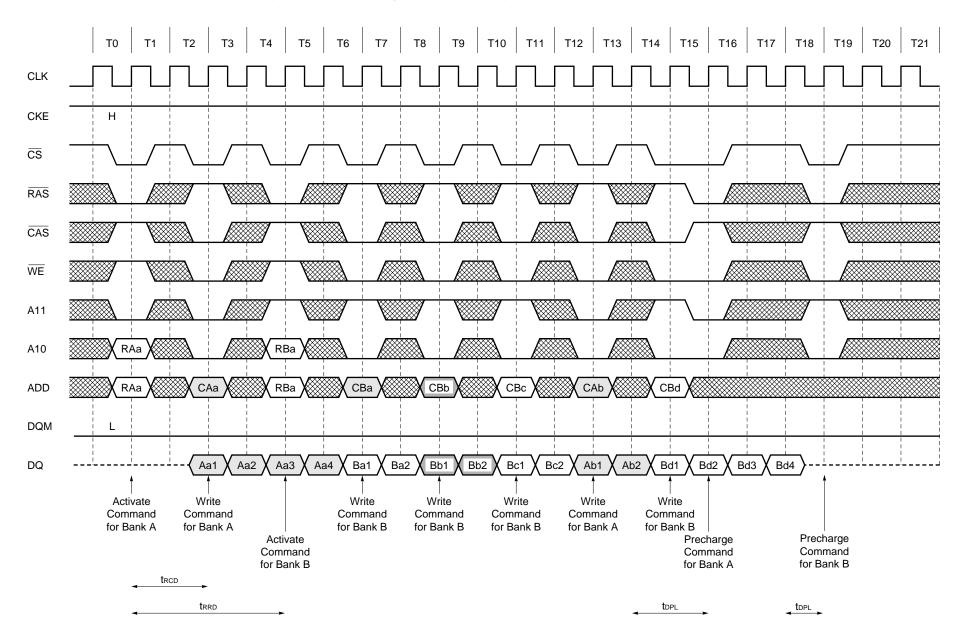
READ and WRITE (2/2) (Burst length = 4, \overline{CAS} latency = 3)



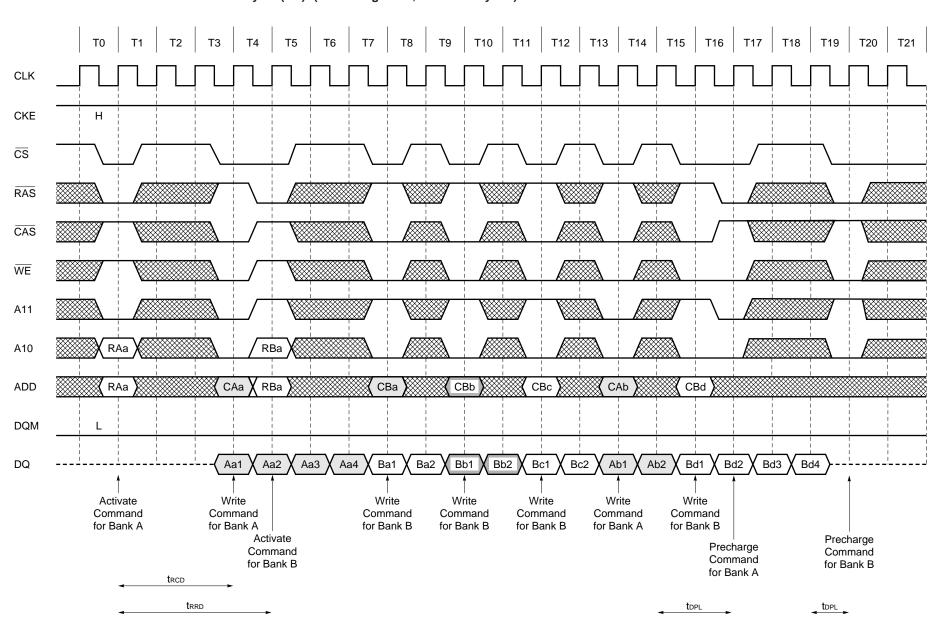


Interleaved Column READ Cycle (2/2) (Burst length = 4, CAS latency = 3)

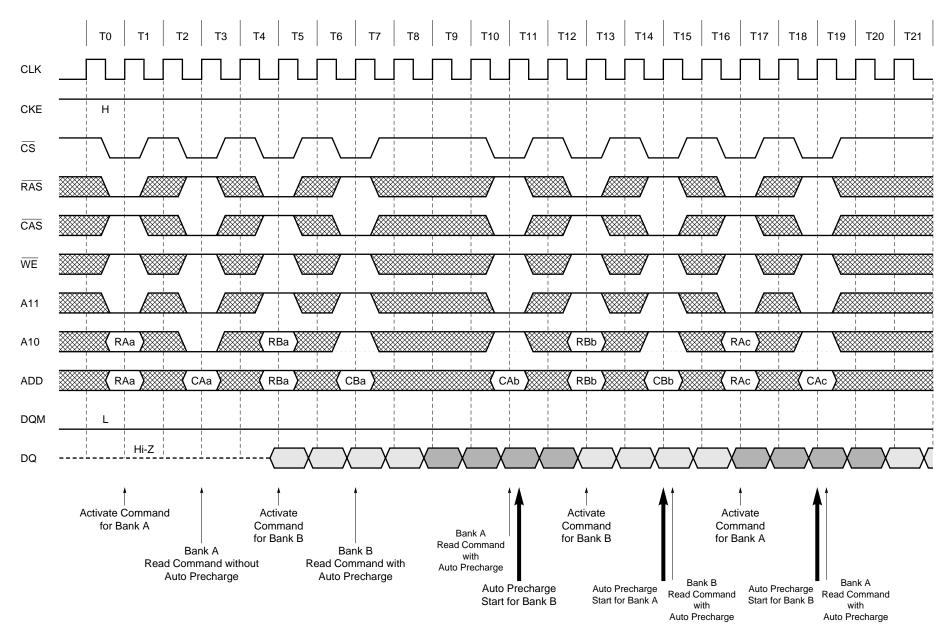




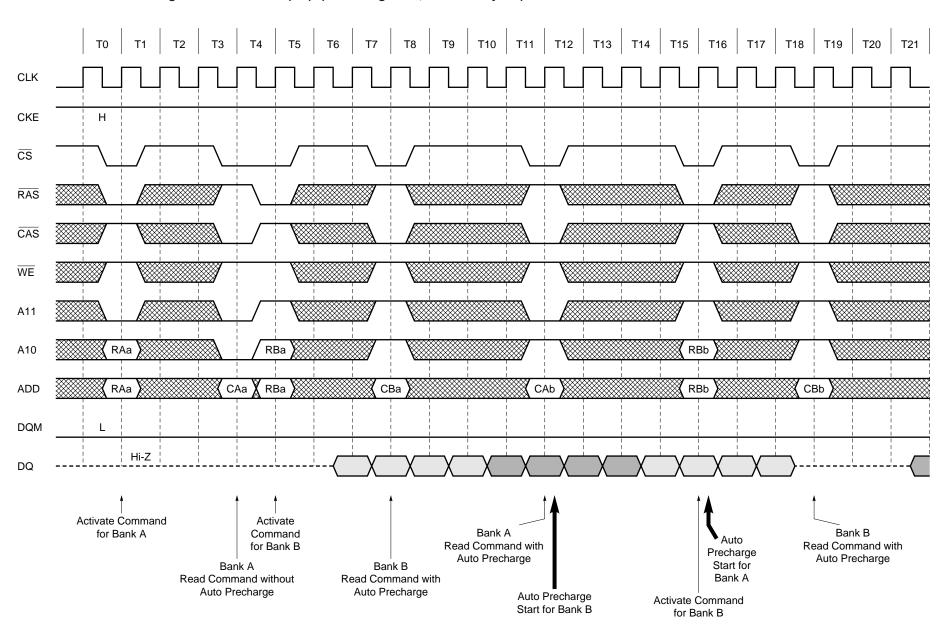
Interleaved Column WRITE Cycle (2/2) (Burst length = 4, CAS latency = 3)



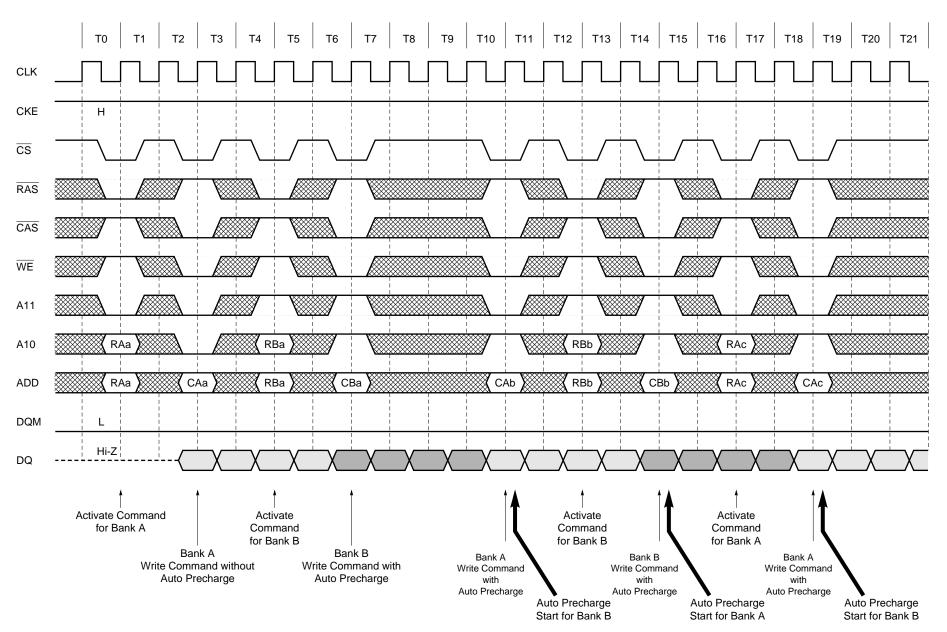
U



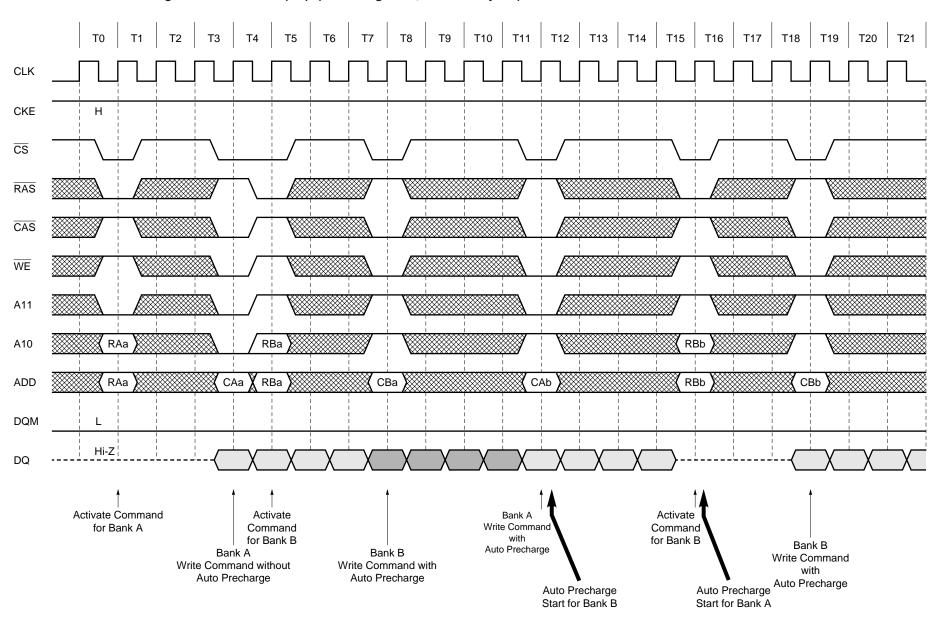
Auto Precharge after Read Burst (2/2) (Burst length = 4, CAS latency = 3)

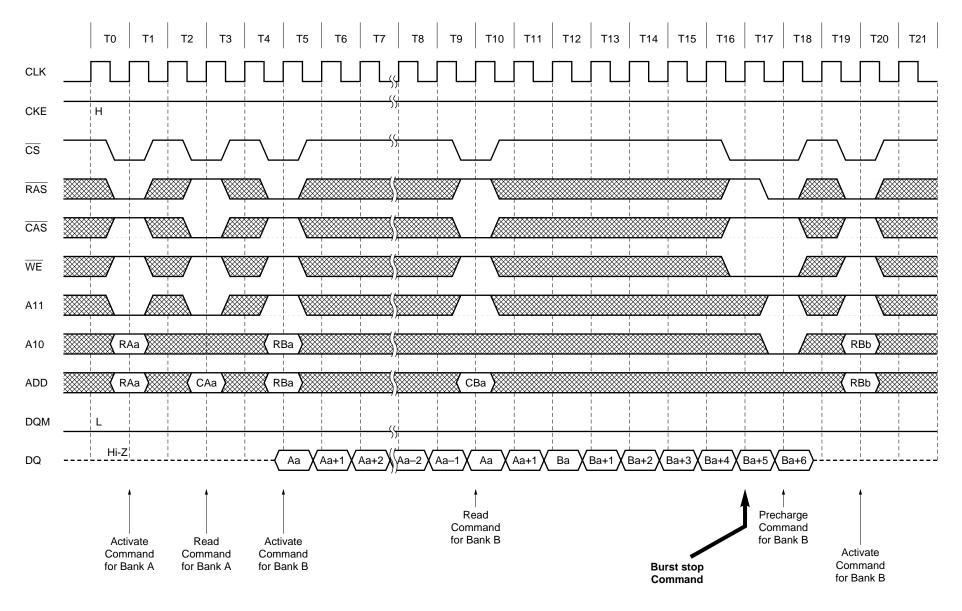


U

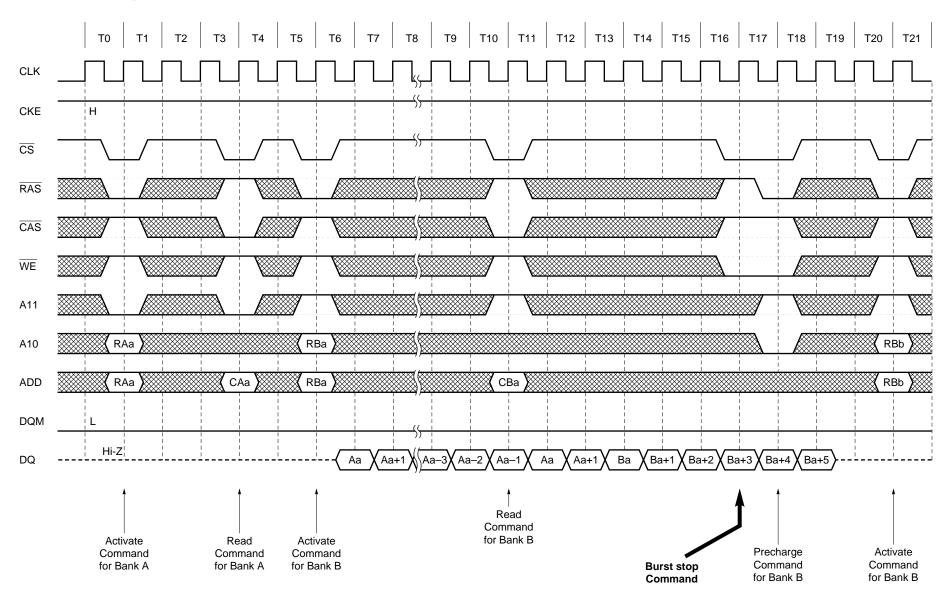


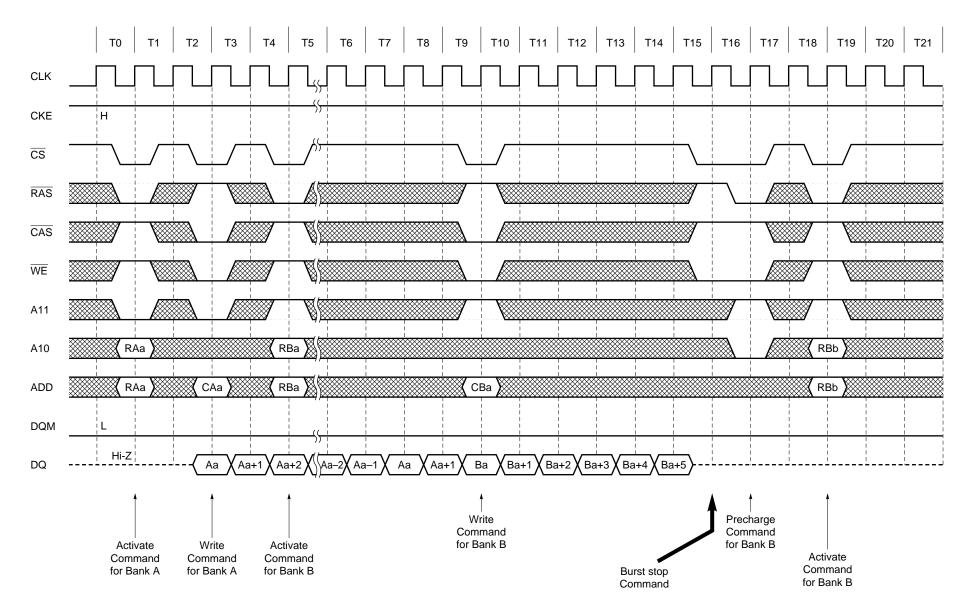
Auto Precharge after Write Burst (2/2) (Burst length = 4, CAS latency = 3)



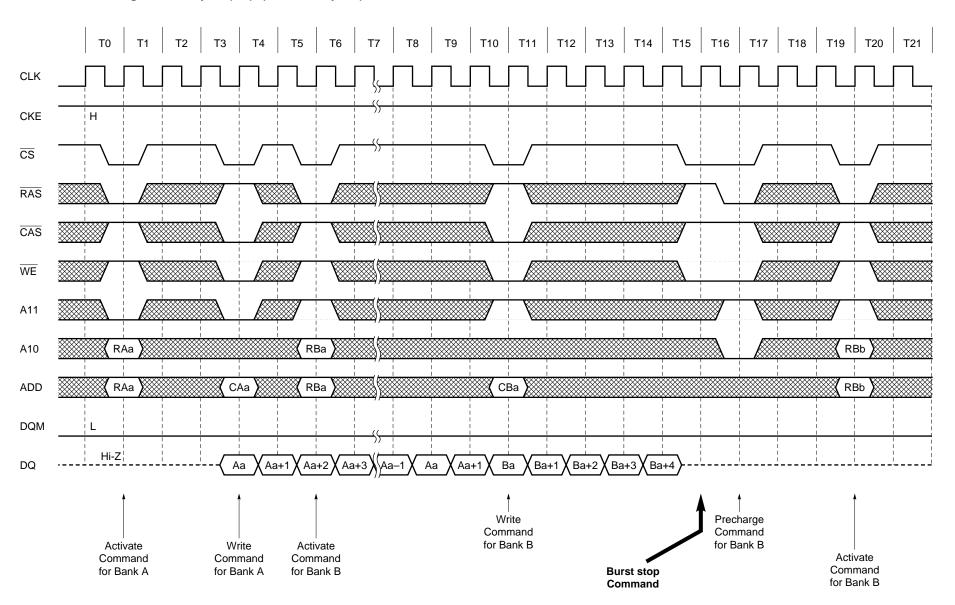


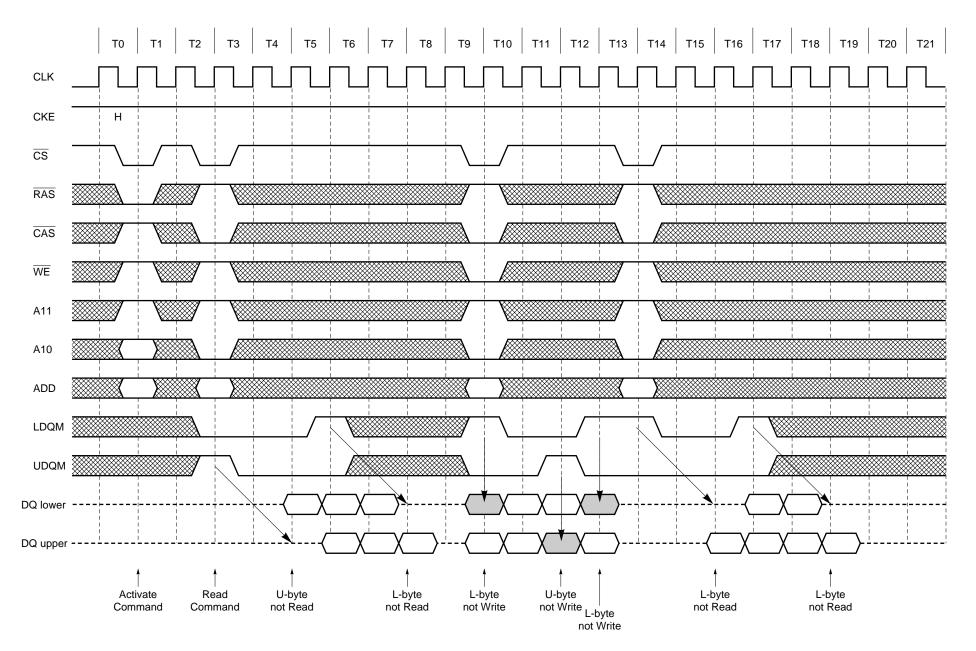
Full Page READ Cycle (2/2) (CAS latency = 3)



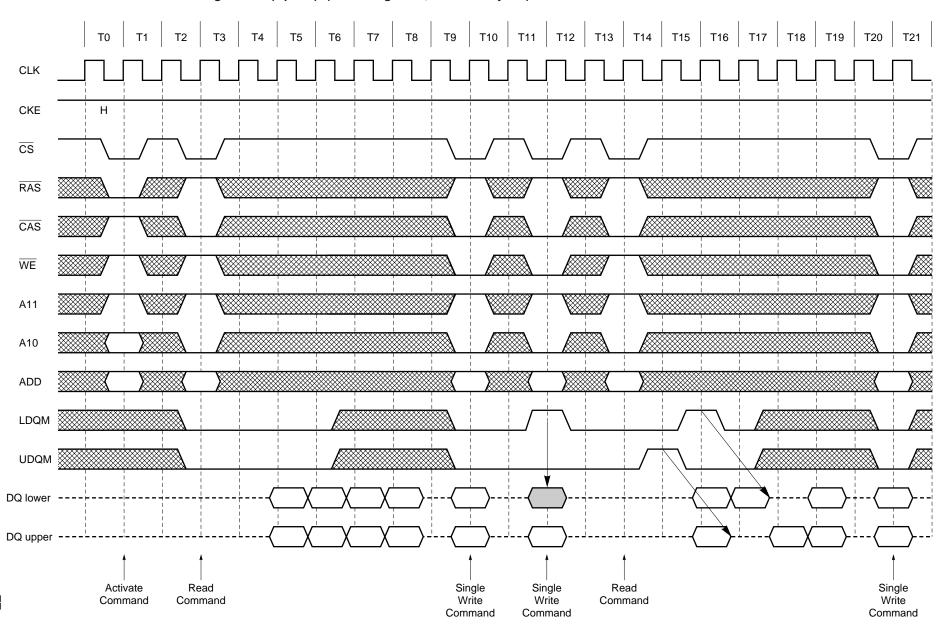


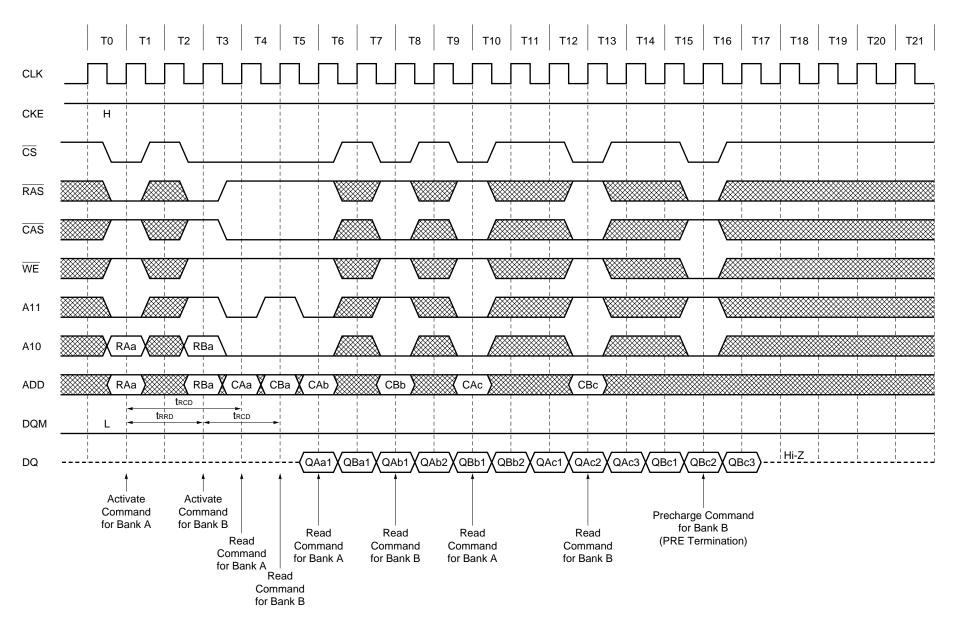
Full Page WRITE Cycle (2/2) (CAS latency = 3)



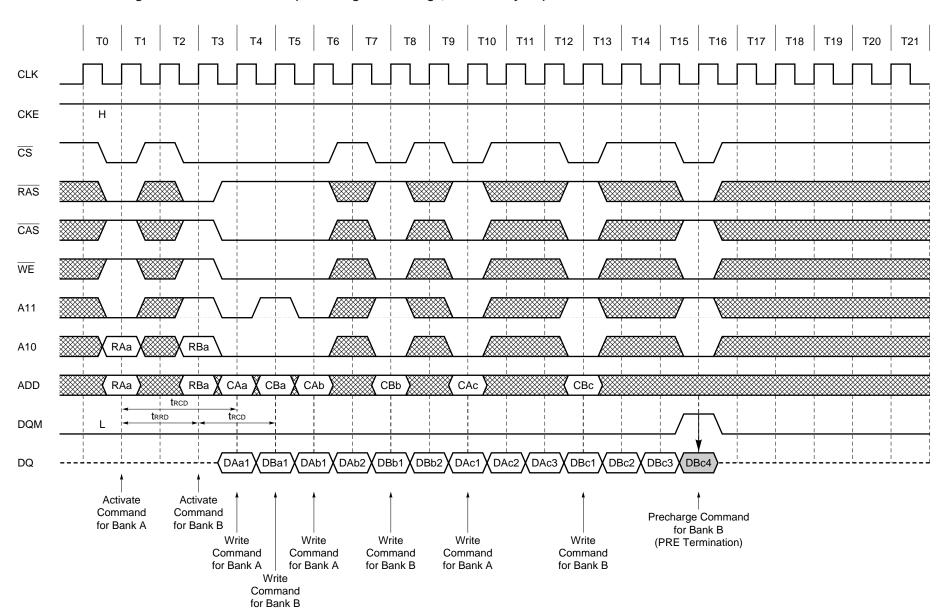


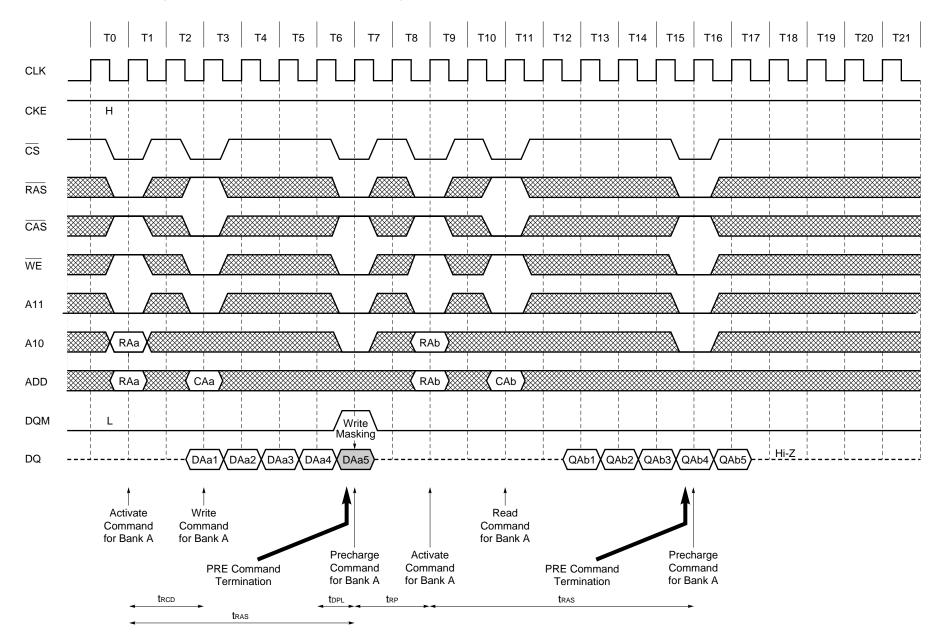
13.24 Burst Read and Single Write (Option) (Burst length = 4, CAS latency = 2)



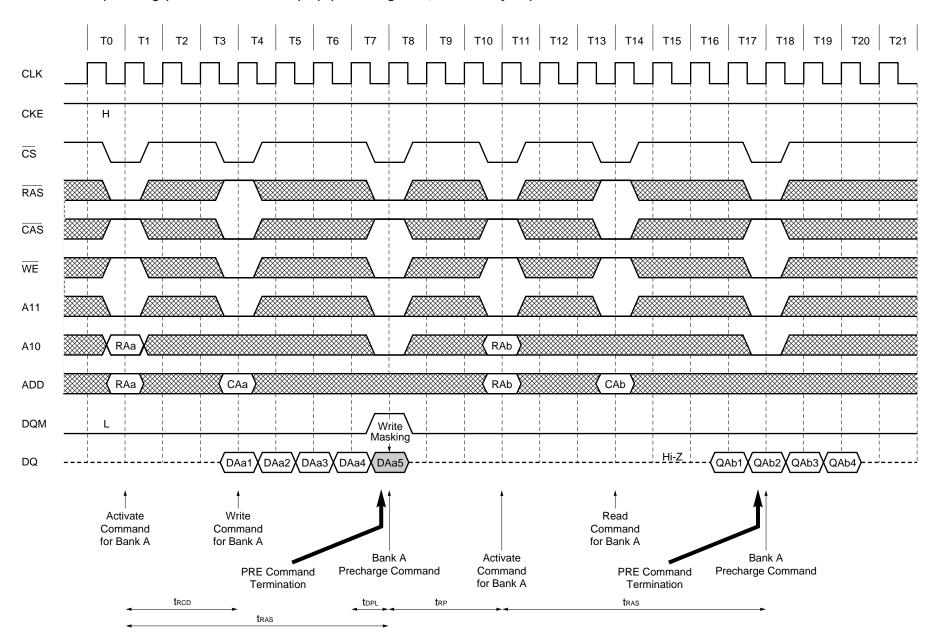


13.26 Full Page Random Column Write (Burst length = Full Page, CAS latency = 2)





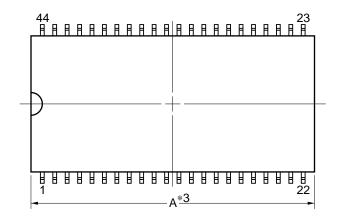
PRE(Precharge)Termination of Burst (2/2) (Burst length = 8, CAS latency = 3)



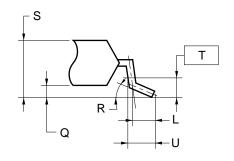
14. Package Drawings

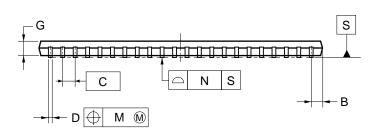
[µPD4516421AG5-9NF, 4516821AG5-9NF]

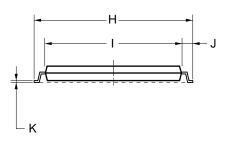
44PIN PLASTIC TSOP(II) (400 mil)



detail of lead end







NOTE

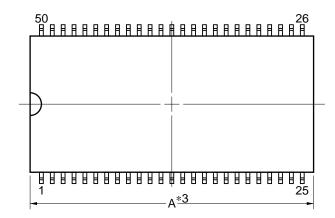
- 1. Controlling dimension millimeter.
- 2. Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.
- *3. Dimension "A" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm(0.006inch) per side.

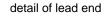
ITEM	MILLIMETERS	INCHES
Α	18.32±0.04	0.721±0.002
В	0.905 MAX.	0.036 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	$0.32^{+0.08}_{-0.07}$	0.013±0.003
G	1.0±0.05	$0.039^{+0.003}_{-0.002}$
Н	11.76±0.2	0.463±0.008
I	10.11±0.04	0.398±0.002
J	0.825±0.2	$0.032^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5	0.020
М	0.13	0.005
N	0.10	0.004
Q	0.1±0.05	0.004±0.002
R	3°+5°	3°+5°
S	1.2MAX.	0.048MAX.
Т	0.25(T.P.)	0.010(T.P.)
U	0.60±0.15	$0.024^{+0.006}_{-0.007}$

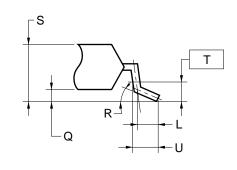
S44G5-80-9NF

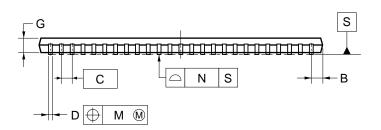
[µPD4516161AG5-9NF]

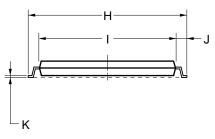
50PIN PLASTIC TSOP(II) (400 mil)











NOTE

- 1. Controlling dimension millimeter.
- Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.
- *3. Dimension "A" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm(0.006inch) per side.

ITEM	MILLIMETERS	INCHES
Α	20.86±0.04	0.821±0.002
В	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	$0.32^{+0.08}_{-0.07}$	0.013±0.003
G	1.0±0.05	$0.039^{+0.003}_{-0.002}$
Н	11.76±0.2	0.463±0.008
1	10.11±0.04	0.398±0.002
J	0.825±0.2	$0.032^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5	0.020
М	0.13	0.005
N	0.10	0.004
Q	0.1±0.05	0.004±0.002
R	3°+5°	3°+5°
S	1.2MAX.	0.048MAX.
Т	0.25(T.P.)	0.010(T.P.)
U	0.60±0.15	$0.024^{+0.006}_{-0.007}$

S50G5-80-9NF



15. Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μ PD4516421A, 4516821A, 4516161A.

Types of Surface Mount Device

4516421AG5-9NF, 4516821AG5-9NF: 44-pin plastic TSOP (II) (400 mil)

 μ PD4516161AG5-9NF: 50-pin plastic TSOP (II) (400 mil)

NOTES FOR CMOS DEVICES -

(1) PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

(2) HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

(3) STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

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While NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customers must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.

NEC devices are classified into the following three quality grades:

"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

Anti-radioactive design is not implemented in this product.

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