CENTILLIUM COMMUNICATIONS

Universal Flite Optimizer

Universal Full-Rate ADSL System Chipsets for CPE

Features

- Compliant with
  - — ITU G.992.1 (G.dmt)
  - — ITU G.992.2 (G.lite)
  - — ITU G.994.1 (G.hs)
  - — ANSI T1.413 Issue 2
- Supports Annex A and Annex C[1]
- Supports all framing modes per G.992.1
- Supports G.dmt, G.lite and T1.413 i2 through auto-detect feature
- Annex A operation
  - — Up to 8 Mbps downstream, 1 Mbps upstream for G.dmt mode
  - — Up to 1.5 Mbps downstream, 512 kbps upstream for G.lite mode
- Annex C operation
  - — Excellent performance for FBM (FEXT bitmap) and DBM (dual bitmap) modes
- Support for dual latency for G.dmt mode
- Host-based Soft SAR consumes minimum CPU time
- PCM interface for STM and voice applications

Benefits

- Small form factor reduces PC board space requirements
- Lowest power dissipation
- Software upgradeable, eliminates costly hardware upgrades
- Lowest BOM, requires only two additional active components
- Reference designs available, with software stacks, for fast time to market

1. Flite Optimizer available to support Annex A only markets.

Overview

The Universal Flite Optimizer™ is a chipset for a full-rate ADSL modem, consisting of only two chips, a DSP chip and an analog front end.

The chipset incorporates all silicon functions from the PC interface to the hybrid circuitry for an ITU G.992.1-compliant full-rate ADSL (asymmetric digital subscriber line) modem and provides a cost-effective, small-footprint, low-power solution. This solution requires only two additional active components, an EEPROM and a line driver. No external memory, controller, or VCXO are required, thus reducing the BOM cost. Through the choice of software drivers and few passive components, the chipset can be configured for either Annex A or Annex C operation.

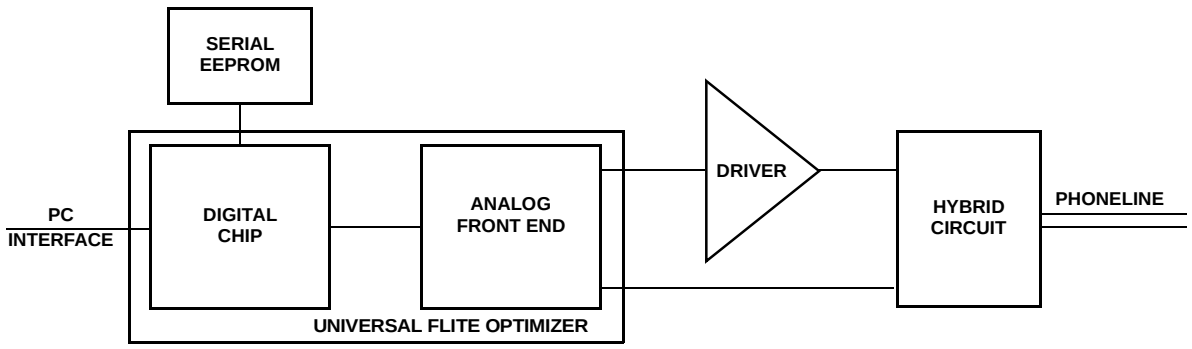
The chipset integrates an efficient power management scheme, which guarantees lowest power consumption. The operating efficiency and programmability of the chipset ensure long product lifetime and avoid the need for costly hardware upgrades.

Software stacks are provided to support PPP-over-ATM, PPP-over-Ethernet, RFC 1483, and IP-over-ATM network protocols.

The Universal Flite Optimizer software drivers support Microsoft Windows 95, Windows 98, Windows 98 Second Edition, Windows 2000, and Windows Millennium (once available) Operating Systems.

The ATM SAR function is supported via host processing with minimum impact on the host CPU. Since the modem function is independent of the host CPU, there is no deterioration in PC performance.

System Block Diagram



Universal Flite Optimizer USB

- No external power supply required, even at maximum G.dmt data rates
- Powered off the standard USB bus
- Compliant with USB v1.1 industry standard

Universal Flite Optimizer Mini-PCI

- Compliant with Mini-PCI v1.0 and PCI v2.2 industry standards
- 3.3V compatible IOs
- Support of power management v1.1 specification
- Support for PCI power states D0, D2, and D3
- 169-pin BGA package ideal for Mini-PCI board space requirements

Universal Flite Optimizer PCI

- Connects to standard PCI version 2.2 PC interface with support of power management v1.1 specification
- Supports MSI interrupt capability
- Concurrent ADSL and POTS operation
- AC97 interface for a soft V.90 modem

Universal Flite Optimizer CardBus

- 32-bit bus interface for standard CardBus design
- Slew-rate limited outputs, compliant with CardBus SSO requirements
- 3.3V compatible IOs
- AC97 interface for a soft V.90 modem
- 169-pin BGA package ideal for CardBus

Part Ordering Information:

Chipset	Function	Part Number	Package
Universal Flite Optimizer USB	Digital chip	CT-L62DU81	176-pin LQFP
	Analog front end	CT-L60AT81	32-pin LQFP
Universal Flite Optimizer PCI	Digital chip	CT-L62DP81	176-pin LQFP
	Analog front end	CT-L60AT81	32-pin LQFP
Universal Flite Optimizer Mini-PCI	Digital chip	CT-L62DM81	169-pin BGA
	Analog front end	CT-L60AT81	32-pin LQFP
Universal Flite Optimizer CardBus	Digital chip	CT-L62DB81	169-pin BGA
	Analog front end	CT-L60AT81	32-pin LQFP
Note: The chipsets must be ordered in pairs. Orders of individual components will be filled as chipset orders.			

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