

MOS INTEGRATED CIRCUIT

μ PD42S18165, 4218165

16 M-BIT DYNAMIC RAM

1 M-WORD BY 16-BIT, EDO, BYTE READ/WRITE MODE

Description

The μ PD42S18165, 4218165 are 1,048,576 words by 16 bits CMOS dynamic RAMs with optional EDO.

EDO is a kind of the page mode and is useful for the read operation.

Besides, the μ PD42S18165 can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

The μ PD42S18165, 4218165 are packaged in 50-pin plastic TSOP (II) and 42-pin plastic SOJ.

Features

- EDO (Hyper page mode)
- 1,048,576 words by 16 bits organization
- Single +5.0 V $\pm$ 10 % power supply
- Fast access and cycle time

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	EDO (Hyper page mode) cycle time (MIN.)
μ PD42S18165-50, 4218165-50	935 mW	50 ns	84 ns	20 ns
μ PD42S18165-60, 4218165-60	880 mW	60 ns	104 ns	25 ns
μ PD42S18165-70, 4218165-70	825 mW	70 ns	124 ns	30 ns

- The μ PD42S18165 can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μ PD42S18165	1,024 cycles/128 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	1.4 mW (CMOS level input)
μ PD4218165	1,024 cycles/16 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	5.5 mW (CMOS level input)

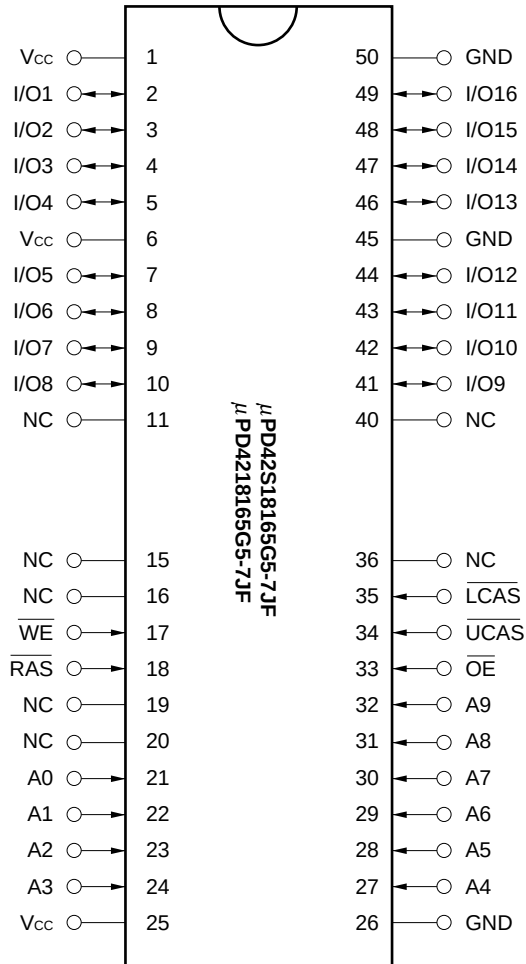
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Ordering Information

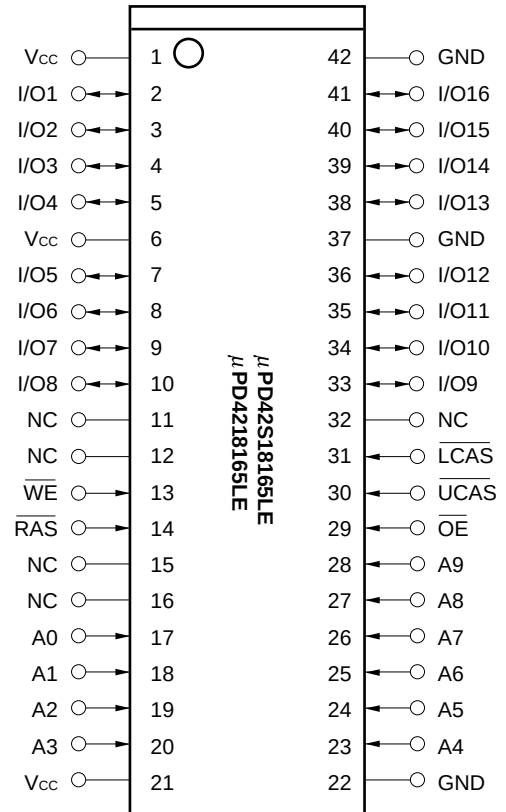
Part number	Access time (MAX.)	Package	Refresh
μ PD42S18165G5-50-7JF	50 ns	50-pin plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD42S18165G5-60-7JF	60 ns		
μ PD42S18165G5-70-7JF	70 ns		
μ PD42S18165LE-50	50 ns	42-pin plastic SOJ (400 mil)	
μ PD42S18165LE-60	60 ns		
μ PD42S18165LE-70	70 ns		
μ PD4218165G5-50-7JF	50 ns	50-pin plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD4218165G5-60-7JF	60 ns		
μ PD4218165G5-70-7JF	70 ns		
μ PD4218165LE-50	50 ns	42-pin plastic SOJ (400 mil)	
μ PD4218165LE-60	60 ns		
μ PD4218165LE-70	70 ns		

Pin Configurations (Marking Side)

50-pin Plastic TSOP (II) (400 mil)

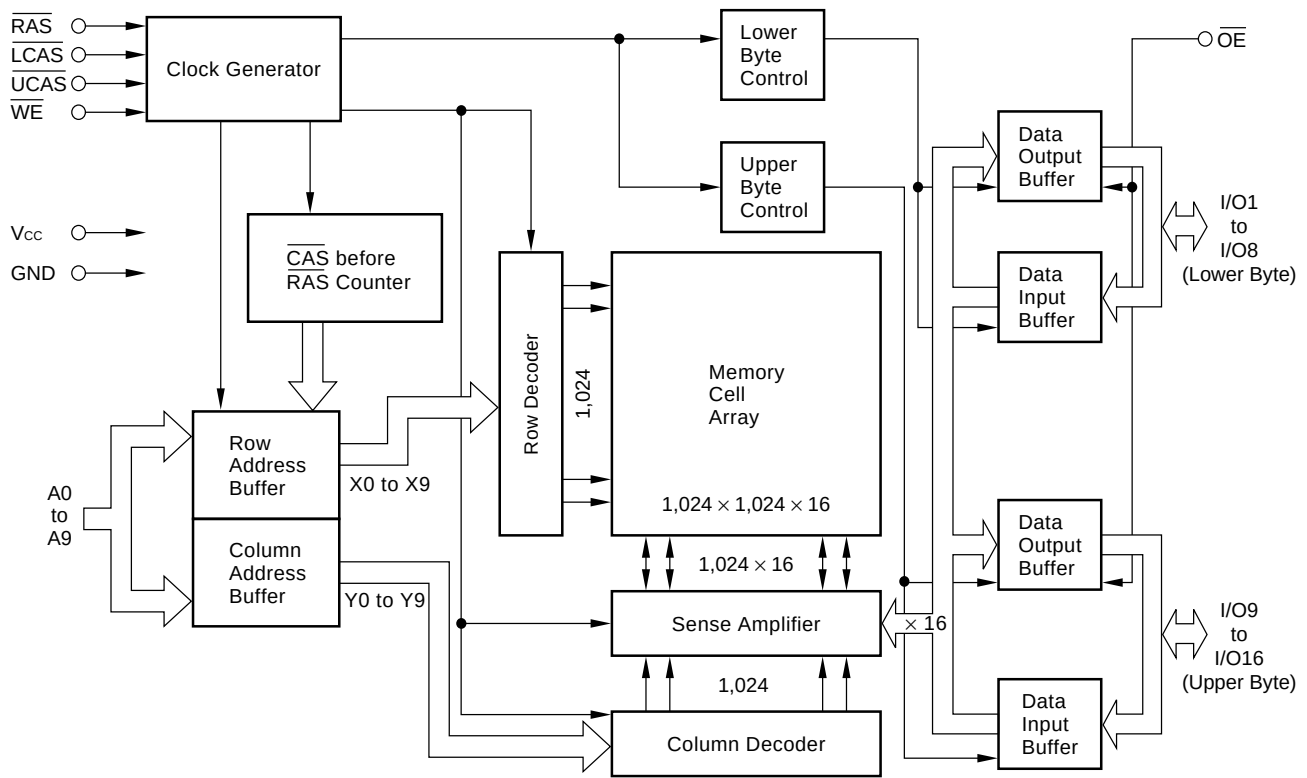


42-pin Plastic SOJ (400 mil)



- A0 to A9 : Address Inputs
- I/O1 to I/O16 : Data Inputs/Outputs
- $\overline{\text{RAS}}$: Row Address Strobe
- $\overline{\text{UCAS}}$: Column Address Strobe (upper)
- $\overline{\text{LCAS}}$: Column Address Strobe (lower)
- $\overline{\text{WE}}$: Write Enable
- $\overline{\text{OE}}$: Output Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

Block Diagram



Input/Output Pin Functions

The μ PD42S18165, 4218165 have input pins $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ ^{Note}, $\overline{\text{WE}}$, $\overline{\text{OE}}$, A0 to A9 and input/output pins I/O1 to I/O16.

Pin name	Input/Output	Function
$\overline{\text{RAS}}$ (Row address strobe)	Input	$\overline{\text{RAS}}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • CAS before $\overline{\text{RAS}}$ refresh
$\overline{\text{CAS}}$ (Column address strobe)		$\overline{\text{CAS}}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A9 (Address inputs)		Address bus. Input total 20-bit of address signal, upper 10-bit and lower 10-bit in sequence (address multiplex method). Therefore, one word is selected from 1,048,576-word by 16-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{\text{RAS}}$. Then, switch the address bus to column address and activate $\overline{\text{CAS}}$. Each address is taken into the device when $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are activated. Therefore, the address input setup time (t_{ASR} , t_{ASC}) and hold time (t_{RAH} , t_{CAH}) are specified for the activation of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$.
$\overline{\text{WE}}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$.
$\overline{\text{OE}}$ (Output enable)		Read control signal. Read operation can be executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{OE}}$. If $\overline{\text{WE}}$ is activated during read operation, $\overline{\text{OE}}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O16 (Data inputs/outputs)	Input/Output	16-bit data bus. I/O1 to I/O16 are used to input/output data.

Note $\overline{\text{CAS}}$ means $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.

★ Hyper Page Mode (EDO)

The hyper page mode (EDO) is a kind of page mode with enhanced features. The two major features of the hyper page mode (EDO) are as follows.

1. Data output time is extended.

In the hyper page mode (EDO), the output data is held to the next $\overline{\text{CAS}}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode (EDO) is extended compared with the fast page mode (= data extend function). In the fast page mode, the data output time becomes shorter as the $\overline{\text{CAS}}$ cycle time becomes shorter. Therefore, in the hyper page mode (EDO), the timing margin in read cycle is larger than that of the fast page mode even if the $\overline{\text{CAS}}$ cycle time becomes shorter.

2. The $\overline{\text{CAS}}$ cycle time in the hyper page mode (EDO) is shorter than that in the fast page mode.

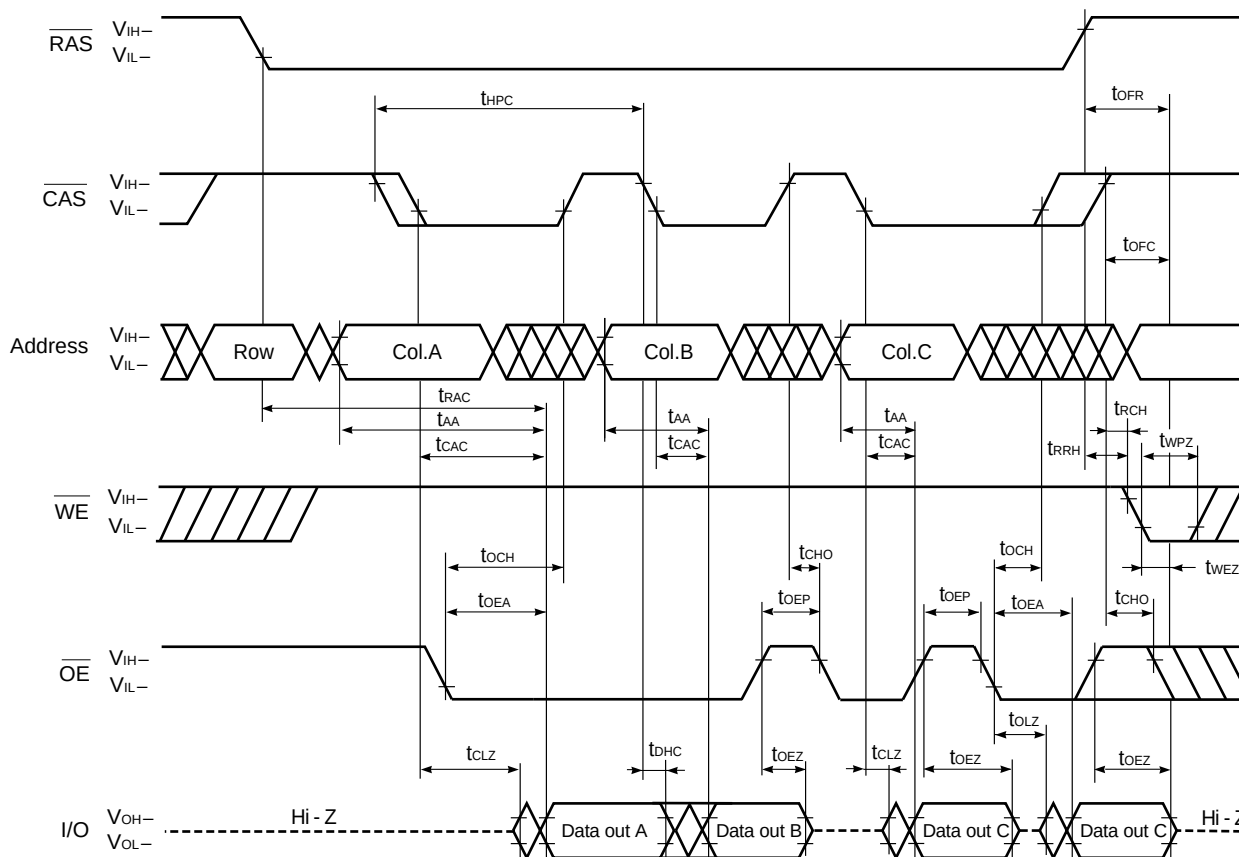
In the hyper page mode (EDO), due to the data extend function, the $\overline{\text{CAS}}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.

Taking a device whose t_{RAC} is 60 ns as an example, the $\overline{\text{CAS}}$ cycle time in the fast page mode is 25 ns while that in the fast page mode is 40 ns.

In the hyper page mode (EDO), read (data out) and write (data in) cycles can be executed repeatedly during one $\overline{\text{RAS}}$ cycle. The hyper page mode (EDO) allows both read and write operations during one cycle.

The following shows a part of the hyper page mode (EDO) read cycle. Specifications to be observed are described in the next page.

Hyper Page Mode (EDO) Read Cycle



Cautions when using the hyper page mode (EDO)

1. $\overline{\text{CAS}}$ access should be used to operate t_{HPC} at the MIN. value.
2. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$ as follows. The effective specification depends on the state of each signal.
 - (1) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are inactive (at the end of read cycle)

$\overline{\text{WE}}$: inactive, $\overline{\text{OE}}$: active

t_{OFC} is effective when $\overline{\text{RAS}}$ is inactivated before $\overline{\text{CAS}}$ is inactivated.

t_{OFR} is effective when $\overline{\text{CAS}}$ is inactivated before $\overline{\text{RAS}}$ is inactivated.

The slower of t_{OFC} and t_{OFR} becomes effective.
 - (2) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are active or either $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ is active (in read cycle)

$\overline{\text{WE}}$, $\overline{\text{OE}}$: inactive t_{BEZ} is effective.

Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are inactive or $\overline{\text{RAS}}$ is active and $\overline{\text{CAS}}$ is inactive (at the end of read cycle)

$\overline{\text{WE}}$, $\overline{\text{OE}}$: active and either t_{RRH} or t_{RCH} must be met t_{WEZ} and t_{WPZ} are effective.

The faster of t_{OEZ} and t_{WEZ} becomes effective.

The faster of (1) and (2) becomes effective.
3. In read cycle, the effective specification depends on the state of $\overline{\text{CAS}}$ signal when controlling data output with the $\overline{\text{OE}}$ signal.
 - (1) $\overline{\text{CAS}}$: inactive, $\overline{\text{OE}}$: active t_{HO} is effective.
 - (2) $\overline{\text{CAS}}$, $\overline{\text{OE}}$: active t_{CH} is effective.

Electrical Specifications

- $\overline{\text{CAS}}$ means $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.
- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μs ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$ inactive) and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-1.0 to +7.0	V
Supply voltage	V_{CC}		-1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	$^{\circ}\text{C}$
Storage temperature	T_{stg}		-55 to +125	$^{\circ}\text{C}$

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low level input voltage	V_{IL}		-1.0		+0.8	V
Operating ambient temperature	T_A		0		70	$^{\circ}\text{C}$

Capacitance ($T_A = 25^{\circ}\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

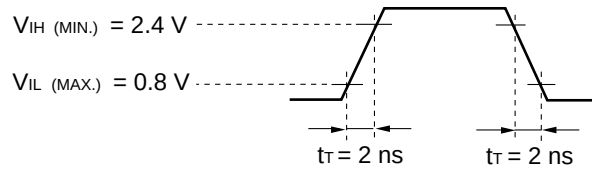
Parameter		Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current		I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ cycling	t _{RAC} = 50 ns	170	mA	1, 2, 3
			t _{RC} = t _{RC (MIN.)} , I _O = 0 mA	t _{RAC} = 60 ns	160		
				t _{RAC} = 70 ns	150		
Standby current	μ PD42S18165	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{IH (MIN.)}$, I _O = 0 mA		2.0	mA	
			$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}$, I _O = 0 mA		0.25		
	μ PD4218165		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{IH (MIN.)}$, I _O = 0 mA		2.0		
			$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}$, I _O = 0 mA		1.0		
$\overline{\text{RAS}}$ only refresh current		I _{CC3}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} \geq V_{IH (MIN.)}$ t _{RC} = t _{RC (MIN.)} , I _O = 0 mA	t _{RAC} = 50 ns	170	mA	1, 2, 3, 4
				t _{RAC} = 60 ns	160		
				t _{RAC} = 70 ns	150		
Operating current (Hyper page mode (EDO))		I _{CC4}	$\overline{\text{RAS}} \leq V_{IL (MAX.)}$, $\overline{\text{CAS}}$ cycling t _{HPC} = t _{HPC (MIN.)} , I _O = 0 mA	t _{RAC} = 50 ns	120	mA	1, 2, 5
				t _{RAC} = 60 ns	110		
				t _{RAC} = 70 ns	100		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current		I _{CC5}	$\overline{\text{RAS}}$ cycling t _{RC} = t _{RC (MIN.)} , I _O = 0 mA	t _{RAC} = 50 ns	170	mA	1, 2
				t _{RAC} = 60 ns	160		
				t _{RAC} = 70 ns	150		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh current (1,024 cycles / 128 ms, only for the μ PD42S18165)		I _{CC6}	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh : t _{RC} = 125.0 μ s $\overline{\text{RAS}}, \overline{\text{CAS}}$: $V_{CC} - 0.2 \text{ V} \leq V_{IH} \leq V_{IH (MAX.)}$ $0 \text{ V} \leq V_{IL} \leq 0.2 \text{ V}$ Standby: $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}$ Address: V_{IH} or V_{IL} $\overline{\text{WE}}, \overline{\text{OE}}$: V_{IH} I _O = 0 mA	t _{RAS} ≤ 300 ns	350	μ A	1, 2
				t _{RAS} ≤ 1 μ s	400	μ A	1, 2
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh current (only for the μ PD42S18165)		I _{CC7}	$\overline{\text{RAS}}, \overline{\text{CAS}}$: t _{RASS} = 5 ms $V_{CC} - 0.2 \text{ V} \leq V_{IH} \leq V_{IH (MAX.)}$ $0 \text{ V} \leq V_{IL} \leq 0.2 \text{ V}$ I _O = 0 mA		250	μ A	2
Input leakage current		I _{I (L)}	V _I = 0 to 5.5 V All other pins not under test = 0 V	-10	+10	μ A	
Output leakage current		I _{O (L)}	V _O = 0 to 5.5 V Output is disabled (Hi-Z)	-10	+10	μ A	
High level output voltage		V _{OH}	I _O = -5.0 mA	2.4		V	
Low level output voltage		V _{OL}	I _O = +4.2 mA		0.4	V	

- Notes 1.** I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{HPC}).
- 2.** Specified values are obtained with outputs unloaded.
- 3.** I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{IL (MAX.)}$ and $\overline{\text{CAS}} \geq V_{IH (MIN.)}$.
- 4.** I_{CC3} is measured assuming that all column address inputs are held at either high or low.
- 5.** I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page (EDO) cycle.

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

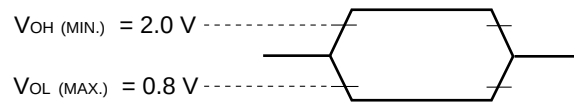
AC Characteristics Test Conditions

(1) Input timing specification

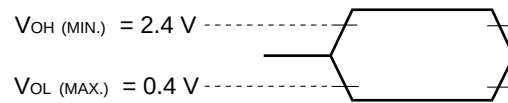


★ (2) Output timing specification

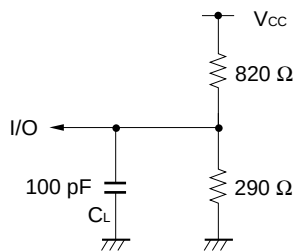
- μ PD42S18165-50, 4218165-50



- μ PD42S18165-60, 4218165-60
- μ PD42S18165-70, 4218165-70



(3) Output loading conditions



Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time		t _{RC}	84	–	104	–	124	–	ns	
$\overline{\text{RAS}}$ precharge time		t _{RP}	30	–	40	–	50	–	ns	
$\overline{\text{CAS}}$ precharge time		t _{CPN}	8	–	10	–	10	–	ns	
$\overline{\text{RAS}}$ pulse width		t _{RAS}	50	10,000	60	10,000	70	10,000	ns	1
$\overline{\text{CAS}}$ pulse width		t _{CAS}	8	10,000	10	10,000	12	10,000	ns	
$\overline{\text{RAS}}$ hold time		t _{RSH}	10	–	10	–	12	–	ns	
$\overline{\text{CAS}}$ hold time		t _{CSH}	38	–	40	–	50	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time		t _{RCD}	11	37	14	45	14	52	ns	2
$\overline{\text{RAS}}$ to column address delay time		t _{RAD}	9	25	12	30	12	35	ns	2
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time		t _{CRP}	5	–	5	–	5	–	ns	3
Row address setup time		t _{ASR}	0	–	0	–	0	–	ns	
Row address hold time		t _{RAH}	7	–	10	–	10	–	ns	
Column address setup time		t _{ASC}	0	–	0	–	0	–	ns	
Column address hold time		t _{CAH}	7	–	10	–	12	–	ns	
$\overline{\text{OE}}$ lead time referenced to $\overline{\text{RAS}}$		t _{OES}	0	–	0	–	0	–	ns	
$\overline{\text{CAS}}$ to data setup time		t _{CLZ}	0	–	0	–	0	–	ns	
$\overline{\text{OE}}$ to data setup time		t _{OLZ}	0	–	0	–	0	–	ns	
$\overline{\text{OE}}$ to data delay time		t _{OED}	10	–	13	–	15	–	ns	
Masked byte write hold time referenced to $\overline{\text{RAS}}$		t _{MRH}	0	–	0	–	0	–	ns	
Transition time (rise and fall)		t _T	1	50	1	50	1	50	ns	
Refresh time	μPD42S18165	t _{REF}	–	128	–	128	–	128	ms	4
	μPD4218165		–	16	–	16	–	16	ms	

Notes 1. In $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles, $t_{RAS(MAX.)}$ is 100 μ s.

If 10 μ s < t_{RAS} < 100 μ s, $\overline{\text{RAS}}$ precharge time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh (t_{RPS}) is applied.

2. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{\text{RAS}}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

3. $t_{CRP(MIN.)}$ requirement is applied to $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycles.

4. This specification is applied only to the μ PD42S18165.

Read Cycle

Parameter	Symbol	$t_{RAC} = 50 \text{ ns}$		$t_{RAC} = 60 \text{ ns}$		$t_{RAC} = 70 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{RAS}$	t_{RAC}	–	50	–	60	–	70	ns	1
Access time from $\overline{CAS}$	t_{CAC}	–	13	–	15	–	18	ns	1
Access time from column address	t_{AA}	–	25	–	30	–	35	ns	1
Access time from $\overline{OE}$	t_{OEA}	–	13	–	15	–	18	ns	
Column address lead time referenced to $\overline{RAS}$	t_{RAL}	25	–	30	–	35	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	ns	2
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	10	0	13	0	15	ns	3
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5	–	5	–	5	–	ns	4

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD}(\text{MAX.})$ and $t_{RCD} \leq t_{RCD}(\text{MAX.})$	$t_{RAC}(\text{MAX.})$	$t_{RAC}(\text{MAX.})$
$t_{RAD} > t_{RAD}(\text{MAX.})$ and $t_{RCD} \leq t_{RCD}(\text{MAX.})$	$t_{AA}(\text{MAX.})$	$t_{RAD} + t_{AA}(\text{MAX.})$
$t_{RCD} > t_{RCD}(\text{MAX.})$	$t_{CAC}(\text{MAX.})$	$t_{RCD} + t_{CAC}(\text{MAX.})$

$t_{RAD}(\text{MAX.})$ and $t_{RCD}(\text{MAX.})$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD}(\text{MAX.})$ and $t_{RCD} \geq t_{RCD}(\text{MAX.})$ will not cause any operation problems.

2. Either $t_{RCH}(\text{MIN.})$ or $t_{RRH}(\text{MIN.})$ should be met in read cycles.
3. $t_{OEZ}(\text{MAX.})$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL} .
4. $\overline{WE}$: inactive (in read cycle)
 $\overline{CAS}$: inactive, $\overline{OE}$: active t_{HO} is effective.
 $\overline{CAS}$, $\overline{OE}$: active t_{CH} is effective.

Write Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{\text{WE}}$ hold time referenced to $\overline{\text{CAS}}$	t _{WCH}	7	–	10	–	10	–	ns	1
$\overline{\text{WE}}$ pulse width	t _{WP}	8	–	10	–	10	–	ns	1
$\overline{\text{WE}}$ lead time referenced to $\overline{\text{RAS}}$	t _{RWL}	10	–	10	–	12	–	ns	
$\overline{\text{WE}}$ lead time referenced to $\overline{\text{CAS}}$	t _{CWL}	8	–	10	–	12	–	ns	
$\overline{\text{WE}}$ setup time	t _{WCS}	0	–	0	–	0	–	ns	2
$\overline{\text{OE}}$ hold time	t _{OEh}	0	–	0	–	0	–	ns	
Data-in setup time	t _{DS}	0	–	0	–	0	–	ns	3
Data-in hold time	t _{DH}	7	–	10	–	10	–	ns	3

- Notes**
1. t_{WP} (MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, t_{WCH} (MIN.) should be met.
 2. If t_{WCS} ≥ t_{WCS} (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
 3. t_{DS} (MIN.) and t_{DH} (MIN.) are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t _{RWC}	107	–	133	–	157	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	t _{RWD}	64	–	77	–	89	–	ns	1
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	t _{CWD}	27	–	32	–	37	–	ns	1
Column address to $\overline{\text{WE}}$ delay time	t _{AWD}	39	–	47	–	54	–	ns	1

- Note**
1. If t_{WCS} ≥ t_{WCS} (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If t_{RWD} ≥ t_{RWD} (MIN.), t_{CWD} ≥ t_{CWD} (MIN.), t_{AWD} ≥ t_{AWD} (MIN.) and t_{CPWD} ≥ t_{CPWD} (MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode (EDO)

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	t _{HPC}	20	—	25	—	30	—	ns	1
$\overline{\text{RAS}}$ pulse width	t _{RASP}	50	125,000	60	125,000	70	125,000	ns	
★ $\overline{\text{CAS}}$ pulse width	t _{H_{CAS}}	8	10,000	10	10,000	12	10,000	ns	
★ $\overline{\text{CAS}}$ precharge time	t _{CP}	8	—	10	—	10	—	ns	
Access time from $\overline{\text{CAS}}$ precharge	t _{ACP}	—	30	—	35	—	40	ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$ delay time	t _{CPWD}	41	—	52	—	59	—	ns	2
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t _{RHCP}	30	—	35	—	40	—	ns	
Read modify write cycle time	t _{HPRWC}	52	—	66	—	75	—	ns	
Data output hold time	t _{DHC}	5	—	5	—	5	—	ns	
$\overline{\text{OE}}$ to $\overline{\text{CAS}}$ hold time	t _{OCH}	5	—	5	—	5	—	ns	3
$\overline{\text{OE}}$ precharge time	t _{OEP}	5	—	5	—	5	—	ns	
Output buffer turn-off delay from $\overline{\text{WE}}$	t _{WEZ}	0	10	0	13	0	15	ns	4, 5
★ $\overline{\text{WE}}$ pulse width	t _{WPZ}	8	—	10	—	10	—	ns	5
Output buffer turn-off delay from $\overline{\text{RAS}}$	t _{OF_R}	0	10	0	13	0	15	ns	4, 5
Output buffer turn-off delay from $\overline{\text{CAS}}$	t _{OF_C}	0	10	0	13	0	15	ns	4, 5

Notes 1. t_{HPC} (MIN.) is applied to $\overline{\text{CAS}}$ access.

2. If t_{WCS} ≥ t_{WCS} (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If t_{RWD} ≥ t_{RWD} (MIN.), t_{CWD} ≥ t_{CWD} (MIN.), t_{AWD} ≥ t_{AWD} (MIN.) and t_{CPWD} ≥ t_{CPWD} (MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

3. $\overline{\text{WE}}$: inactive (in read cycle)

$\overline{\text{CAS}}$: inactive, $\overline{\text{OE}}$: active t_{HO} is effective.

$\overline{\text{CAS}}$, $\overline{\text{OE}}$: active t_{CH} is effective.

4. t_{OF_C} (MAX.), t_{OF_R} (MAX.) and t_{WEZ} (MAX.) define the time when the output achieves the conditions of Hi-Z and is not referenced to V_{OH} or V_{OL}.

5. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$ as follows. The effective specification depends on state of each signal.

(1) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are inactive (at the end of the read cycle)

$\overline{\text{WE}}$: inactive, $\overline{\text{OE}}$: active

t_{OF_C} is effective when $\overline{\text{RAS}}$ is inactivated before $\overline{\text{CAS}}$ is inactivated.

t_{OF_R} is effective when $\overline{\text{CAS}}$ is inactivated before $\overline{\text{RAS}}$ is inactivated.

The slower of t_{OF_C} and t_{OF_R} becomes effective.

(2) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are active or either $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ is active (in read cycle)

$\overline{\text{WE}}$, $\overline{\text{OE}}$: inactive t_{BEZ} is effective.

Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are inactive or $\overline{\text{RAS}}$ is active and $\overline{\text{CAS}}$ is inactive (at the end of read cycle)

$\overline{\text{WE}}$, $\overline{\text{OE}}$: active and either t_{RRH} or t_{TRCH} must be met t_{WEZ} and t_{WPZ} are effective.

The faster of t_{OEZ} and t_{WEZ} becomes effective.

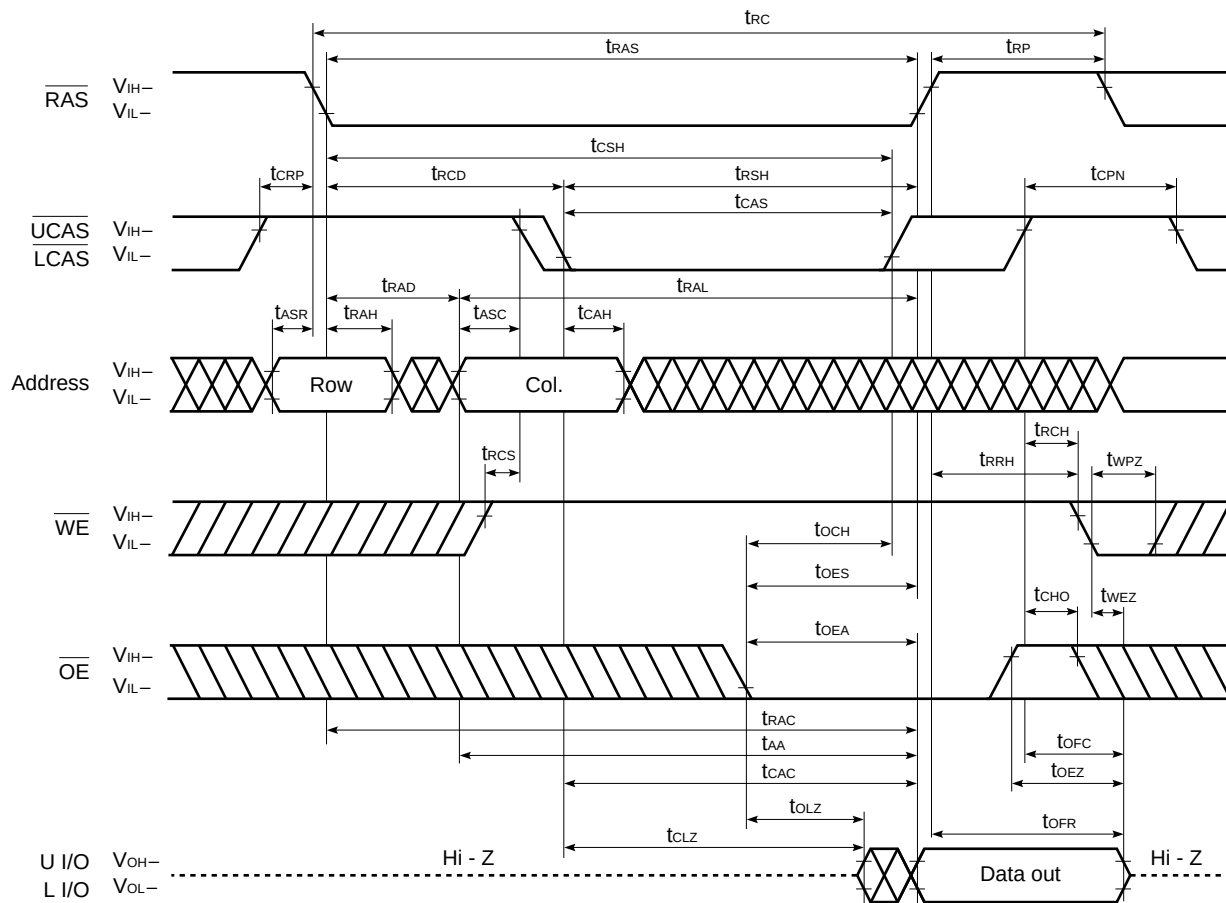
The faster of (1) and (2) becomes effective.

Refresh Cycle

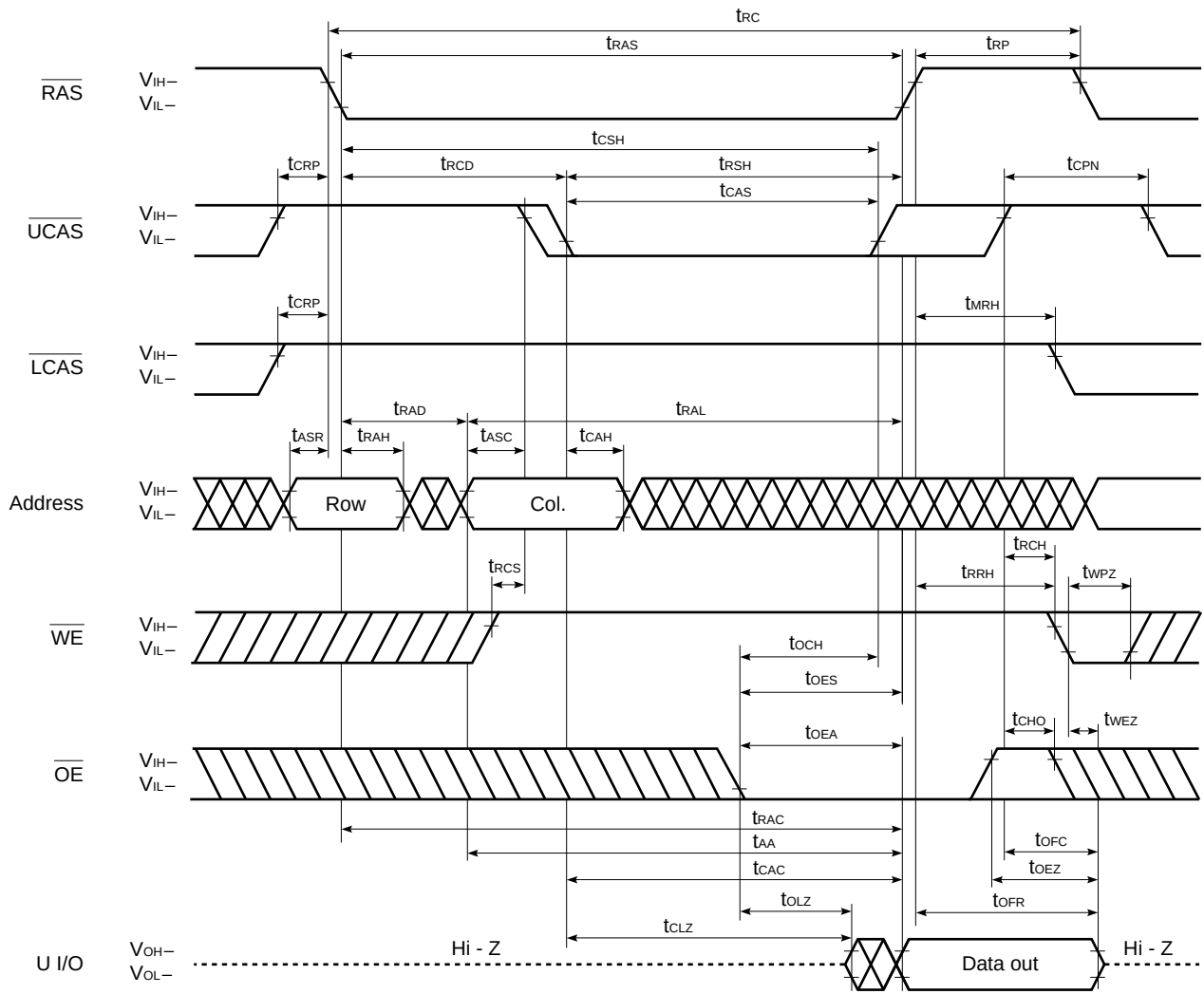
Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{\text{CAS}}$ setup time	t _{CSR}	5	–	5	–	5	–	ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh)	t _{CHR}	10	–	10	–	10	–	ns	
$\overline{\text{RAS}}$ precharge $\overline{\text{CAS}}$ hold time	t _{RPC}	5	–	5	–	5	–	ns	
$\overline{\text{RAS}}$ pulse width ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh)	t _{RASS}	100	–	100	–	100	–	μs	1
$\overline{\text{RAS}}$ precharge time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh)	t _{RPS}	90	–	110	–	130	–	ns	1
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh)	t _{CHS}	–50	–	–50	–	–50	–	ns	1
$\overline{\text{WE}}$ hold time	t _{WHR}	15	–	15	–	15	–	ns	

Note 1. This specification is applied only to the μPD42S18165.

Read Cycle

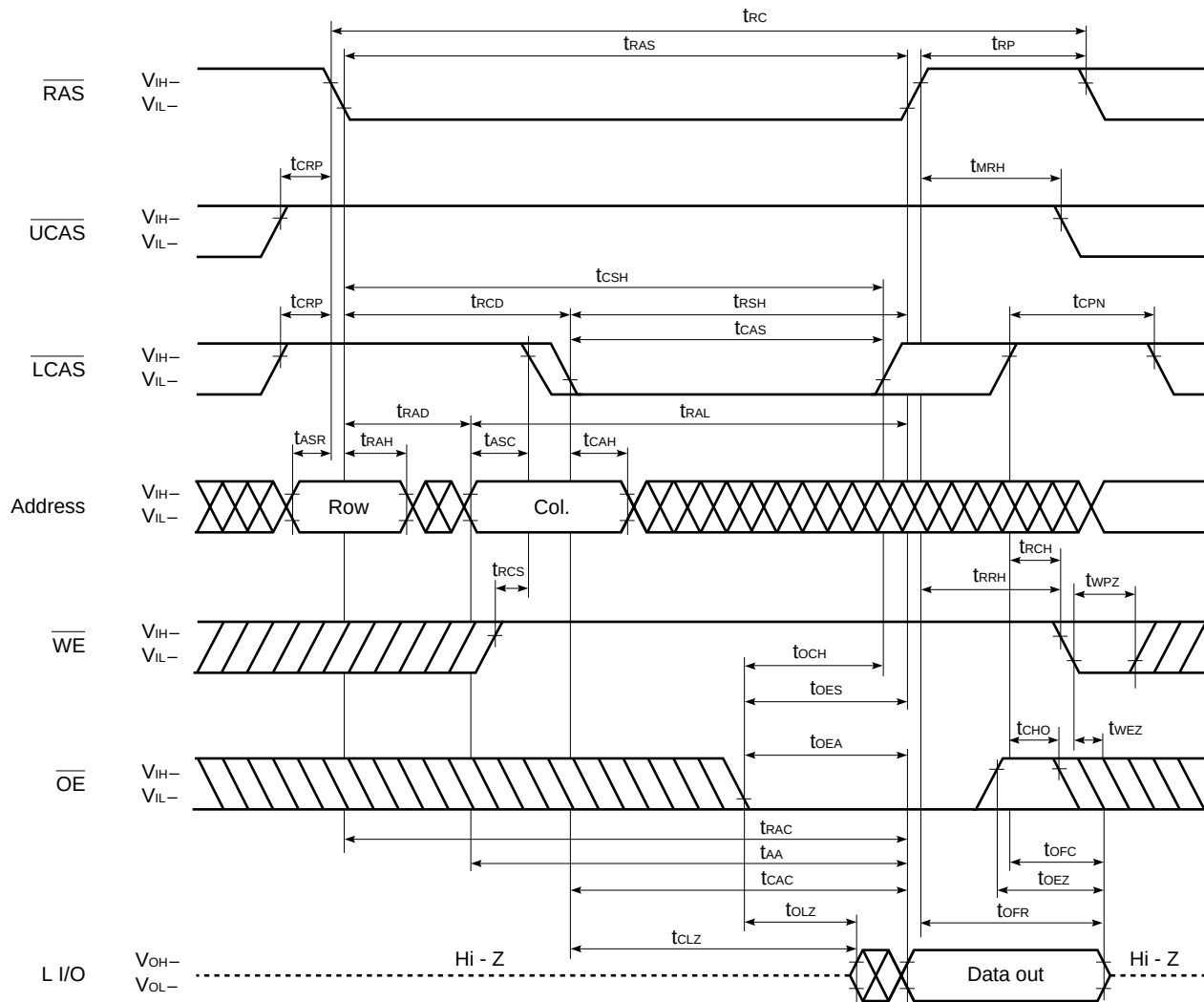


Upper Byte Read Cycle



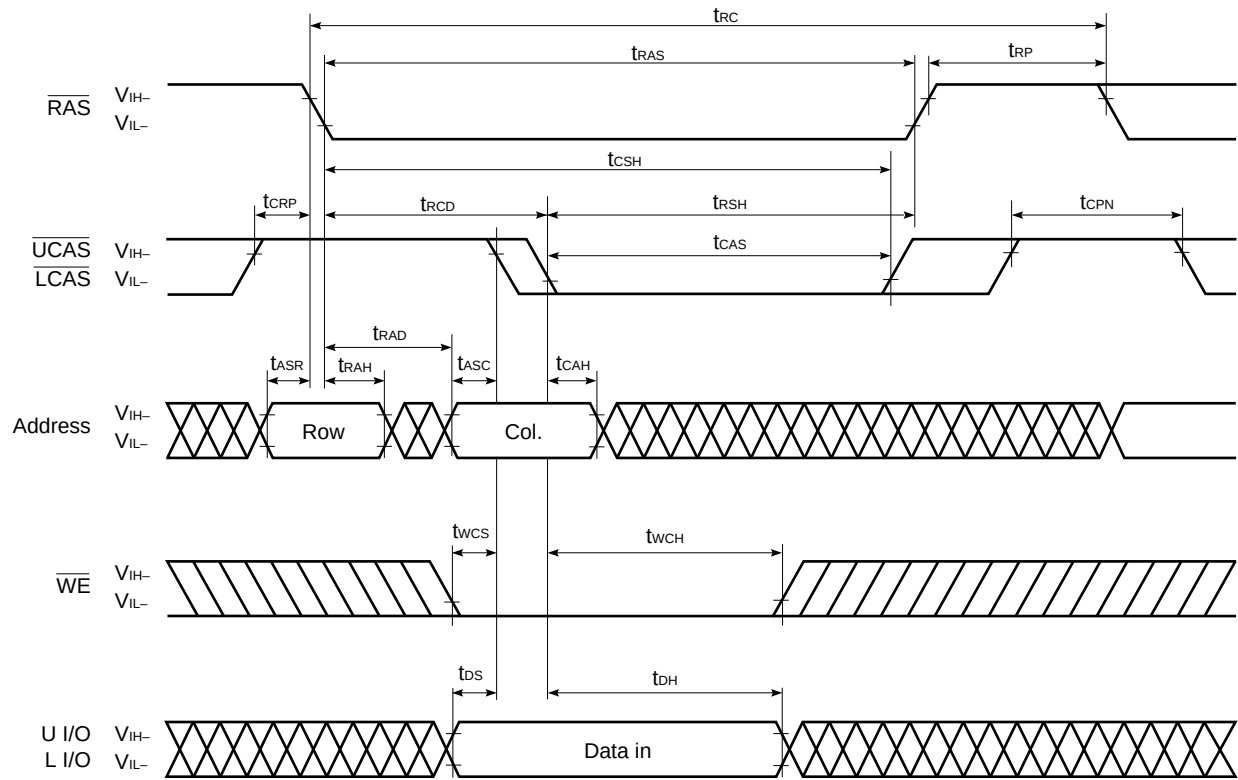
Remark L I/O: Hi-Z

Lower Byte Read Cycle



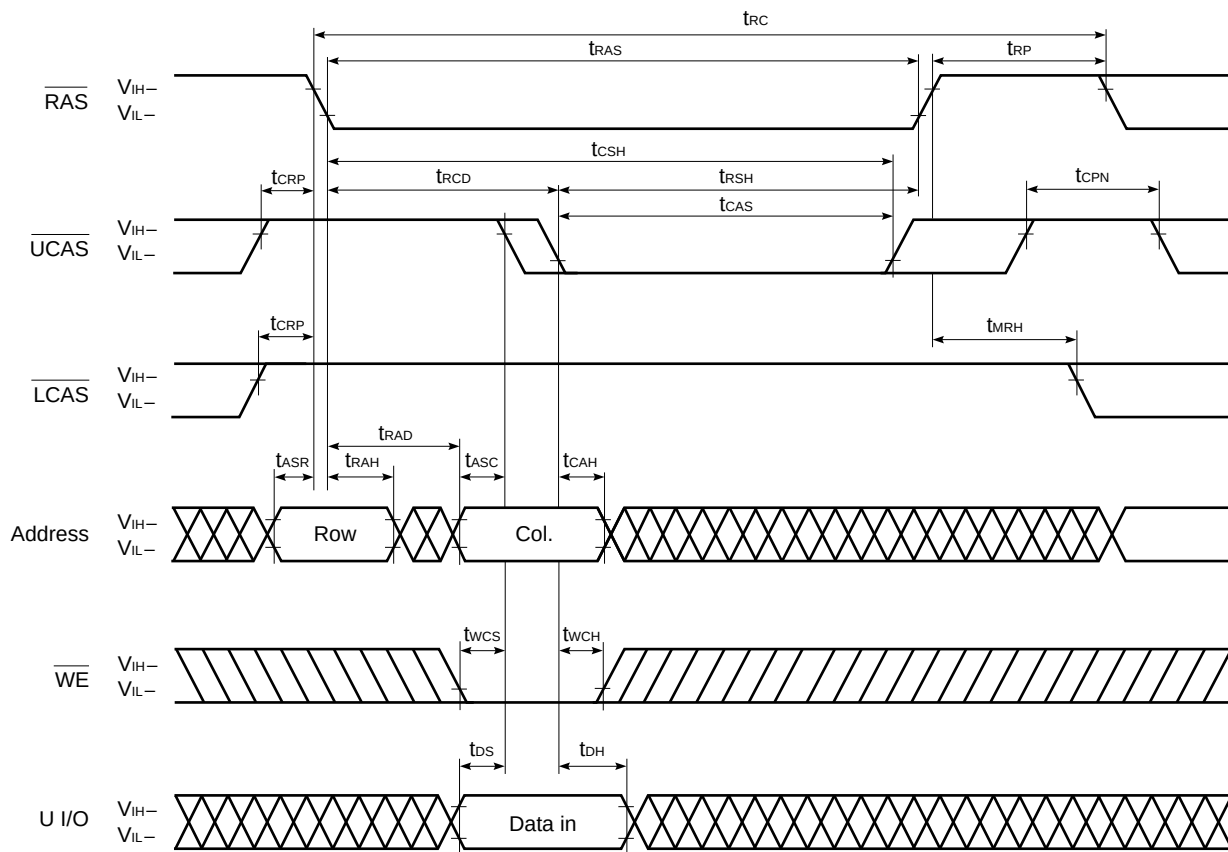
Remark U I/O: Hi-Z

Early Write Cycle



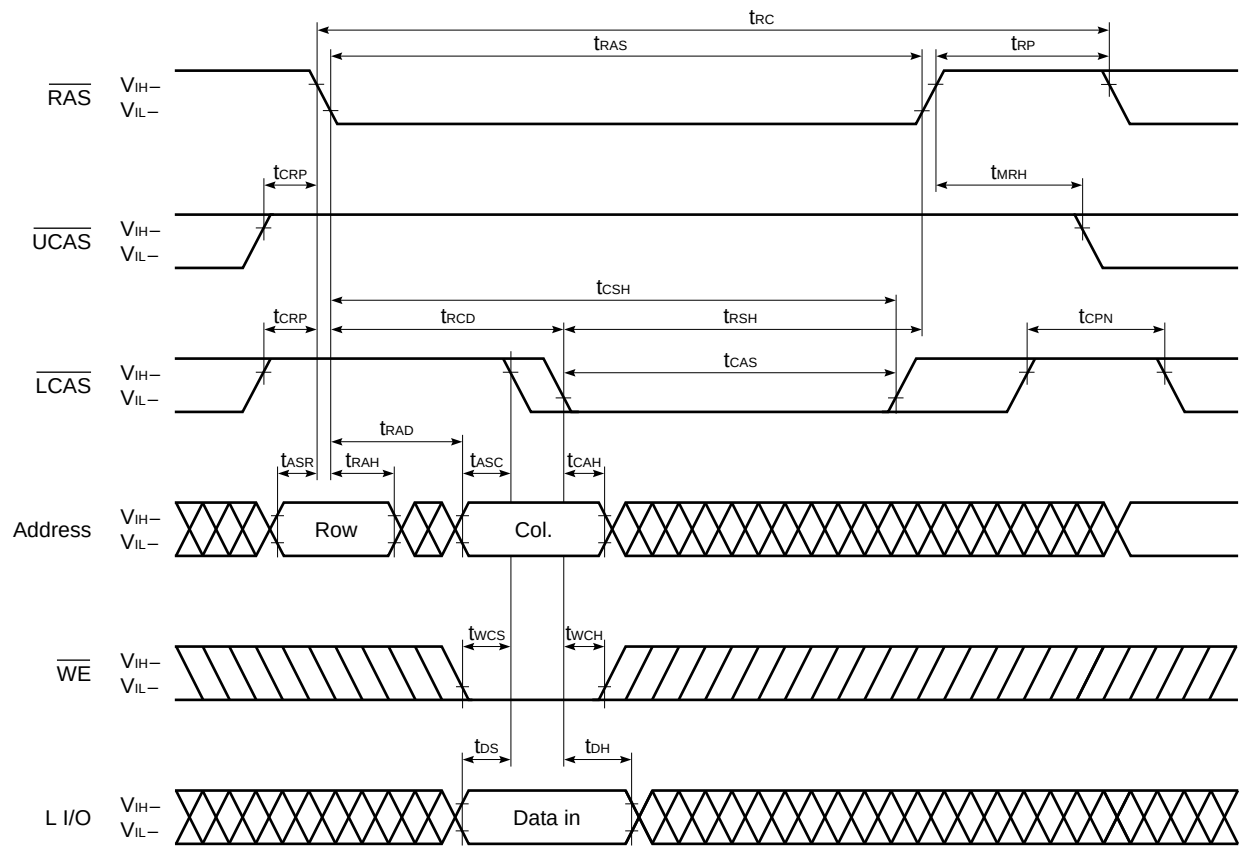
Remark $\overline{\text{OE}}$: Don't care

Upper Byte Early Write Cycle



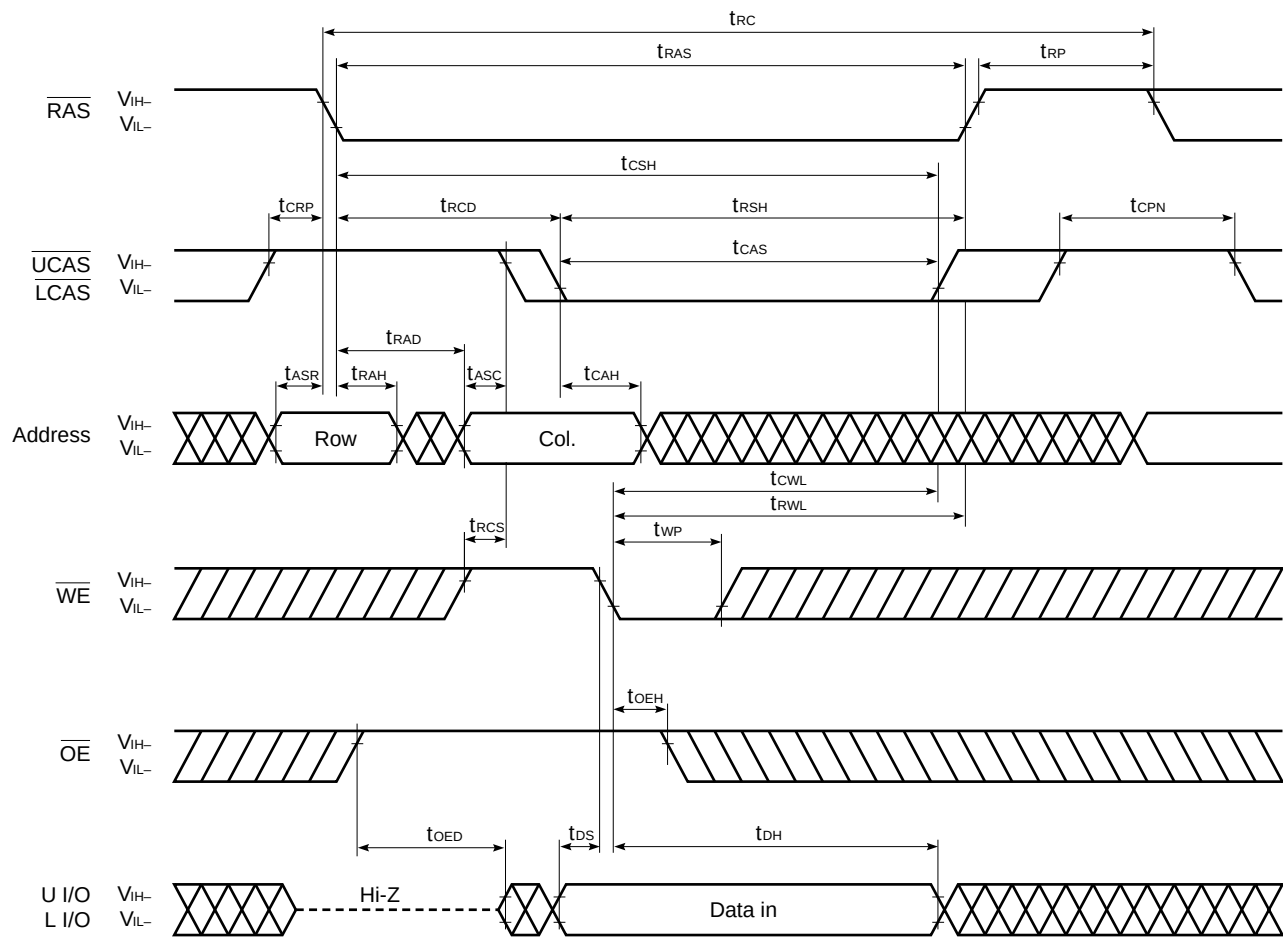
Remark $\overline{OE}$, L I/O: Don't care

Lower Byte Early Write Cycle

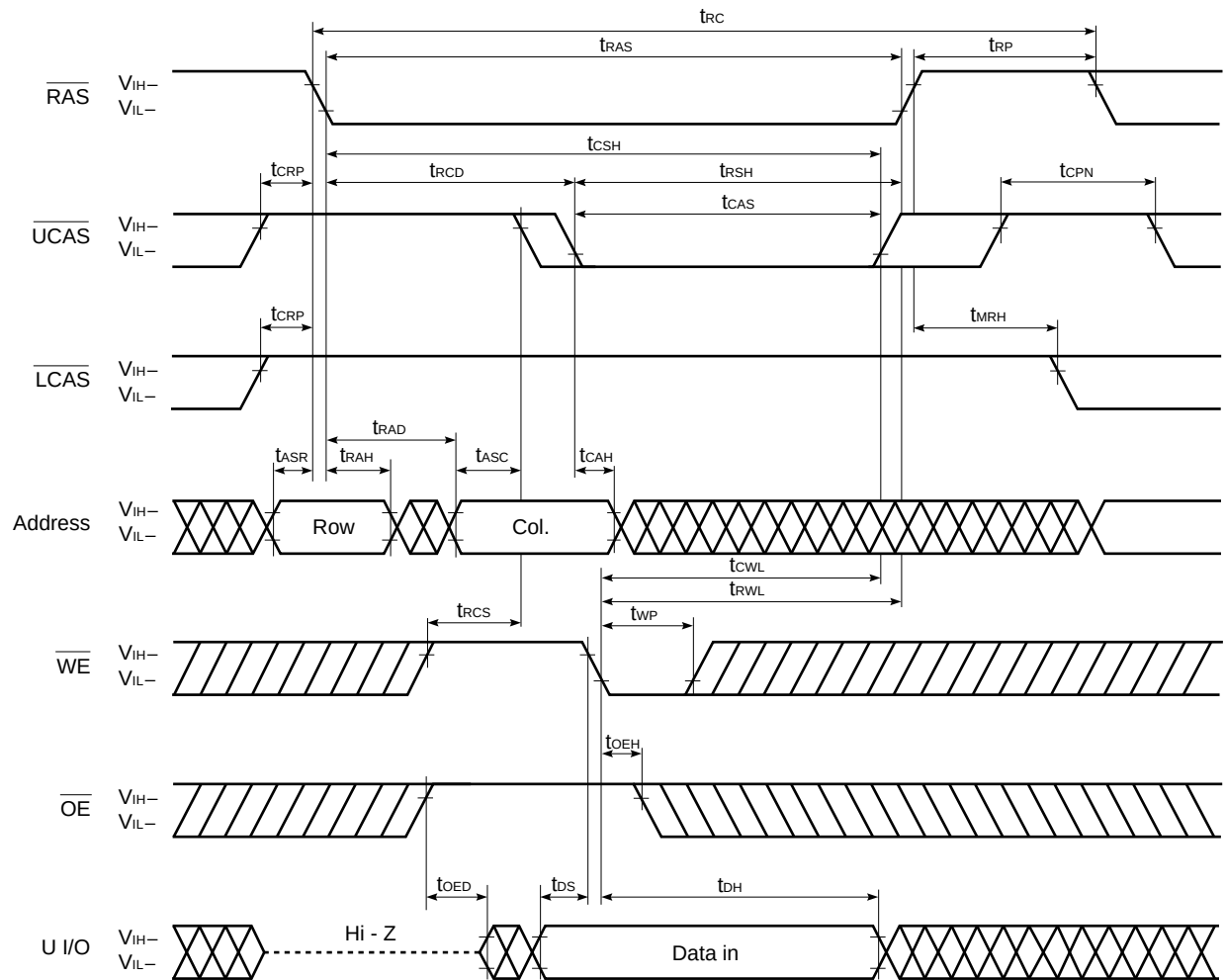


Remark $\overline{OE}$, U I/O: Don't care

Late Write Cycle

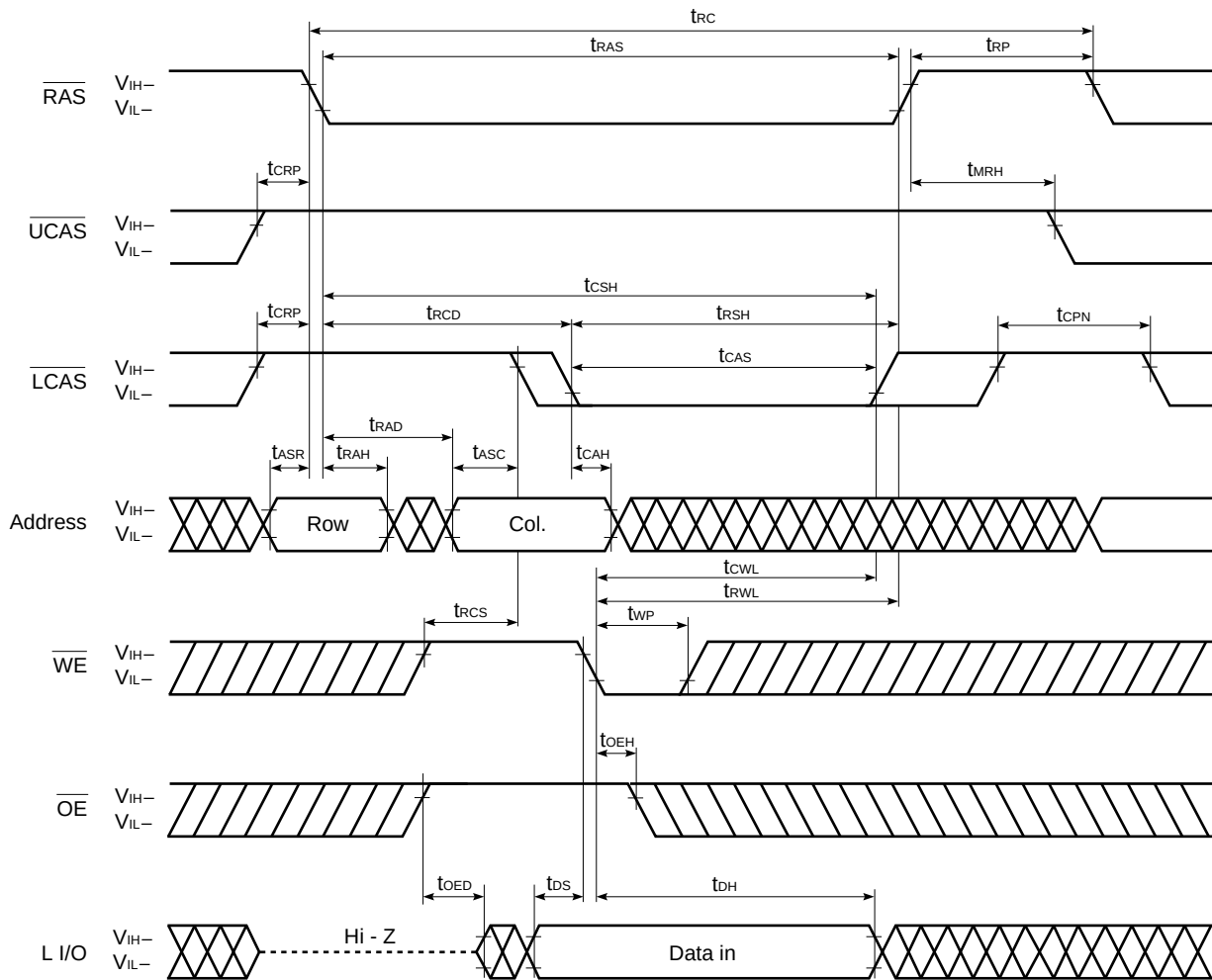


Upper Byte Late Write Cycle



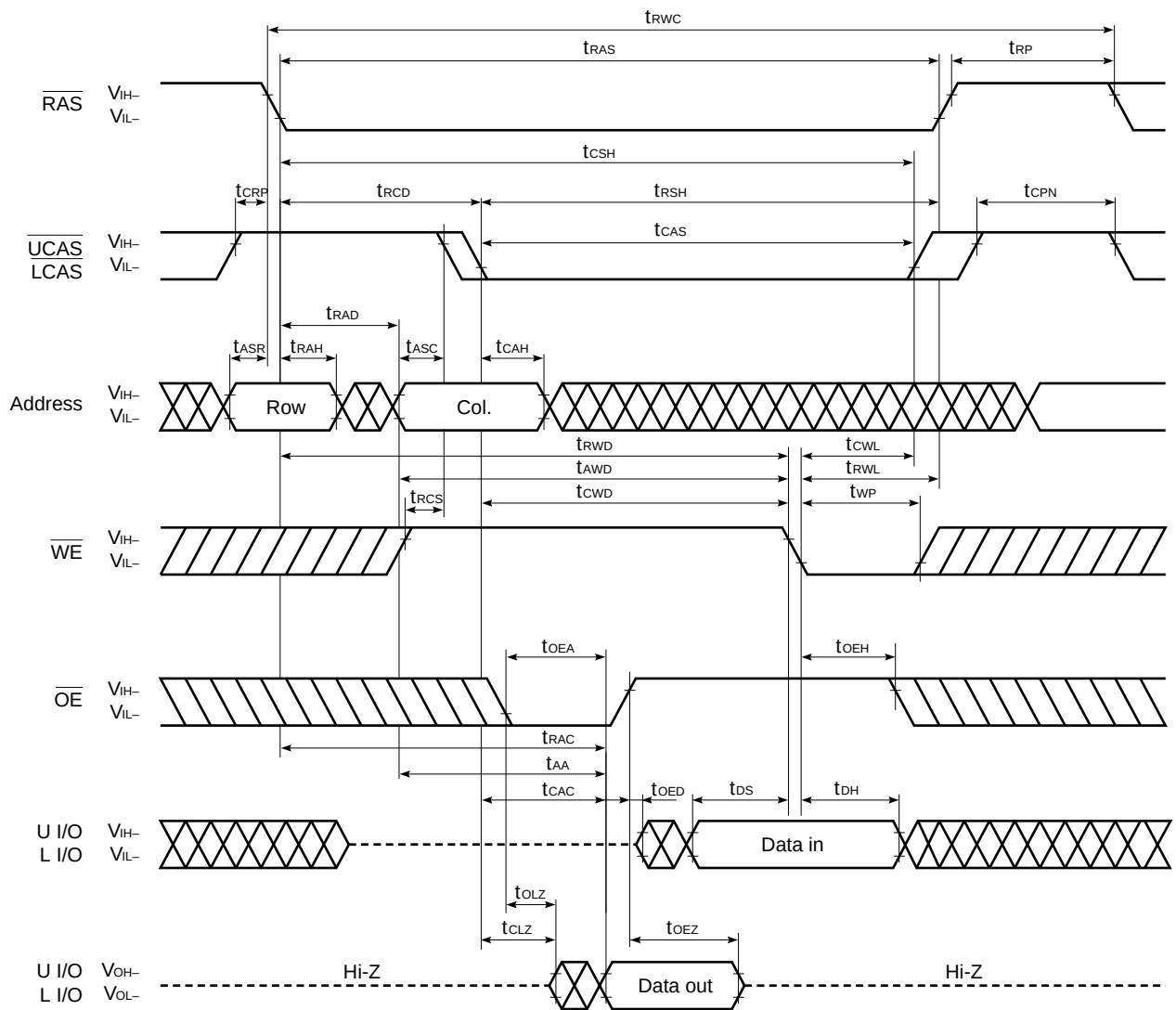
Remark L I/O: Don't care

Lower Byte Late Write Cycle



Remark U I/O: Don't care

Read Modify Write Cycle



The diagram illustrates the timing relationships for a 2D DRAM array. The signals and their timing parameters are as follows:

- RAS:** V_{IH} , V_{IL} . Timing parameters: t_{RAS} , t_{RWC} , t_{RP} .
- UCAS:** V_{IH} , V_{IL} . Timing parameters: t_{CRP} , t_{RCD} , t_{CSH} , t_{RSH} , t_{CAS} , t_{CPN} .
- LCAS:** V_{IH} , V_{IL} . Timing parameters: t_{CRP} , t_{MRH} .
- Address:** V_{IH} , V_{IL} . Timing parameters: t_{ASR} , t_{RAD} , t_{RAH} , t_{ASC} , t_{CAH} .
- WE:** V_{IH} , V_{IL} . Timing parameters: t_{RWD} , t_{AWD} , t_{RCS} , t_{CWD} , t_{CWL} , t_{RWL} , t_{WP} .
- OE:** V_{IH} , V_{IL} . Timing parameters: t_{OEA} , t_{OEH} , t_{OED} , t_{DS} , t_{DH} .
- U I/O:** V_{IH} , V_{IL} . Timing parameters: t_{OLZ} , t_{CLZ} , t_{OEZ} .
- U I/O:** V_{OH} , V_{OL} . Timing parameters: t_{OLZ} , t_{CLZ} , t_{OEZ} .

Remark In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.

The diagram illustrates the timing relationships for the 16M1602 LCD module. The signals and their timing parameters are as follows:

- RAS**: $\overline{\text{RAS}}$ signal. Timing parameters: t_{RAS} (high pulse width), t_{RP} (fall time), t_{CRP} (setup time before UCAS), t_{MRH} (hold time after UCAS).
- UCAS**: $\overline{\text{UCAS}}$ signal. Timing parameters: t_{CRP} (setup time before RAS), t_{MRH} (hold time after RAS).
- LCAS**: $\overline{\text{LCAS}}$ signal. Timing parameters: t_{CRP} (setup time before RAS), t_{RCD} (row address setup time), t_{CSH} (row address hold time), t_{RSH} (row address setup time), t_{CAS} (row address setup time), t_{CPN} (row address setup time).
- Address**: VIH and VIL signals. Timing parameters: t_{ASR} (setup time before RAS), t_{RAH} (row address hold time), t_{ASC} (row address setup time), t_{CAH} (row address hold time).
- WE**: VIH and VIL signals. Timing parameters: t_{RWD} (write data setup time), t_{AWD} (write data setup time), t_{RWL} (write data setup time), t_{CWD} (write data setup time), t_{WPD} (write data setup time).
- OE**: VIH and VIL signals. Timing parameters: t_{RCS} (row address setup time), t_{OE} (output enable setup time), t_{OE} (output enable hold time).
- L I/O**: VIH and VIL signals. Timing parameters: t_{RAC} (row address setup time), t_{AA} (address setup time), t_{CAC} (column address setup time), t_{OE} (output enable setup time), t_{OE} (output enable hold time).
- L I/O**: VOH and VOL signals. Timing parameters: t_{OLZ} (output low setup time), t_{CLZ} (output low setup time), t_{OE} (output enable setup time), t_{OE} (output enable hold time).

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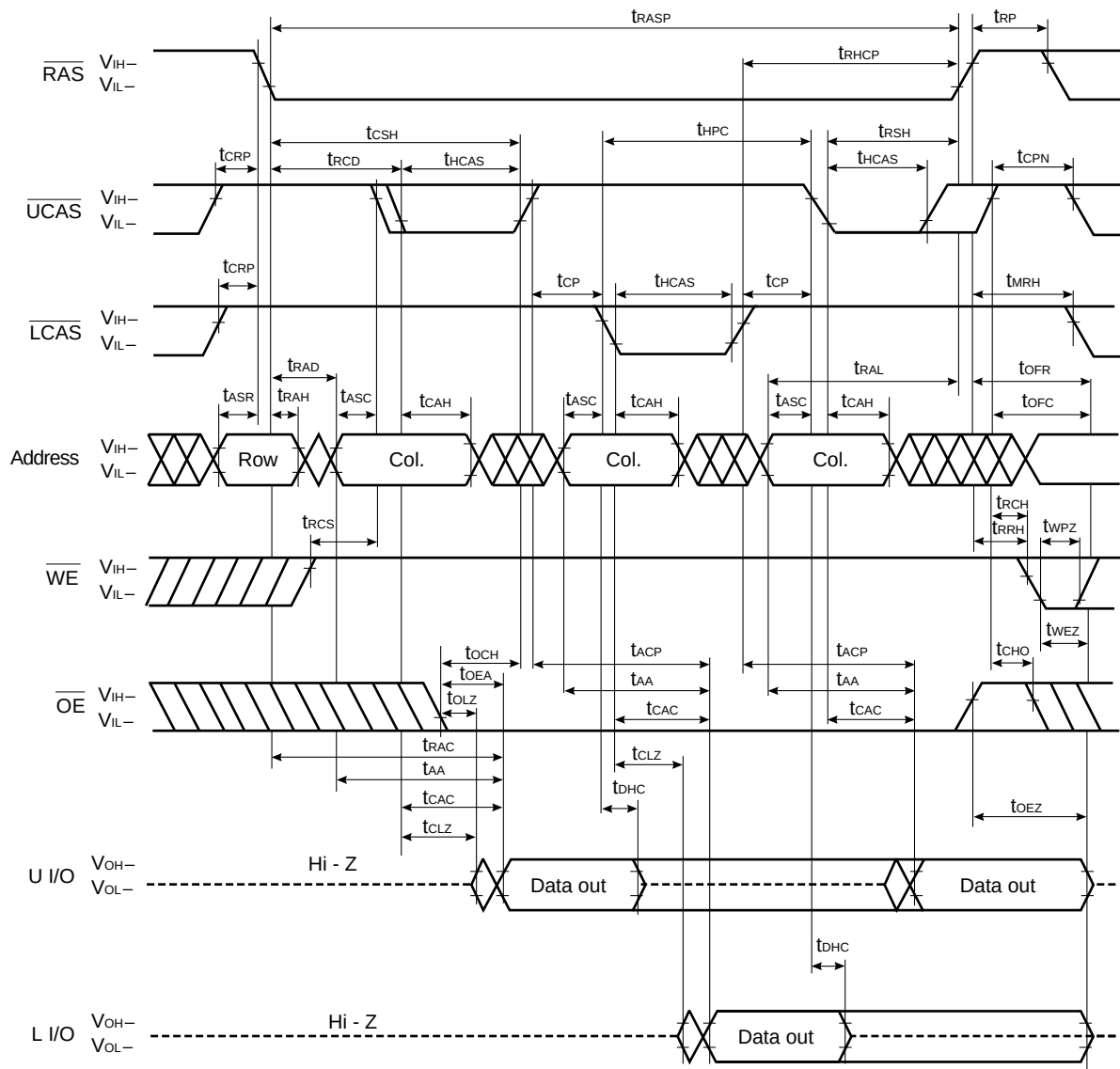
The timing diagram illustrates the relationship between the 64K1602 LCD module and the microcontroller. The signals and their timing parameters are as follows:

- RAS:** $\overline{\text{RAS}}$ signal. Timing parameters: t_{RASP} (pulse width), t_{RHCP} (high pulse width), t_{RP} (fall time).
- UCAS/LCAS:** $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ signals. Timing parameters: t_{CRP} (rise time), t_{RCD} (delay from RAS), t_{CSH} (high pulse width), t_{HCAS} (high to data setup), t_{CP} (delay from UCAS/LCAS), t_{HPC} (high pulse width), t_{RSH} (rise time), t_{CPN} (delay from UCAS/LCAS).
- Address:** V_{IH} and V_{IL} signals. Timing parameters: t_{ASR} (setup before RAS), t_{RAH} (hold after RAS), t_{ASC} (setup before UCAS/LCAS), t_{CAH} (hold after UCAS/LCAS), t_{AL} (setup before WE), t_{OFC} (hold after WE), t_{OFC} (hold after OE).
- WE:** V_{IH} and V_{IL} signals. Timing parameters: t_{RCH} (rise time), t_{RRH} (high pulse width), t_{WPZ} (pulse width), t_{WEZ} (pulse width), t_{CHO} (hold after WE).
- OE:** V_{IH} and V_{IL} signals. Timing parameters: t_{OEA} (setup before UCAS/LCAS), t_{OLZ} (hold after UCAS/LCAS), t_{OHC} (hold after OE), t_{AA} (high pulse width), t_{CAC} (high to data setup), t_{DHC} (delay from OE), t_{OEZ} (hold after OE).
- U/I/O:** V_{OH} and V_{OL} signals. Timing parameters: t_{RAC} (rise time), t_{AA} (high pulse width), t_{CAC} (high to data setup), t_{CLZ} (hold after UCAS/LCAS).

The diagram shows the sequence of operations: Row Address Strobe (RAS), Column Address Strobe (UCAS/LCAS), Write Enable (WE), and Output Enable (OE). The data bus is shown as "Data out" during the active periods of the address and enable signals.

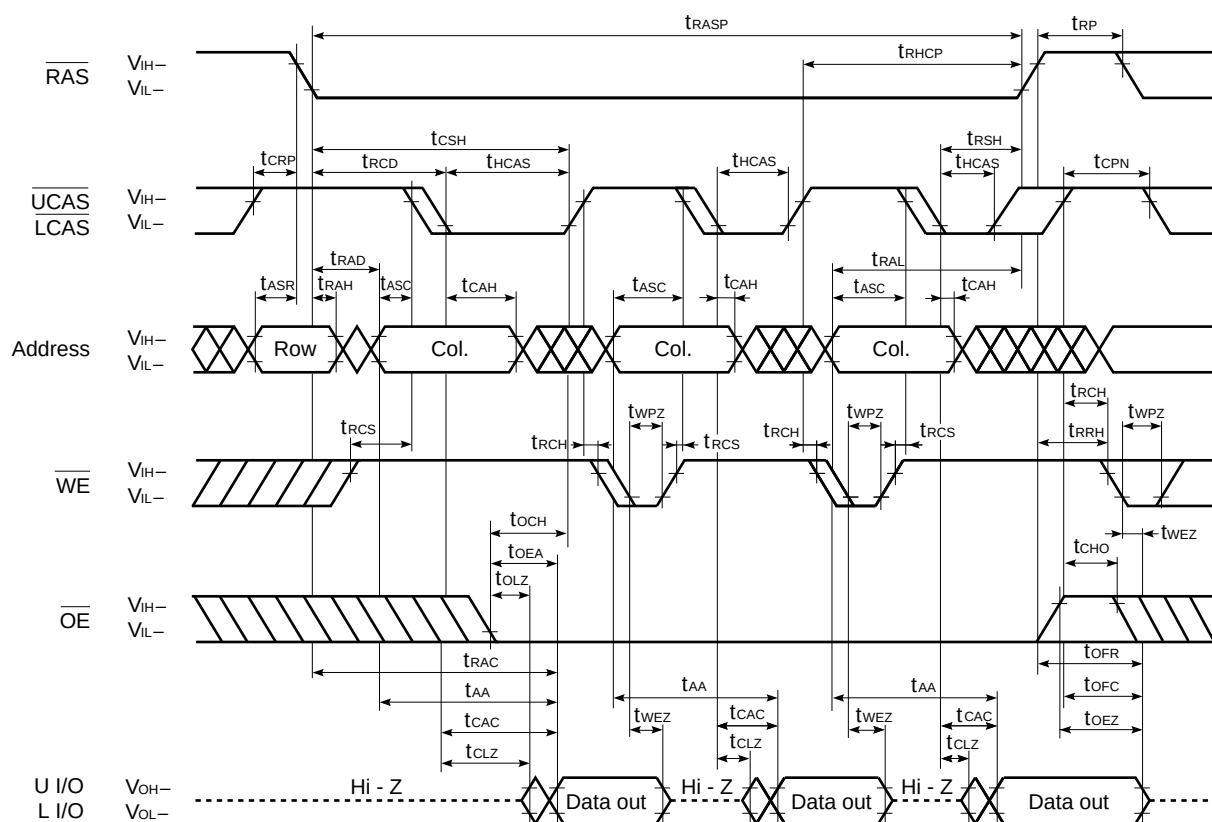
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Hyper Page Mode (EDO) Byte Read Cycle



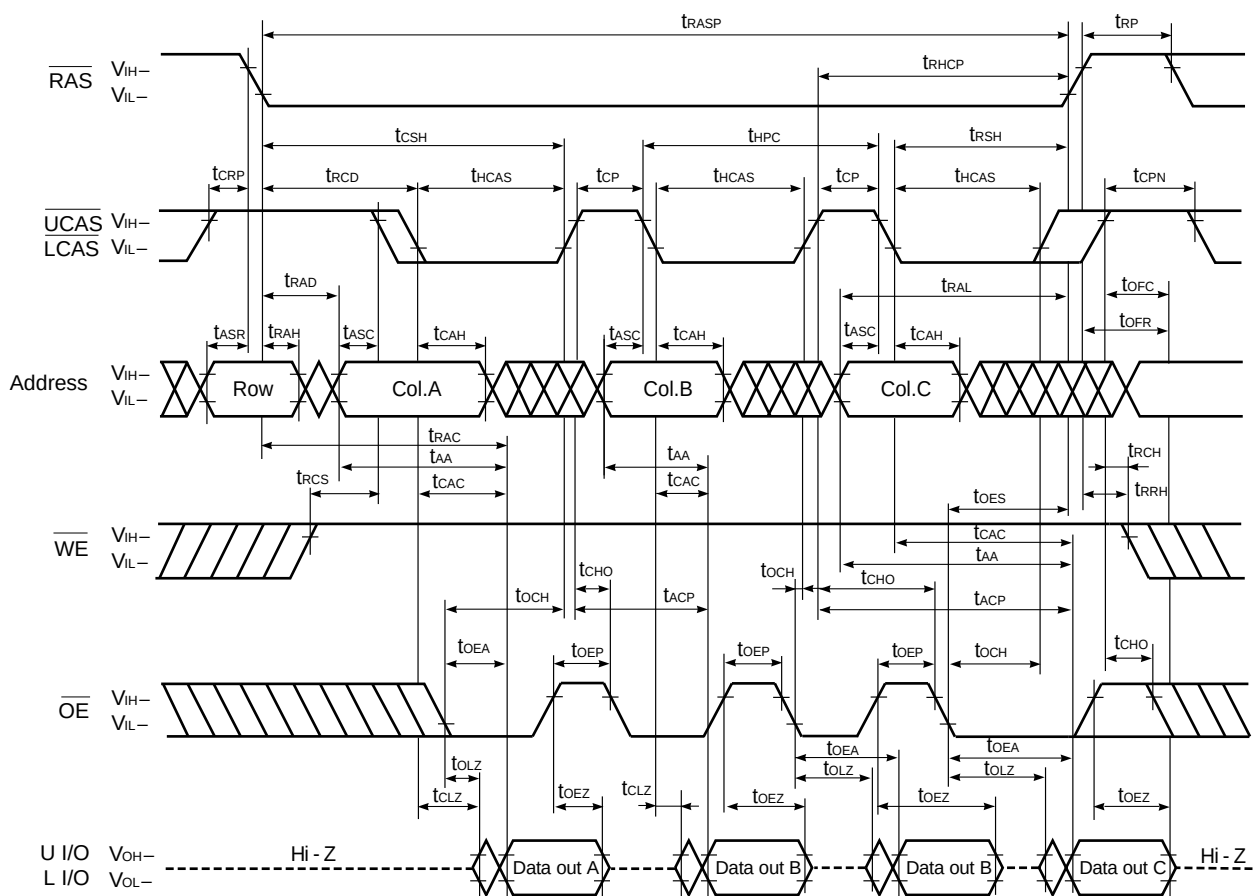
- Remark**
1. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.
 2. This cycle can be used to control either $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ only. Or, it can be used to control $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ simultaneously, or at random.

Hyper Page Mode (EDO) Read Cycle ($\overline{\text{WE}}$ Control)



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Hyper Page Mode (EDO) Read Cycle ($\overline{\text{OE}}$ Control)



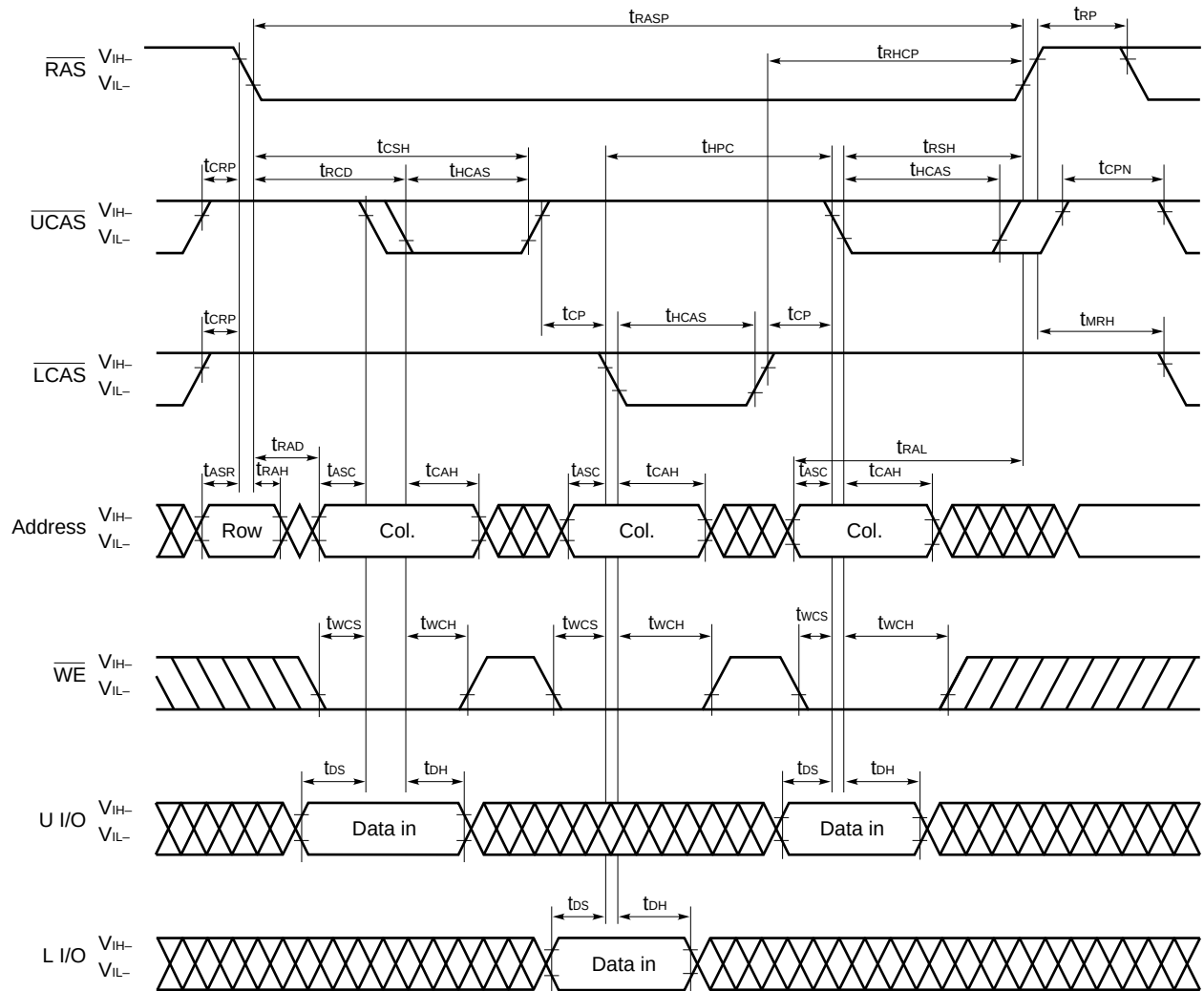
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

The timing diagram illustrates the relationship between several signals and their timing parameters:

- RAS:** Shows the RAS signal with parameters t_{RASP} (RAS pulse width), t_{RHCP} (RAS hold time), and t_{RTP} (RAS to output delay).
- UCAS/LCAS:** Shows the UCAS/LCAS signal with parameters t_{CSH} (UCAS/LCAS setup time), t_{HPC} (UCAS/LCAS hold time), t_{RSH} (UCAS/LCAS to output delay), t_{CRP} (UCAS/LCAS to output delay), t_{RCD} (UCAS/LCAS to output delay), t_{HCAS} (UCAS/LCAS to output delay), t_{CP} (UCAS/LCAS to output delay), t_{CPN} (UCAS/LCAS to output delay), and t_{RAD} (UCAS/LCAS to output delay).
- Address:** Shows the Address signal with parameters t_{ASR} (Address setup time), t_{RAH} (Address hold time), t_{ASC} (Address to output delay), t_{CAH} (Address to output delay), t_{ASC} (Address to output delay), t_{CAH} (Address to output delay), t_{ASC} (Address to output delay), t_{CAH} (Address to output delay), and t_{ASC} (Address to output delay).
- WE:** Shows the WE signal with parameters t_{WCS} (WE setup time), t_{WCH} (WE hold time), t_{WCS} (WE setup time), t_{WCH} (WE hold time), t_{WCS} (WE setup time), t_{WCH} (WE hold time), and t_{WCS} (WE setup time).
- U/I/O L/I/O:** Shows the U/I/O L/I/O signal with parameters t_{DS} (Data setup time), t_{DH} (Data hold time), t_{DS} (Data setup time), t_{DH} (Data hold time), t_{DS} (Data setup time), t_{DH} (Data hold time), and t_{DS} (Data setup time).

2. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

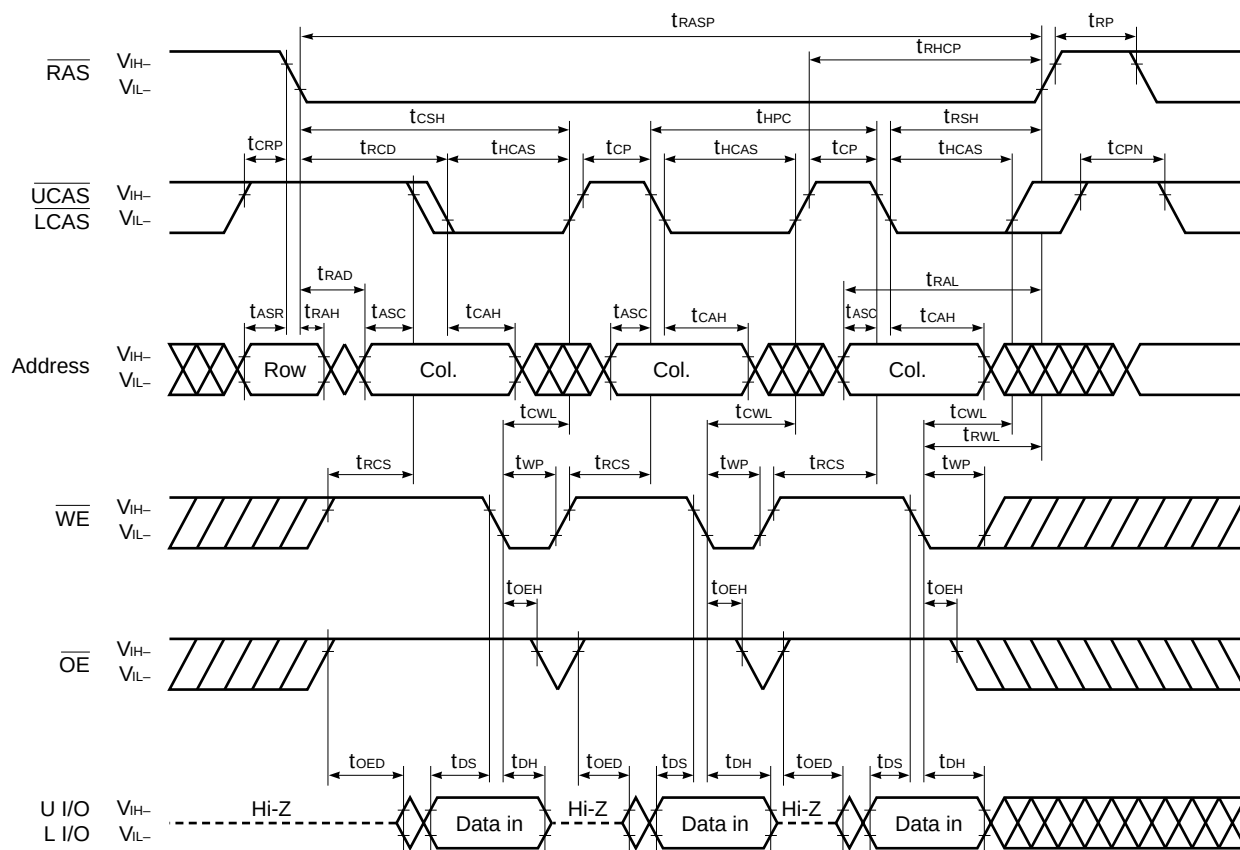
Hyper Page Mode (EDO) Byte Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

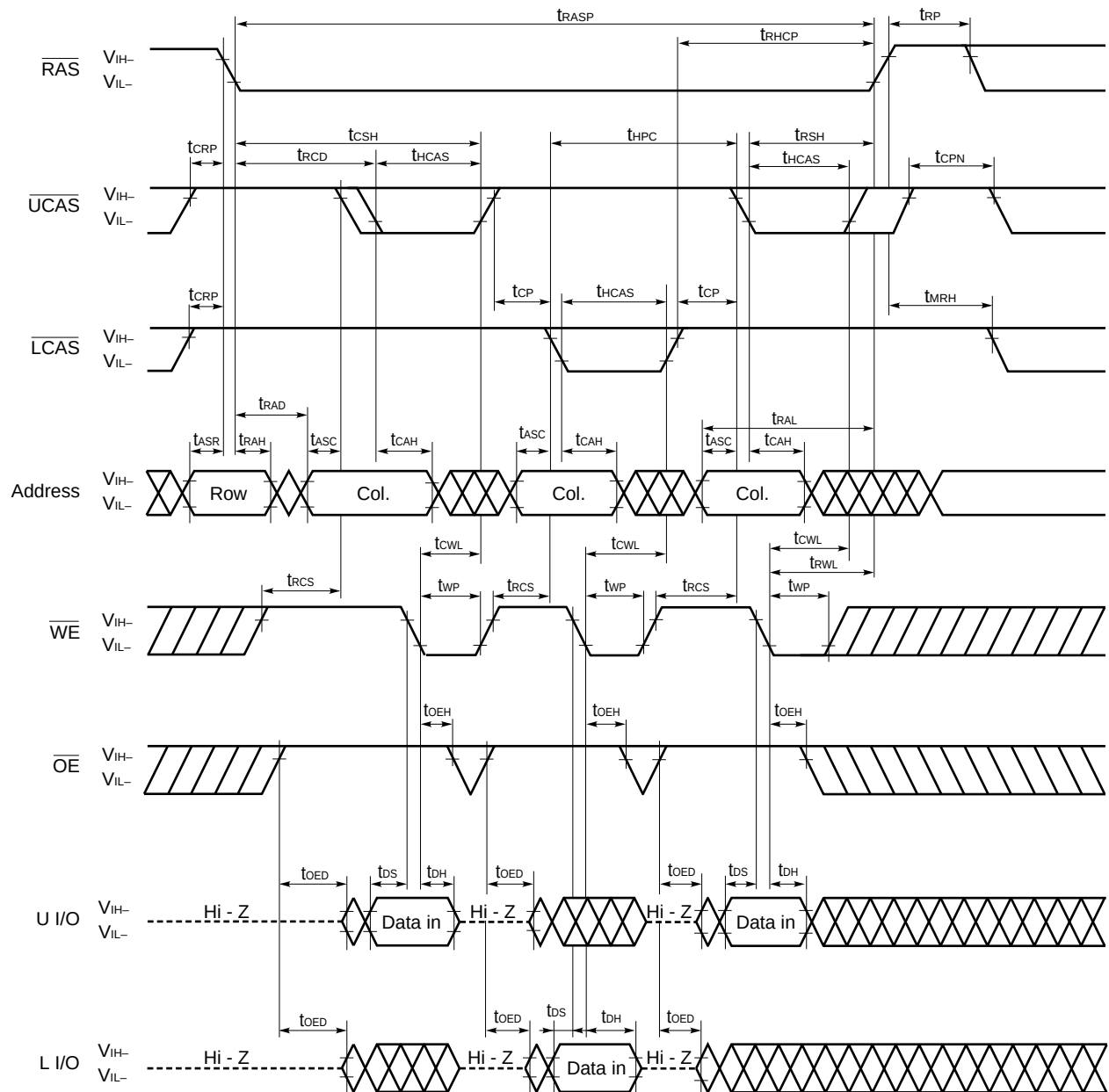
2. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.
3. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Hyper Page Mode (EDO) Late Write Cycle



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Hyper Page Mode (EDO) Byte Late Write Cycle



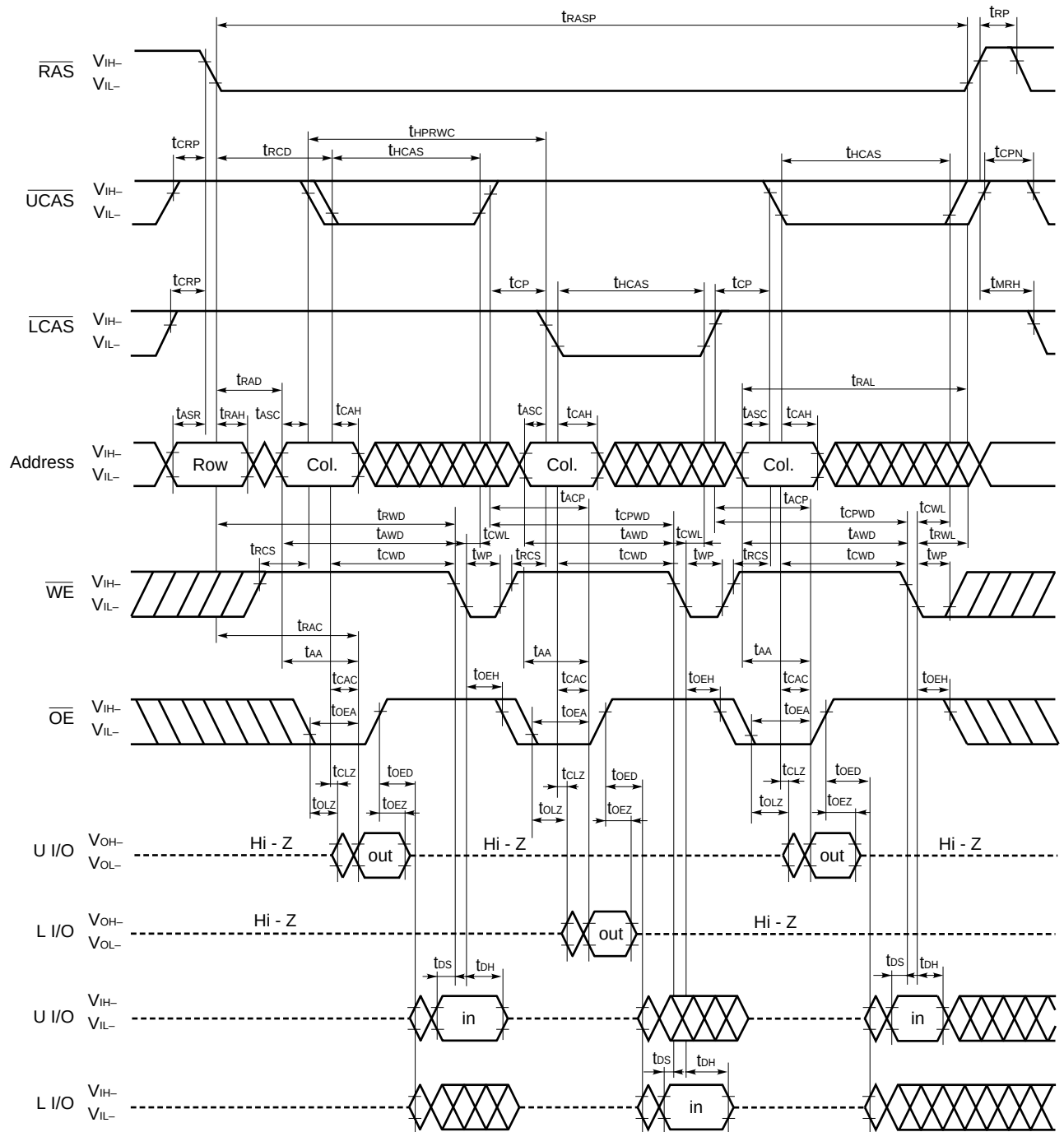
Remarks 1. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

2. This cycle can be used to control either $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ only. Or, it can be used to control $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ simultaneously, or at random.

[illegible]

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Hyper Page Mode (EDO) Byte Read Modify Write Cycle

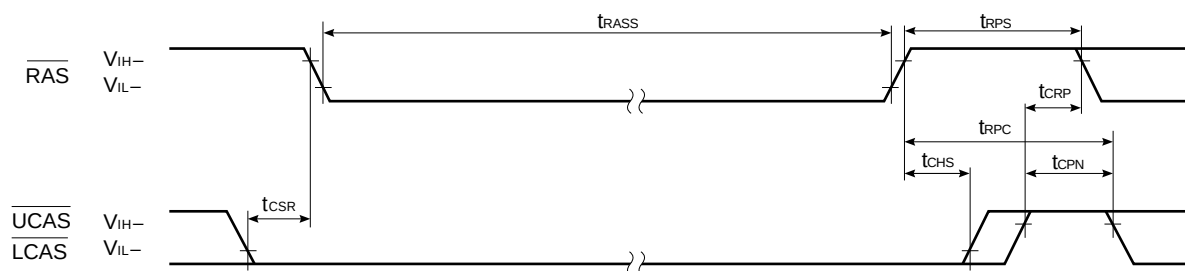


Remarks 1. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

2. This cycle can be used to control either $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ only. Or, it can be used to control $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ simultaneously, or at random.

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CAS Before RAS Self Refresh Cycle (Only for the μPD42S18165)



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Cautions on Use of CAS Before RAS Self Refresh

CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with long RAS only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh

When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh 1,024 times within a 16 ms interval just before and after setting CAS before RAS self refresh.

(2) Normal Combined Use of CAS Before RAS Self Refresh and Long RAS Only Refresh

When CAS before RAS self refresh and RAS only refresh are used in combination, please perform RAS only refresh 1,024 times within a 16 ms interval just before and after setting CAS before RAS self refresh.

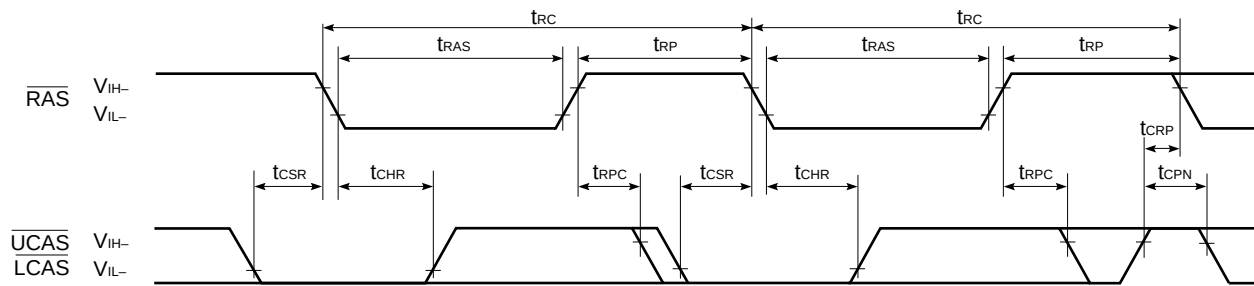
(3) If $t_{RASS(MIN.)}$ is not satisfied at the beginning of CAS before RAS self refresh cycles ($t_{RAS} < 100 \mu s$), CAS before RAS refresh cycles will be executed one time.

If $10 \mu s < t_{RAS} < 100 \mu s$, RAS precharge time for CAS before RAS self refresh (t_{RPS}) is applied.

And refresh cycles (1,024/128 ms) should be met.

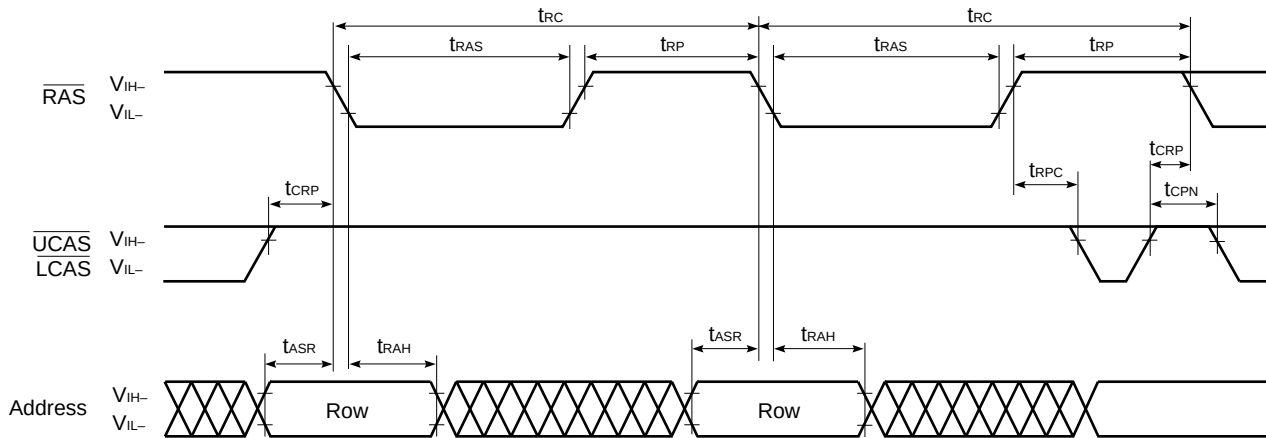
For details, please refer to **How to use DRAM** User's Manual.

CAS Before RAS Refresh Cycle



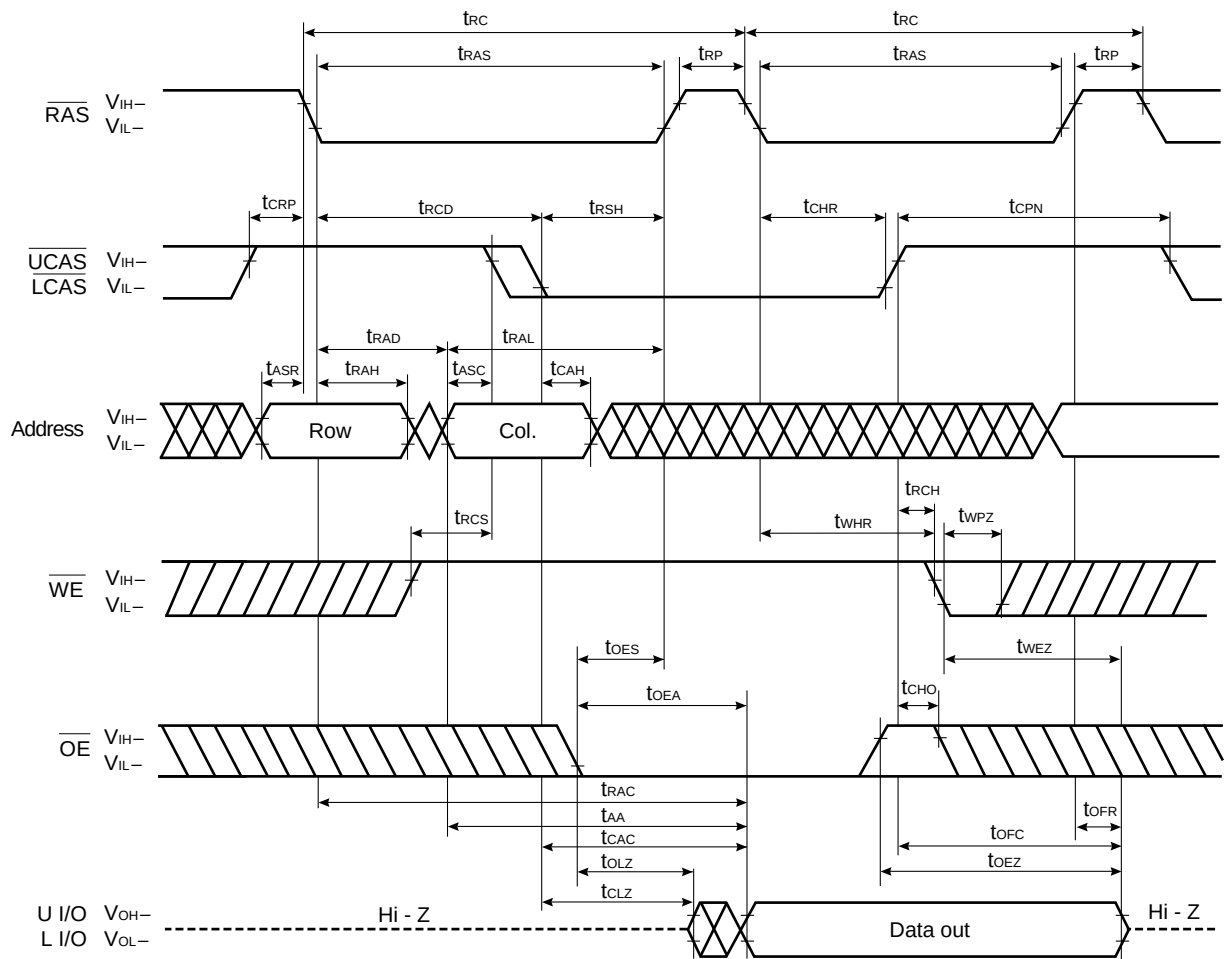
Remark Address, $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care L I/O, U I/O: Hi-Z

RAS Only Refresh Cycle

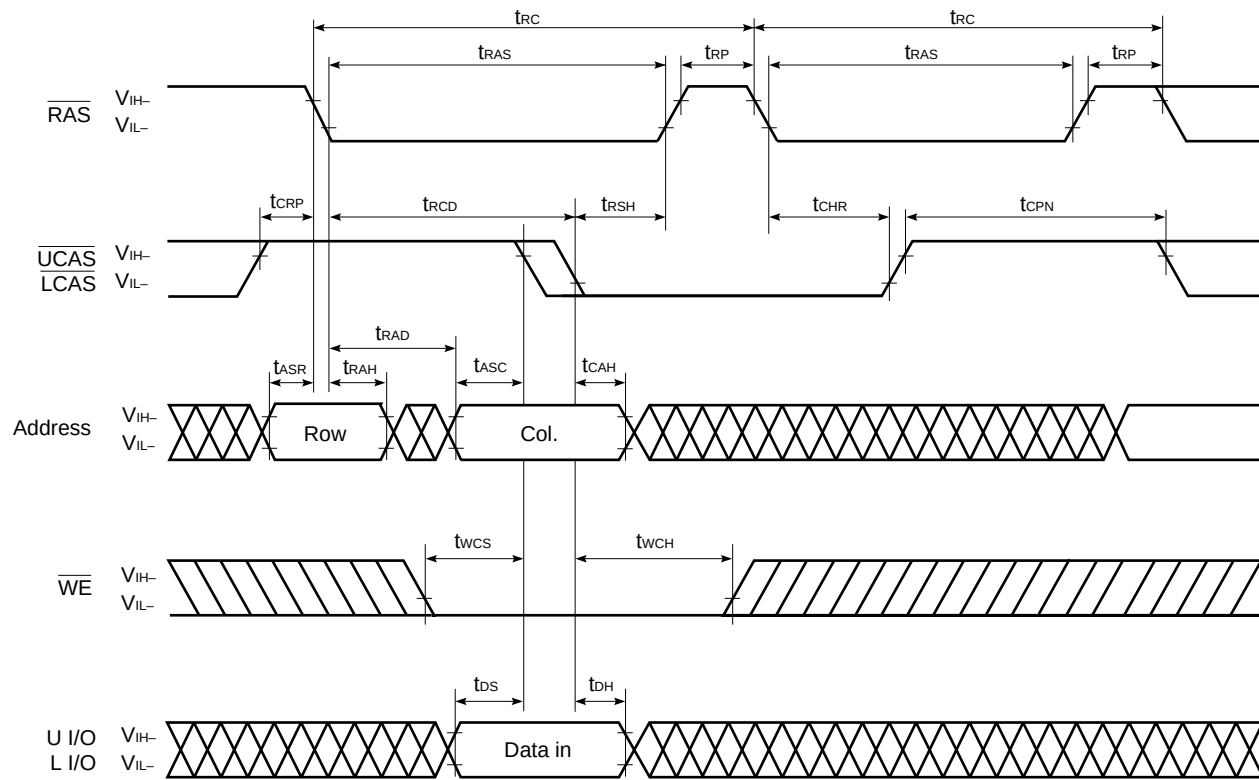


Remark $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care L I/O, U I/O: Hi-Z

Hidden Refresh Cycle (Read)



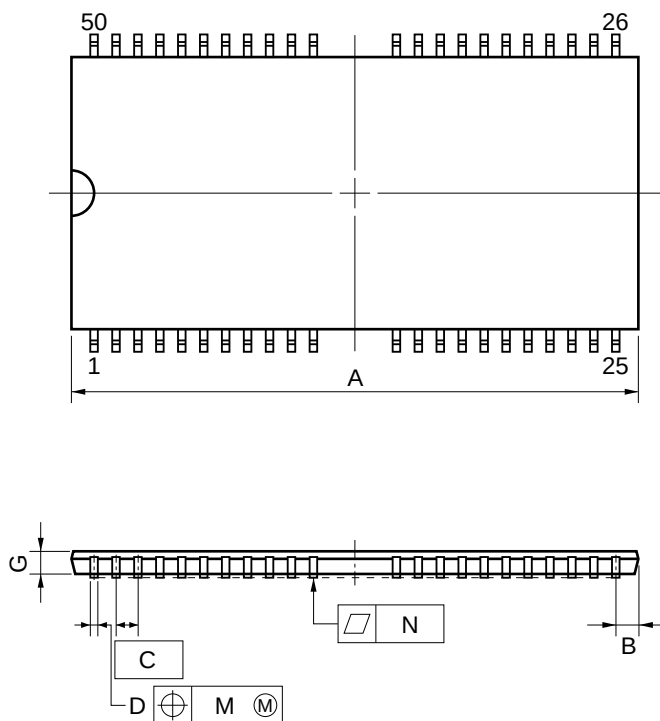
Hidden Refresh Cycle (Write)



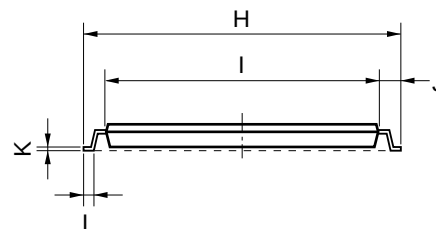
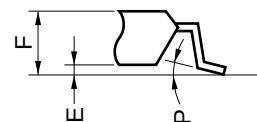
Remark $\overline{\text{OE}}$: Don't care

Package Drawings

50PIN PLASTIC TSOP(II) (400 mil)



detail of lead end



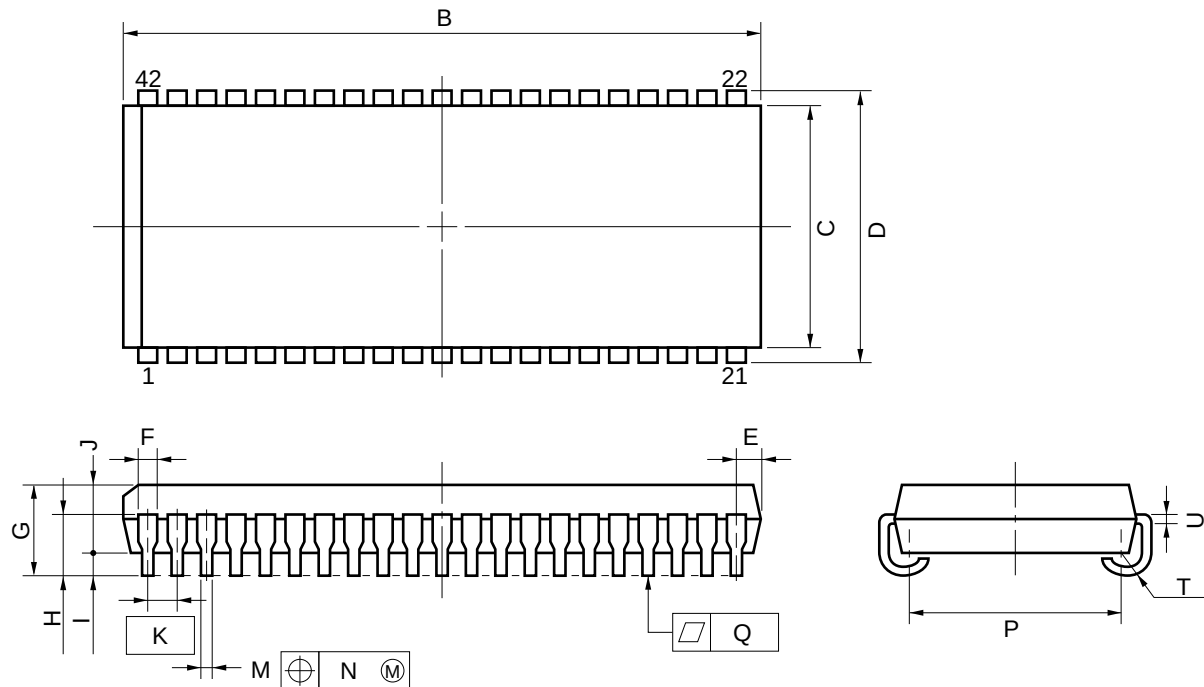
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.32 ^{+0.08} _{-0.07}	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.145 ^{+0.025} _{-0.015}	0.006±0.001
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.13	0.005
N	0.10	0.004
P	3° ^{+7°} _{-3°}	3° ^{+7°} _{-3°}

S50G5-80-7JF4

42 PIN PLASTIC SOJ (400 mil)

**NOTE**

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P42LE-400A

ITEM	MILLIMETERS	INCHES
B	27.56 ^{+0.2} _{-0.35}	1.085 ^{+0.008} _{-0.014}
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.08±0.15	0.043 ^{+0.006} _{-0.007}
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.10	0.004
T	R 0.85	R 0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}

★ Recommended Soldering Conditions

The following conditions (see tables below and next page) must be met for soldering conditions of the μ PD42S18165, 4218165.

For more details, refer to our document “SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL” (C10535E).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

 μ PD42S18165G5-7JF, 4218165G5-7JF: 50-pin plastic TSOP (II) (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 3 Exposure limit: 7 days ^{Note} (10 hours pre-baking is required at 125 °C afterwards)	IR35-107-3
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 3 Exposure limit: 7 days ^{Note} (10 hours pre-baking is required at 125 °C afterwards)	VP15-107-3
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or lower (Per side of the package).	—

Note Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for “Partial heating method”.

μ PD42S18165LE, 4218165LE: 42-pin plastic SOJ (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 3 Exposure limit: 7 days ^{Note} (20 hours pre-baking is required at 125 °C afterwards)	IR35-207-3
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 3 Exposure limit: 7 days ^{Note} (20 hours pre-baking is required at 125 °C afterwards)	VP15-207-3
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or less (Per side of the package).	—

Note Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for “Partial heating method”.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

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While NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customers must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.

NEC devices are classified into the following three quality grades:

"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

Anti-radioactive design is not implemented in this product.