

MOS INTEGRATED CIRCUIT

μ PD42S17405, 4217405

16 M-BIT DYNAMIC RAM 4 M-WORD BY 4-BIT, EDO

Description

The μ PD42S17405, 4217405 are 4,194,304 words by 4 bits CMOS dynamic RAMs with optional EDO.

EDO is a kind of the page mode and is useful for the read operation.

Besides, the μ PD42S17405 can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

The μ PD42S17405, 4217405 are packaged in 26-pin plastic TSOP (II) and 26-pin plastic SOJ.

Features

- EDO (Hyper page mode)
- 4,194,304 words by 4 bits organization
- Single +5.0 V ± 10 % power supply
- Fast access and cycle time

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	EDO (Hyper page mode) cycle time (MIN.)
μ PD42S17405-50, 4217405-50	660 mW	50 ns	84 ns	20 ns
μ PD42S17405-60, 4217405-60	605 mW	60 ns	104 ns	25 ns
μ PD42S17405-70, 4217405-70	550 mW	70 ns	124 ns	30 ns

- μ PD42S17405 can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μ PD42S17405	2,048 cycles/128 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh	1.4 mW (CMOS level input)
μ PD4217405	2,048 cycles/32 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh	5.5 mW (CMOS level input)

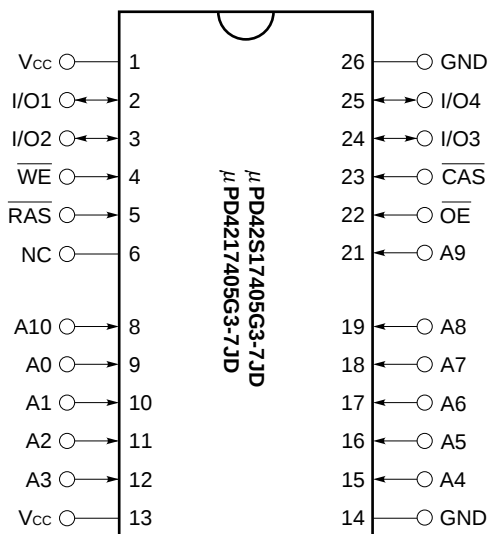
The information in this document is subject to change without notice.

Ordering Information

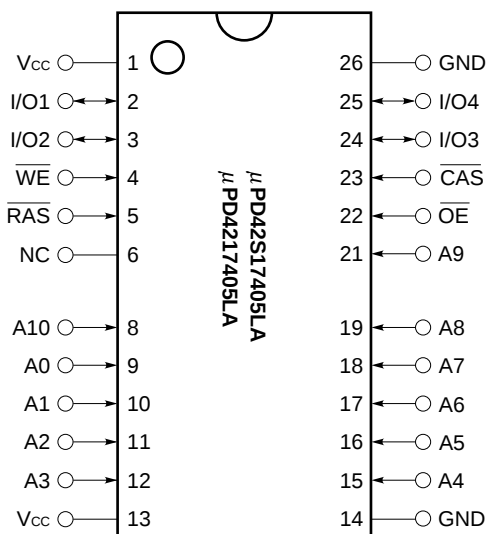
Part number	Access time (MAX.)	Package	Refresh
μ PD42S17405G3-50-7JD	50 ns	26-pin plastic TSOP (II) (300 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD42S17405G3-60-7JD	60 ns		
μ PD42S17405G3-70-7JD	70 ns		
μ PD42S17405LA-50	50 ns	26-pin plastic SOJ (300 mil)	
μ PD42S17405LA-60	60 ns		
μ PD42S17405LA-70	70 ns		
μ PD4217405G3-50-7JD	50 ns	26-pin plastic TSOP (II) (300 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD4217405G3-60-7JD	60 ns		
μ PD4217405G3-70-7JD	70 ns		
μ PD4217405LA-50	50 ns	26-pin plastic SOJ (300 mil)	
μ PD4217405LA-60	60 ns		
μ PD4217405LA-70	70 ns		

Pin Configurations (Marking Side)

26-pin Plastic TSOP (II) (300 mil)

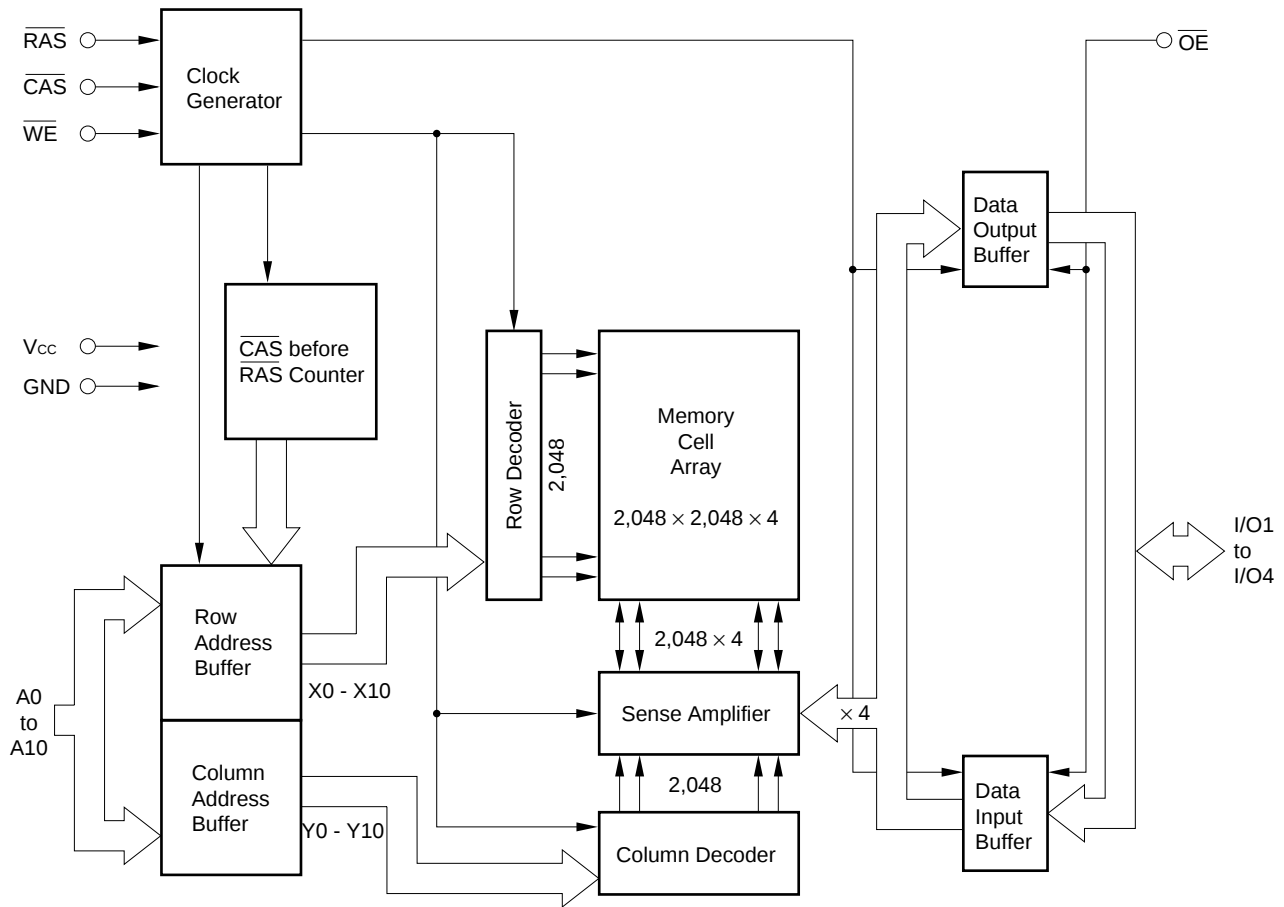


26-pin Plastic SOJ (300 mil)



A0 to A10 : Address Inputs
 I/O1 to I/O4: Data Inputs/Outputs
 $\overline{\text{RAS}}$: Row Address Strobe
 $\overline{\text{CAS}}$: Column Address Strobe
 $\overline{\text{WE}}$: Write Enable
 $\overline{\text{OE}}$: Output Enable
 Vcc : Power Supply
 GND : Ground
 NC : No Connection

Block Diagram



Input/Output Pin Functions

The μ PD42S17405, 4217405 have input pins $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$, A0 to A10 and input/output pins I/O1 to I/O4.

Pin name	Input/Output	Function
$\overline{\text{RAS}}$ (Row address strobe)	Input	$\overline{\text{RAS}}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. CAS before RAS refresh
$\overline{\text{CAS}}$ (Column address strobe)	Input	$\overline{\text{CAS}}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A10 (Address inputs)	Input	Address bus. Input total 22-bit of address signal, upper 11-bit and lower 11-bit in sequence (address multiplex method). Therefore, one word is selected from 4,194,304-word by 4-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{\text{RAS}}$. Then, switch the address bus to column address and activate $\overline{\text{CAS}}$. Each address is taken into the device when $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are activated. Therefore, the address input setup time (t_{ASR} , t_{ASC}) and hold time (t_{RAH} , t_{CAH}) are specified for the activation of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$.
$\overline{\text{WE}}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$.
$\overline{\text{OE}}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{OE}}$. If $\overline{\text{WE}}$ is activated during read operation, $\overline{\text{OE}}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O4 (Data inputs/outputs)	Input/Output	4-bit data bus. I/O1 to I/O4 are used to input/output data.

★ Hyper Page Mode (EDO)

The hyper page mode (EDO) is a kind of page mode with enhanced features. The two major features of the hyper page mode (EDO) are as follows.

1. Data output time is extended.

In the hyper page mode (EDO), the output data is held to the next $\overline{\text{CAS}}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode (EDO) is extended compared with the fast page mode (= data extend function). In the fast page mode, the data output time becomes shorter as the $\overline{\text{CAS}}$ cycle time becomes shorter. Therefore, in the hyper page mode (EDO), the timing margin in read cycle is larger than that of the fast page mode even if the $\overline{\text{CAS}}$ cycle time becomes shorter.

2. The $\overline{\text{CAS}}$ cycle time in the hyper page mode (EDO) is shorter than that in the fast page mode.

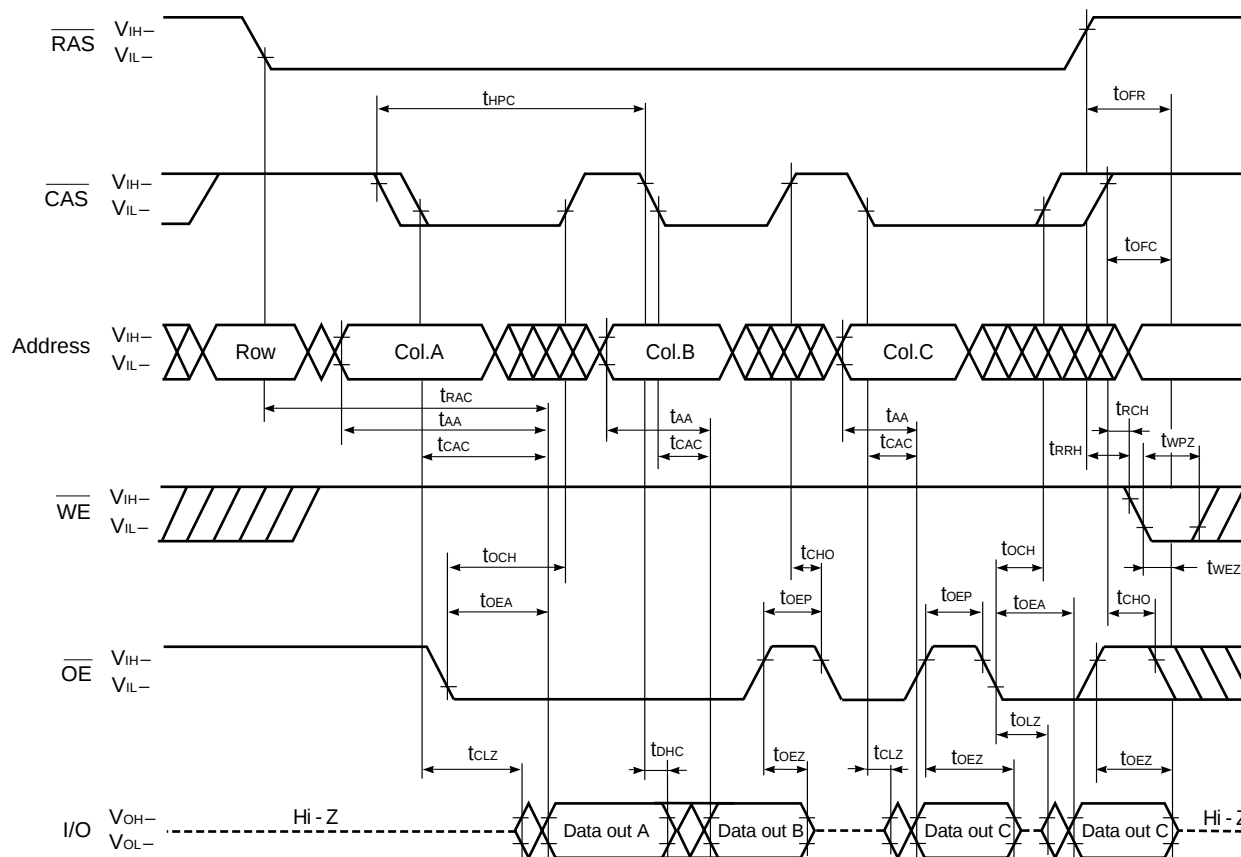
In the hyper page mode (EDO), due to the data extend function, the $\overline{\text{CAS}}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.

Taking a device whose t_{RAC} is 60 ns as an example, the $\overline{\text{CAS}}$ cycle time in the fast page mode is 25 ns while that in the fast page mode is 40 ns.

In the hyper page mode (EDO), read (data out) and write (data in) cycles can be executed repeatedly during one $\overline{\text{RAS}}$ cycle. The hyper page mode (EDO) allows both read and write operations during one cycle.

The following shows a part of the hyper page mode (EDO) read cycle. Specifications to be observed are described in the next page.

Hyper Page Mode (EDO) Read Cycle



Cautions when using the hyper page mode (EDO)

1. $\overline{\text{CAS}}$ access should be used to operate t_{HPC} at the MIN. value.
2. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$ as follows. The effective specification depends on the state of each signal.
 - (1) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are inactive (at the end of read cycle)

$\overline{\text{WE}}$: inactive, $\overline{\text{OE}}$: active

t_{OFC} is effective when $\overline{\text{RAS}}$ is inactivated before $\overline{\text{CAS}}$ is inactivated.

t_{OFR} is effective when $\overline{\text{CAS}}$ is inactivated before $\overline{\text{RAS}}$ is inactivated.

The slower of t_{OFC} and t_{OFR} becomes effective.
 - (2) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are active or either $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ is active (in read cycle)

$\overline{\text{WE}}$, $\overline{\text{OE}}$: inactive t_{OEZ} is effective.

Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are inactive or $\overline{\text{RAS}}$ is active and $\overline{\text{CAS}}$ is inactive (at the end of read cycle)

$\overline{\text{WE}}$, $\overline{\text{OE}}$: active and either t_{RRH} or t_{RCH} must be met t_{WEZ} and t_{WPZ} are effective.

The faster of t_{OEZ} and t_{WEZ} becomes effective.

The faster of (1) and (2) becomes effective.
3. In read cycle, the effective specification depends on the state of $\overline{\text{CAS}}$ signal when controlling data output with the $\overline{\text{OE}}$ signal.
 - (1) $\overline{\text{CAS}}$: inactive, $\overline{\text{OE}}$: active t_{CHO} is effective.
 - (2) $\overline{\text{CAS}}$, $\overline{\text{OE}}$: active t_{CH} is effective.

Electrical Specifications

- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μ s ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		–1.0 to +7.0	V
Supply voltage	V_{CC}		–1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		–55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low level input voltage	V_{IL}		–1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance ($T_A = 25\text{ }^{\circ}\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

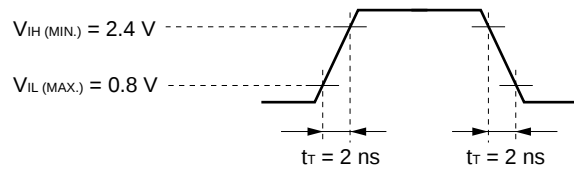
Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current		I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ cycling $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.}), I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 50 \text{ ns}$		120	mA	1, 2, 3
				$t_{\text{RAC}} = 60 \text{ ns}$		110		
				$t_{\text{RAC}} = 70 \text{ ns}$		100		
Standby current	$\mu\text{PD42S17405}$	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.}), I_{\text{O}} = 0 \text{ mA}$		2.0	mA		
			$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}, I_{\text{O}} = 0 \text{ mA}$		0.25			
	$\mu\text{PD4217405}$		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.}), I_{\text{O}} = 0 \text{ mA}$		2.0			
			$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}, I_{\text{O}} = 0 \text{ mA}$		1.0			
$\overline{\text{RAS}}$ only refresh current		I _{CC3}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$ $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.}), I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 50 \text{ ns}$		120	mA	1, 2, 3, 4
				$t_{\text{RAC}} = 60 \text{ ns}$		110		
				$t_{\text{RAC}} = 70 \text{ ns}$		100		
Operating current (Hyper page mode (EDO))		I _{CC4}	$\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.}), \overline{\text{CAS}}$ cycling $t_{\text{HPC}} = t_{\text{HPC}}(\text{MIN.}), I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 50 \text{ ns}$		100	mA	1, 2, 5
				$t_{\text{RAC}} = 60 \text{ ns}$		90		
				$t_{\text{RAC}} = 70 \text{ ns}$		80		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current		I _{CC5}	$\overline{\text{RAS}}$ cycling $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.}), I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 50 \text{ ns}$		120	mA	1, 2
				$t_{\text{RAC}} = 60 \text{ ns}$		110		
				$t_{\text{RAC}} = 70 \text{ ns}$		100		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh current (2,048 cycles / 128 ms, only for the $\mu\text{PD42S17405}$)		I _{CC6}	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh: $t_{\text{RC}} = 62.5 \mu\text{s}$ $\overline{\text{RAS}}, \overline{\text{CAS}}:$ $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}}(\text{MAX.})$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ Standby: $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$ Address: V_{IH} or V_{IL} WE, OE: V_{IH} $I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAS}} \leq 300 \text{ ns}$		400	μA	1, 2
				$t_{\text{RAS}} \leq 1 \mu\text{s}$		500	μA	1, 2
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh current (only for the $\mu\text{PD42S17405}$)		I _{CC7}	$\overline{\text{RAS}}, \overline{\text{CAS}}:$ $t_{\text{RASS}} = 5 \text{ ms}$ $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}}(\text{MAX.})$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ $I_{\text{O}} = 0 \text{ mA}$			250	μA	2
Input leakage current		I _{I (L)}	$V_{\text{I}} = 0 \text{ to } 5.5 \text{ V}$ All other pins not under test = 0 V		-10	+10	μA	
Output leakage current		I _{O (L)}	$V_{\text{O}} = 0 \text{ to } 5.5 \text{ V}$ Output is disabled (Hi-Z)		-10	+10	μA	
High level output voltage		V _{OH}	$I_{\text{O}} = -5.0 \text{ mA}$		2.4		V	
Low level output voltage		V _{OL}	$I_{\text{O}} = +4.2 \text{ mA}$			0.4	V	

- Notes**
1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{HPC}).
 2. Specified values are obtained with outputs unloaded.
 3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.})$ and $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$.
 4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
 5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page (EDO) cycle.

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

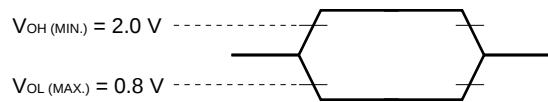
AC Characteristics Test Conditions

(1) Input timing specification

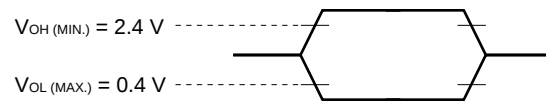


★ (2) Output timing specification

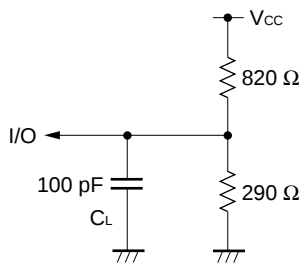
- μ PD42S17405-50, 4217405-50



- μ PD42S17405-60, 4217405-60
- μ PD42S17405-70, 4217405-70



(3) Output loading conditions



Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	$t_{RAC} = 50 \text{ ns}$		$t_{RAC} = 60 \text{ ns}$		$t_{RAC} = 70 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	t_{RC}	84	—	104	—	124	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	30	—	40	—	50	—	ns	
$\overline{CAS}$ precharge time	t_{CPN}	8	—	10	—	10	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	ns	1
$\overline{CAS}$ pulse width	t_{CAS}	8	10,000	10	10,000	12	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	10	—	10	—	12	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	38	—	40	—	50	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	11	37	14	45	14	52	ns	2
$\overline{RAS}$ to column address delay time	t_{RAD}	9	25	12	30	12	35	ns	2
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	5	—	5	—	ns	3
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	7	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	7	—	10	—	12	—	ns	
$\overline{OE}$ lead time referenced to $\overline{RAS}$	t_{OES}	0	—	0	—	0	—	ns	
$\overline{CAS}$ to data setup time	t_{CLZ}	0	—	0	—	0	—	ns	
$\overline{OE}$ to data setup time	t_{OLZ}	0	—	0	—	0	—	ns	
$\overline{OE}$ to data delay time	t_{OED}	10	—	13	—	15	—	ns	
Transition time (rise and fall)	t_t	1	50	1	50	1	50	ns	
Refresh time	μ PD42S17405	t_{REF}	—	128	—	128	—	ms	4
	μ PD4217405		—	32	—	32	—		

Notes 1. In $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, $t_{RAS(MAX.)}$ is 100 μ s.

If $10 \mu\text{s} < t_{RAS} < 100 \mu\text{s}$, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.

2. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

3. $t_{CRP(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

4. This specification is applied only to the μ PD42S17405.

Read Cycle

Parameter	Symbol	$t_{\text{RAC}} = 50 \text{ ns}$		$t_{\text{RAC}} = 60 \text{ ns}$		$t_{\text{RAC}} = 70 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	50	—	60	—	70	ns	1
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	13	—	15	—	18	ns	1
Access time from column address	t_{AA}	—	25	—	30	—	35	ns	1
Access time from $\overline{\text{OE}}$	t_{OEA}	—	13	—	15	—	18	ns	
Column address lead time referenced to $\overline{\text{RAS}}$	t_{RAL}	25	—	30	—	35	—	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time referenced to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	0	—	ns	2
Read command hold time referenced to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	0	—	ns	2
Output buffer turn-off delay time from $\overline{\text{OE}}$	t_{OEZ}	0	10	0	13	0	15	ns	3
$\overline{\text{CAS}}$ hold time to $\overline{\text{OE}}$	t_{CHO}	5	—	5	—	5	—	ns	4

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{\text{RAS}}$
$t_{\text{RAD}} \leq t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{MAX.})$	$t_{\text{RAC}}(\text{MAX.})$	$t_{\text{RAC}}(\text{MAX.})$
$t_{\text{RAD}} > t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{MAX.})$	$t_{\text{AA}}(\text{MAX.})$	$t_{\text{RAD}} + t_{\text{AA}}(\text{MAX.})$
$t_{\text{RCD}} > t_{\text{RCD}}(\text{MAX.})$	$t_{\text{CAC}}(\text{MAX.})$	$t_{\text{RCD}} + t_{\text{CAC}}(\text{MAX.})$

$t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}}(\text{MAX.})$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{MAX.})$ will not cause any operation problems.

2. Either $t_{\text{RCH}}(\text{MIN.})$ or $t_{\text{RRH}}(\text{MIN.})$ should be met in read cycles.
3. $t_{\text{OEZ}}(\text{MAX.})$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL} .
4. $\overline{\text{WE}}$: inactive (in read cycle)
 $\overline{\text{CAS}}$: inactive, $\overline{\text{OE}}$: active t_{CHO} is effective.
 $\overline{\text{CAS}}$, $\overline{\text{OE}}$: active t_{OCH} is effective.

Write Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t _{WCH}	7	–	10	–	10	–	ns	1
$\overline{WE}$ pulse width	t _{WP}	8	–	10	–	10	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t _{RWL}	10	–	10	–	12	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t _{CWL}	8	–	10	–	12	–	ns	
$\overline{WE}$ setup time	t _{WCS}	0	–	0	–	0	–	ns	2
$\overline{OE}$ hold time	t _{OEH}	0	–	0	–	0	–	ns	
Data-in setup time	t _{DS}	0	–	0	–	0	–	ns	3
Data-in hold time	t _{DH}	7	–	10	–	10	–	ns	3

- Notes**
1. t_{WP} (MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, t_{WCH} (MIN.) should be met.
 2. If t_{WCS} ≥ t_{WCS} (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
 3. t_{DS} (MIN.) and t_{DH} (MIN.) are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t _{RWC}	107	–	133	–	157	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t _{RWD}	64	–	77	–	89	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t _{CWD}	27	–	32	–	37	–	ns	1
Column address to $\overline{WE}$ delay time	t _{AWD}	39	–	47	–	54	–	ns	1

- Note**
1. If t_{WCS} ≥ t_{WCS} (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If t_{RWD} ≥ t_{RWD} (MIN.), t_{CWD} ≥ t_{CWD} (MIN.), t_{AWD} ≥ t_{AWD} (MIN.) and t_{CPWD} ≥ t_{CPWD} (MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode (EDO)

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	t _{HPC}	20	—	25	—	30	—	ns	1
$\overline{\text{RAS}}$ pulse width	t _{RASP}	50	125,000	60	125,000	70	125,000	ns	
★ $\overline{\text{CAS}}$ pulse width	t _{HCAS}	8	10,000	10	10,000	12	10,000	ns	
★ $\overline{\text{CAS}}$ precharge time	t _{CP}	8	—	10	—	10	—	ns	
Access time from $\overline{\text{CAS}}$ precharge	t _{ACP}	—	30	—	35	—	40	ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$ delay time	t _{CPWD}	41	—	52	—	59	—	ns	2
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t _{RHCP}	30	—	35	—	40	—	ns	
Read modify write cycle time	t _{HPRWC}	52	—	66	—	75	—	ns	
Data output hold time	t _{DHC}	5	—	5	—	5	—	ns	
$\overline{\text{OE}}$ to $\overline{\text{CAS}}$ hold time	t _{OCH}	5	—	5	—	5	—	ns	3
$\overline{\text{OE}}$ precharge time	t _{OEP}	5	—	5	—	5	—	ns	
Output buffer turn-off delay from $\overline{\text{WE}}$	t _{WEZ}	0	10	0	13	0	15	ns	4,5
★ $\overline{\text{WE}}$ pulse width	t _{WPZ}	8	—	10	—	10	—	ns	5
Output buffer turn-off delay from $\overline{\text{RAS}}$	t _{OFR}	0	10	0	13	0	15	ns	4,5
Output buffer turn-off delay from $\overline{\text{CAS}}$	t _{OFC}	0	10	0	13	0	15	ns	4,5

Notes 1. t_{HPC} (MIN.) is applied to $\overline{\text{CAS}}$ access.

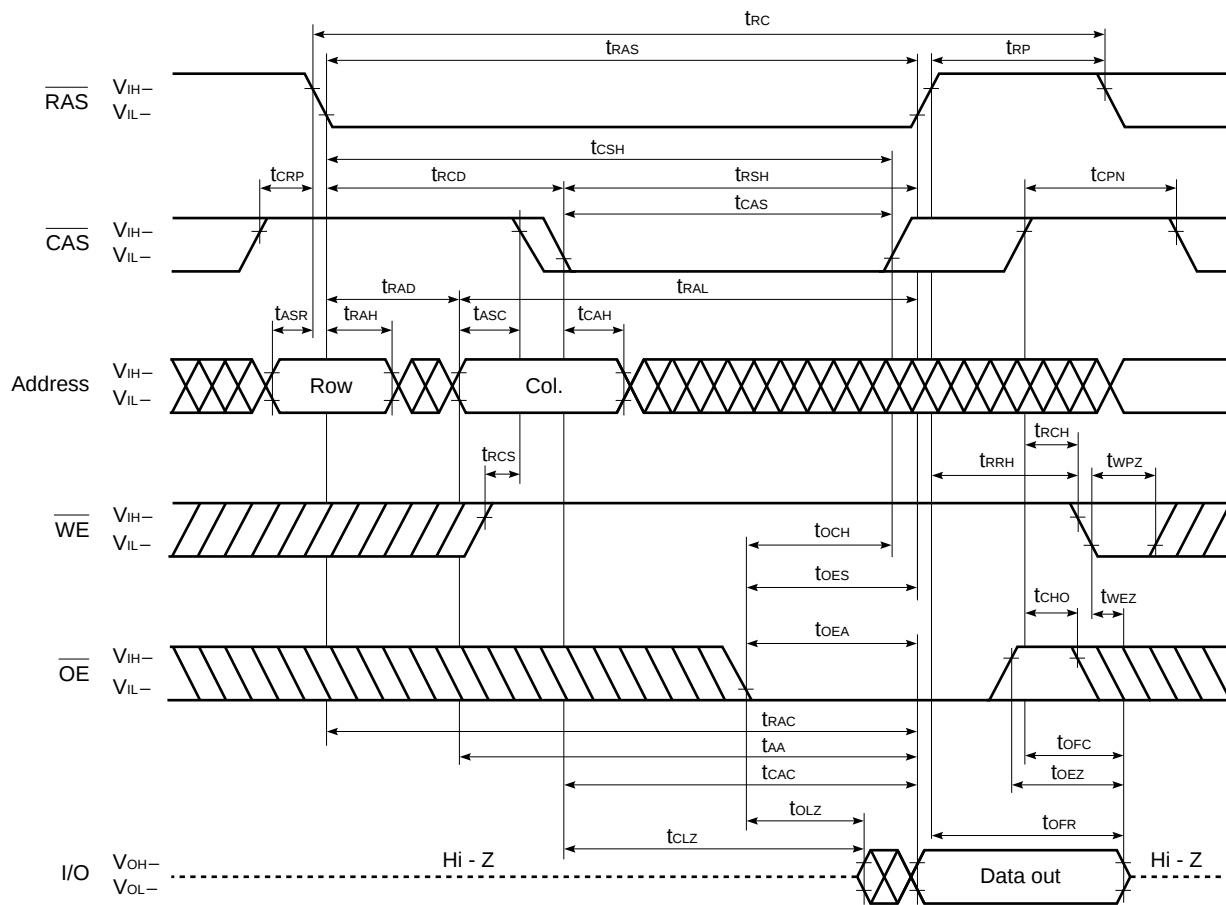
2. If t_{WCS} ≥ t_{WCS} (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If t_{RWD} ≥ t_{RWD} (MIN.), t_{CWD} ≥ t_{CWD} (MIN.), t_{AWD} ≥ t_{AWD} (MIN.) and t_{CPWD} ≥ t_{CPWD} (MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.
 3. $\overline{\text{WE}}$: inactive (in read cycle)
 $\overline{\text{CAS}}$: inactive, $\overline{\text{OE}}$: active t_{CHO} is effective.
 $\overline{\text{CAS}}$, $\overline{\text{OE}}$: active t_{OCH} is effective.
 4. t_{OFC} (MAX.), t_{OFR} (MAX.) and t_{WEZ} (MAX.) define the time when the output achieves the conditions of Hi-Z and is not referenced to V_{OH} or V_{OL}.
 5. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$ as follows. The effective specification depends on state of each signal.
 - (1) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are inactive (at the end of the read cycle)
 $\overline{\text{WE}}$: inactive, $\overline{\text{OE}}$: active
 t_{OFC} is effective when $\overline{\text{RAS}}$ is inactivated before $\overline{\text{CAS}}$ is inactivated.
 t_{OFR} is effective when $\overline{\text{CAS}}$ is inactivated before $\overline{\text{RAS}}$ is inactivated.
 The slower of t_{OFC} and t_{OFR} becomes effective.
 - (2) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are active or either $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ is active (in read cycle)
 $\overline{\text{WE}}$, $\overline{\text{OE}}$: inactive t_{OEZ} is effective.
 Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are inactive or $\overline{\text{RAS}}$ is active and $\overline{\text{CAS}}$ is inactive (at the end of read cycle)
 $\overline{\text{WE}}$, $\overline{\text{OE}}$: active and either t_{RRH} or t_{TRCH} must be met t_{WEZ} and t_{WPZ} are effective.
 The faster of t_{OEZ} and t_{WEZ} becomes effective.
- The faster of (1) and (2) becomes effective.

Refresh Cycle

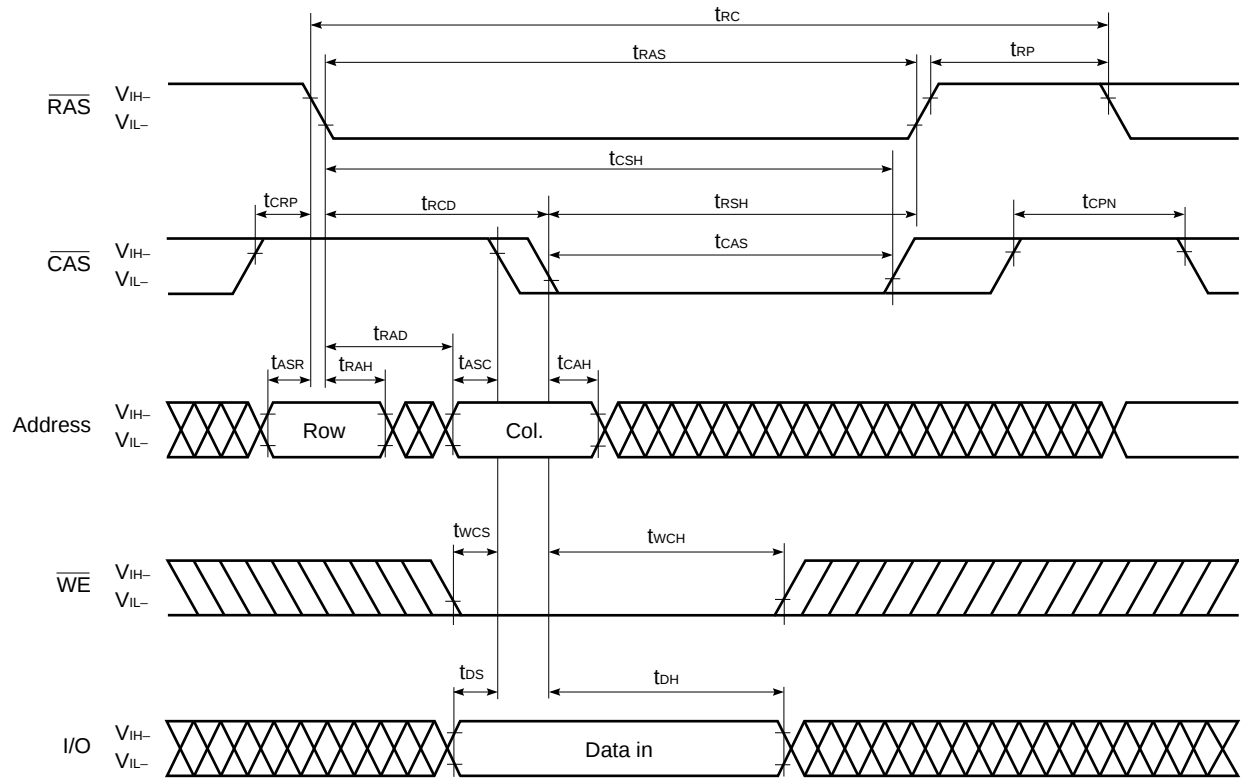
Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{\text{CAS}}$ setup time	t _{CSR}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh)	t _{CHR}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ precharge $\overline{\text{CAS}}$ hold time	t _{RPC}	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ pulse width ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh)	t _{RASS}	100	—	100	—	100	—	μs	1
$\overline{\text{RAS}}$ precharge time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh)	t _{RPS}	90	—	110	—	130	—	ns	1
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh)	t _{CHS}	−50	—	−50	—	−50	—	ns	1
$\overline{\text{WE}}$ setup time	t _{WSR}	10	—	10	—	10	—	ns	
$\overline{\text{WE}}$ hold time	t _{WHR}	15	—	15	—	15	—	ns	

Note 1. This specification is applied only to the μPD42S17405.

Read Cycle

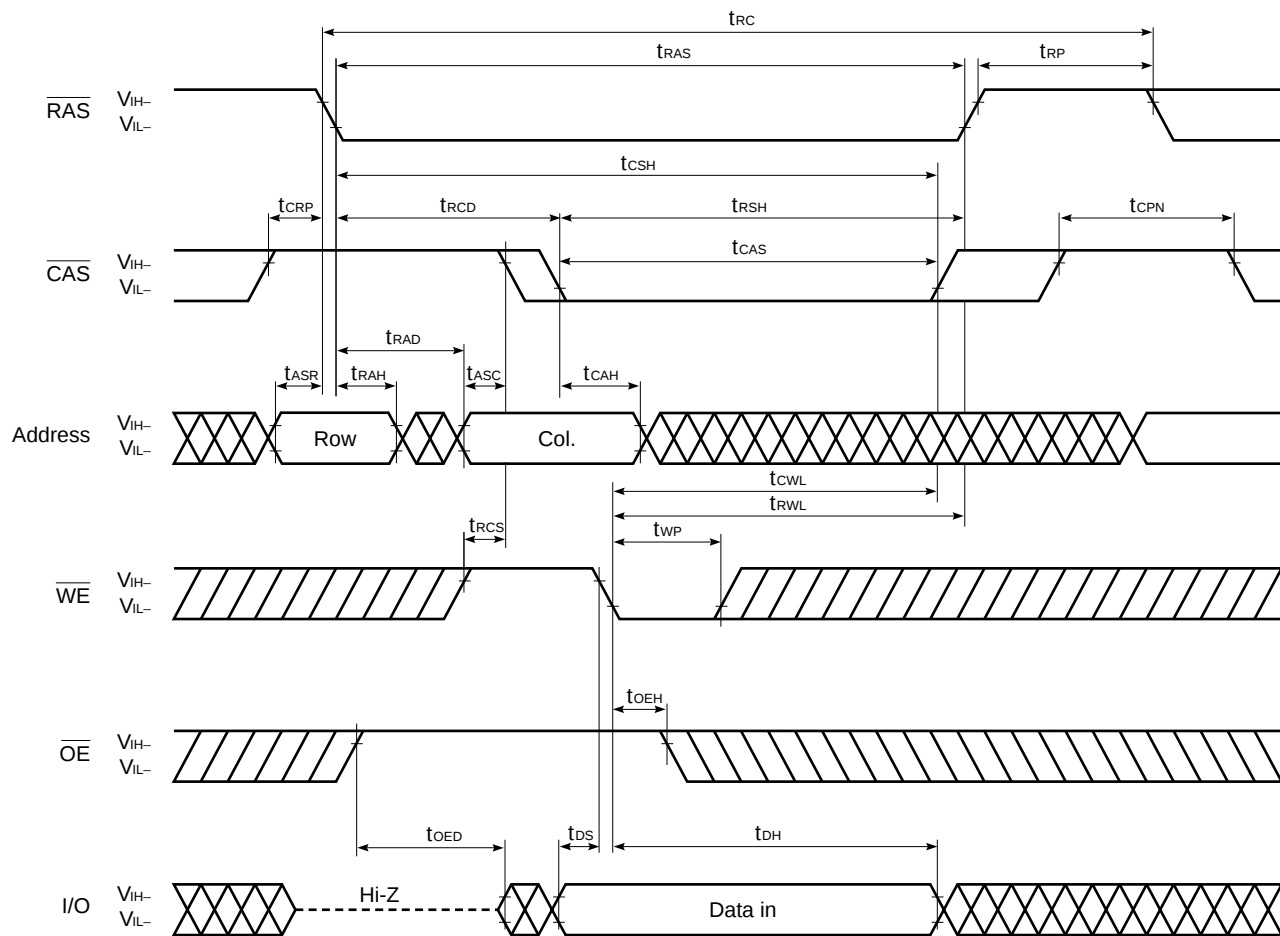


Early Write Cycle

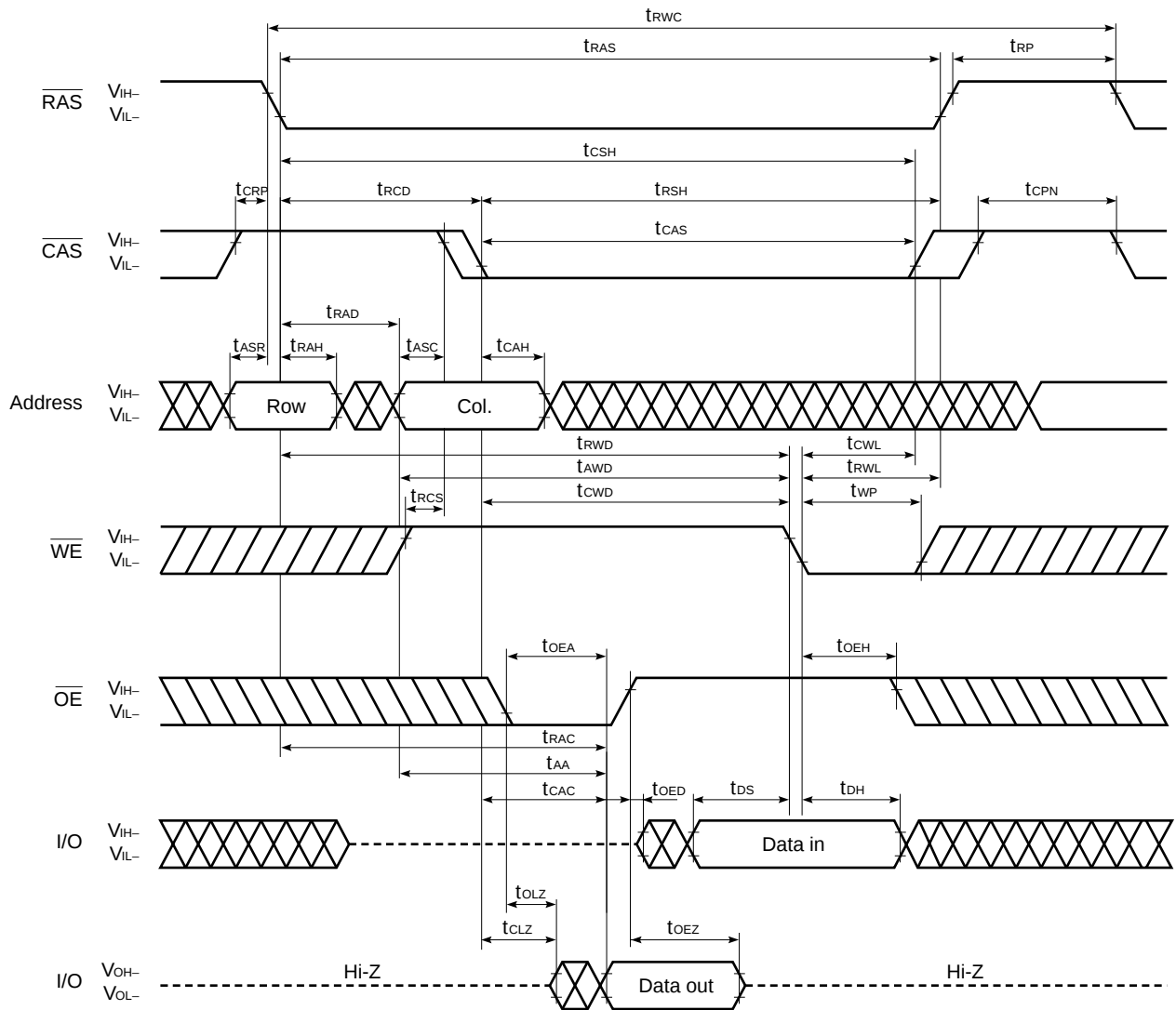


Remark $\overline{OE}$: Don't care

Late Write Cycle



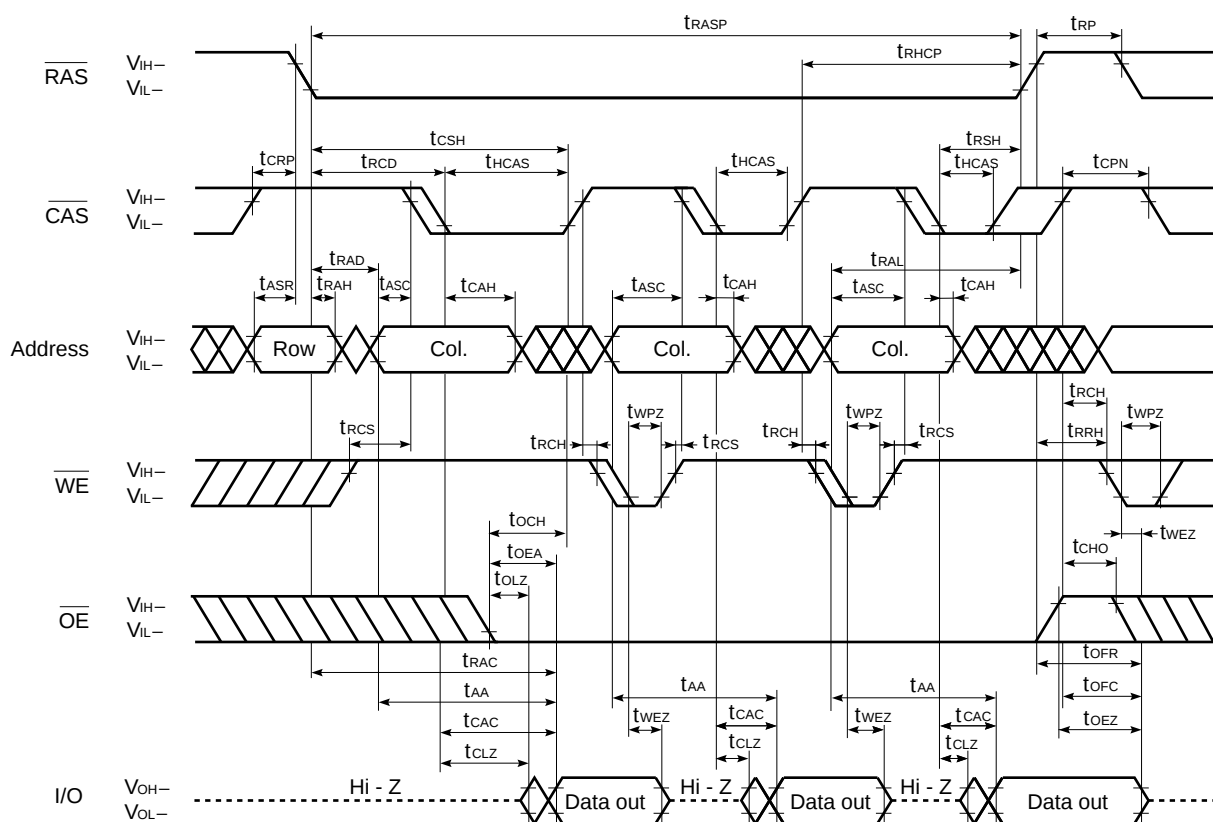
Read Modify Write Cycle



[illegible]

20

Hyper Page Mode (EDO) Read Cycle ($\overline{\text{WE}}$ Control)

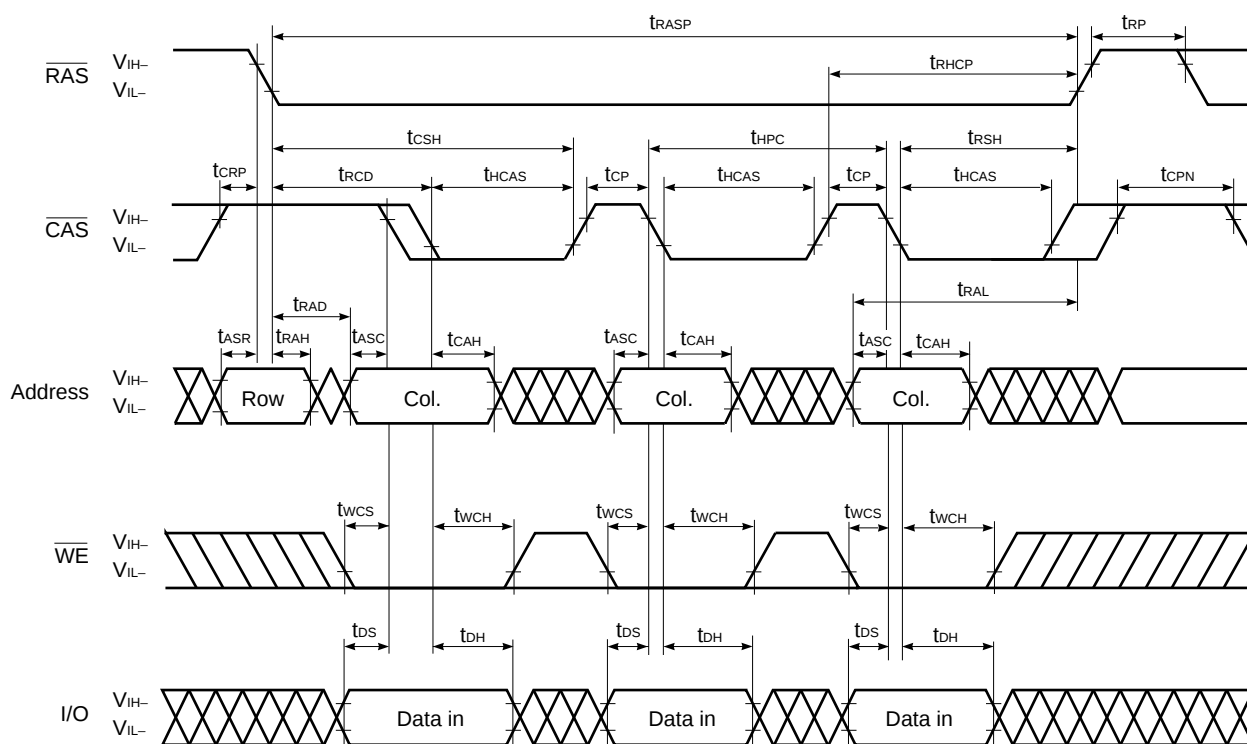


Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

[illegible]

22

Hyper Page Mode (EDO) Early Write Cycle



Remarks 1. $\overline{\text{OE}}$: Don't care

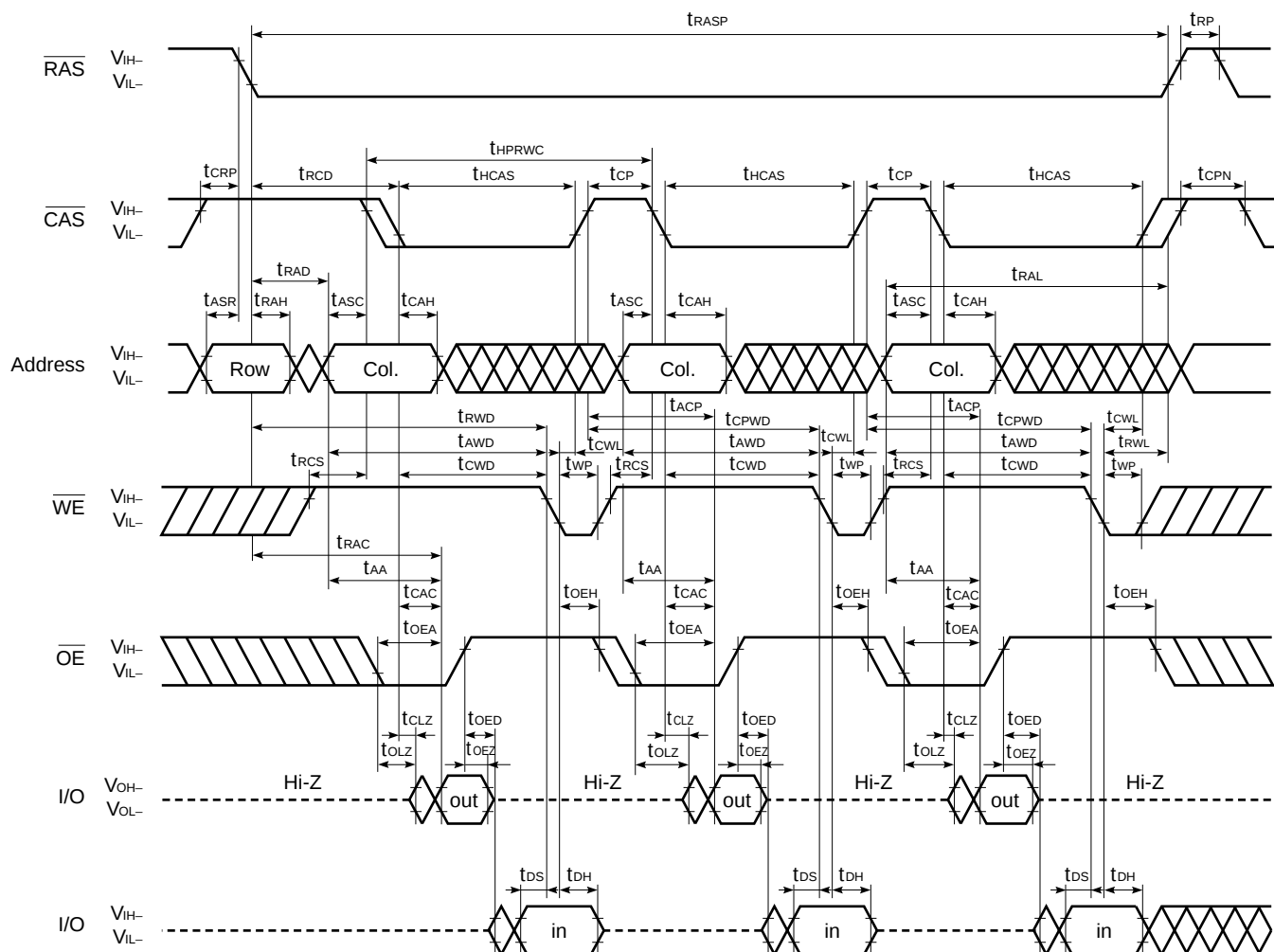
2. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

The diagram illustrates the timing relationships for a 256Kbit DRAM. The signals and their timing parameters are as follows:

- RAS:** $\overline{\text{RAS}}$ signal. Timing parameters: t_{RASP} (RAS pulse width), t_{RHCP} (RAS hold time), t_{RP} (RAS precharge time).
- CAS:** $\overline{\text{CAS}}$ signal. Timing parameters: t_{CRP} (CAS precharge time), t_{RCD} (RAS to CAS delay), t_{HCAS} (CAS high pulse width), t_{CP} (CAS precharge time), t_{CPN} (CAS precharge time).
- Address:** Signal for Row and Column addresses. Timing parameters: t_{ASR} (Address setup time), t_{RAH} (Address hold time), t_{ASC} (Address setup time), t_{CAH} (Address hold time), t_{RAD} (Row address delay), t_{RAL} (Row address delay).
- WE:** $\overline{\text{WE}}$ signal. Timing parameters: t_{RCS} (Row to Column Setup time), t_{WTP} (Write pulse width), t_{RCWL} (Row to Column Write Latency), t_{RWL} (Row to Column Write Latency).
- OE:** $\overline{\text{OE}}$ signal. Timing parameters: t_{OEHL} (Output Enable High Latency), t_{OEHL} (Output Enable High Latency).
- I/O:** Data bus signal. Timing parameters: t_{OED} (Output Enable Delay), t_{DS} (Data Setup time), t_{DH} (Data Hold time).

Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Hyper Page Mode (EDO) Read Modify Write Cycle



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

The diagram illustrates the timing relationships for a 256K16 DRAM. It shows the signals RAS, CAS, Address, WE, OE, and I/O (Data out and Data in) over time. The signals are represented by digital waveforms, and the timing parameters are indicated by arrows and labels. The signals are labeled as follows:

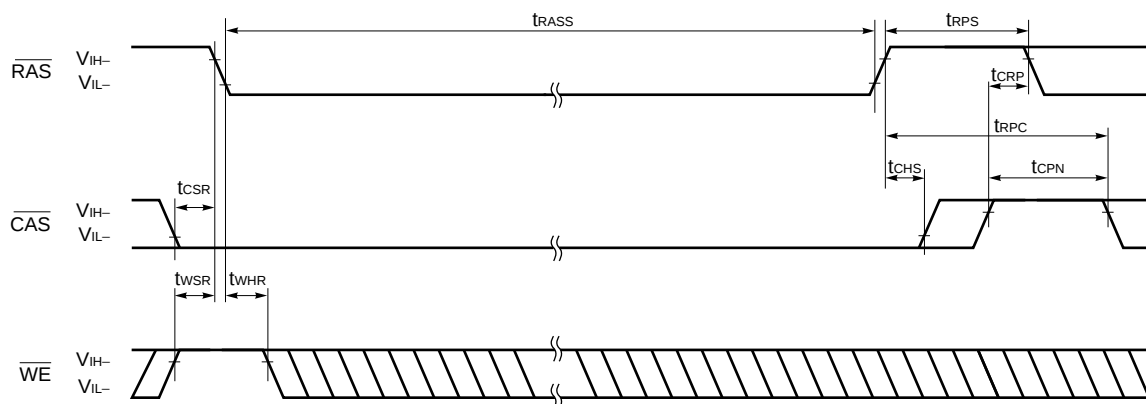
- RAS:** RAS input signal, with timing parameters t_{RASP} , t_{RHP} , and t_{RP} .
- CAS:** CAS input signal, with timing parameters t_{CRP} , t_{RCD} , t_{HCS} , t_{CP} , t_{HPC} , t_{RSH} , t_{HCS} , and t_{CPN} .
- Address:** Address input signal, with timing parameters t_{ASR} , t_{RAH} , t_{ASC} , t_{CAH} , t_{ASC} , t_{CAH} , t_{ASC} , t_{CAH} , and t_{RAL} .
- WE:** Write Enable input signal, with timing parameters t_{RCS} , t_{RCH} , t_{WCS} , and t_{WCH} .
- OE:** Output Enable input signal, with timing parameters t_{OCH} , t_{OE} , t_{OLZ} , t_{AA} , t_{CAC} , t_{CLZ} , t_{DHC} , t_{OEZ} , and t_{WEZ} .
- I/O:** Data out and Data in signals, with timing parameters t_{DS} and t_{DH} .

The diagram also shows the Hi-Z (High Impedance) state for the I/O signals. The signals are labeled as follows:

- Hi-Z:** High Impedance state for the I/O signals.
- Data out:** Data output signal.
- Data in:** Data input signal.

26

CAS Before RAS Self Refresh Cycle (Only for the μPD42S17405)



Remark Address, $\overline{OE}$: Don't care I/O : Hi-Z

Cautions on Use of CAS Before RAS Self Refresh

CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with long RAS only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh

When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh 2,048 times within a 32 ms interval just before and after setting CAS before RAS self refresh.

(2) Normal Combined Use of CAS Before RAS Self Refresh and Long RAS Only Refresh

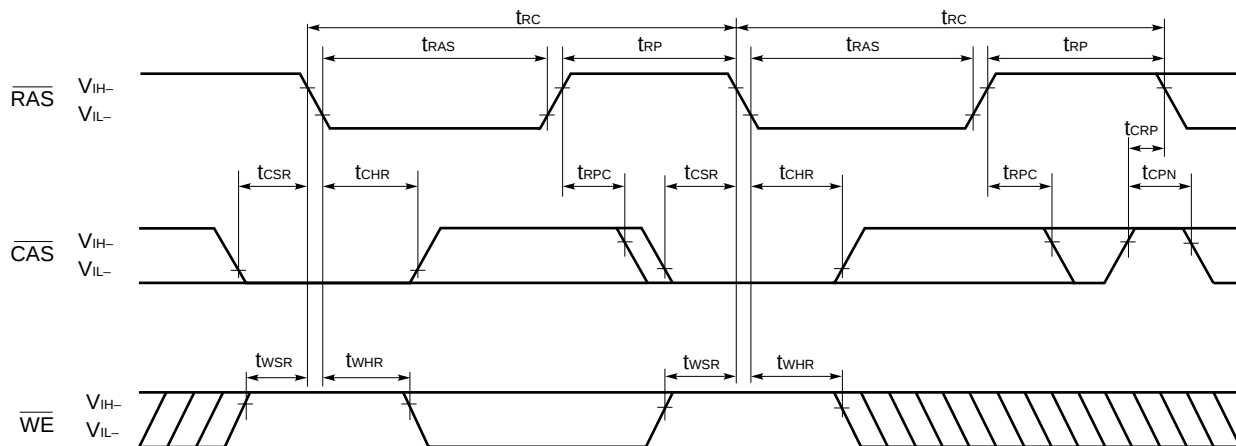
When CAS before RAS self refresh and RAS only refresh are used in combination, please perform RAS only refresh 2,048 times within a 32 ms interval just before and after setting CAS before RAS self refresh.

(3) If $t_{RASS(MIN.)}$ is not satisfied at the beginning of CAS before RAS self refresh cycles ($t_{RAS} < 100 \mu s$), CAS before RAS refresh cycles will be executed one time.

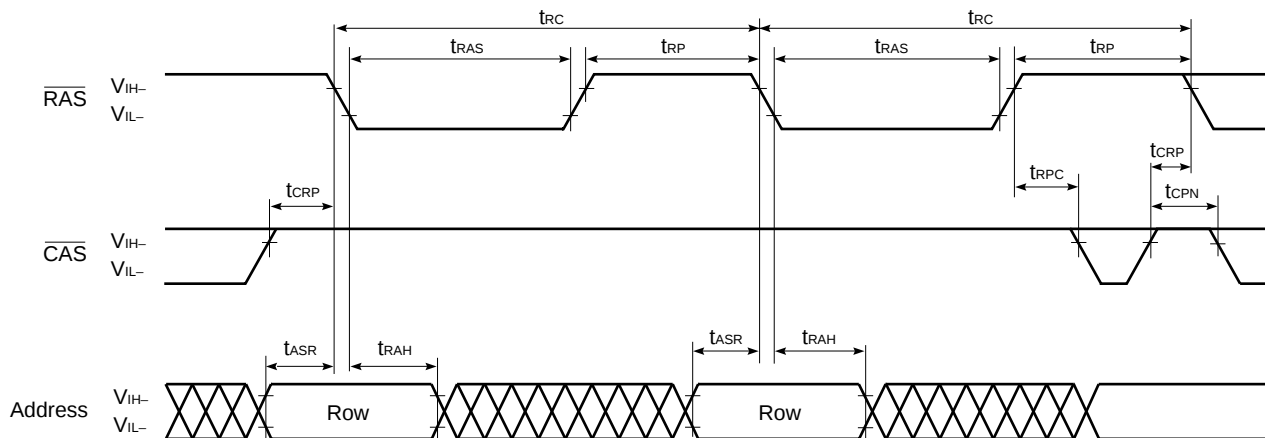
If $10 \mu s < t_{RAS} < 100 \mu s$, RAS precharge time for CAS before RAS self refresh (t_{RPS}) is applied.

And refresh cycles (2,048/128 ms) should be met.

For details, please refer to **How to use DRAM** User's Manual.

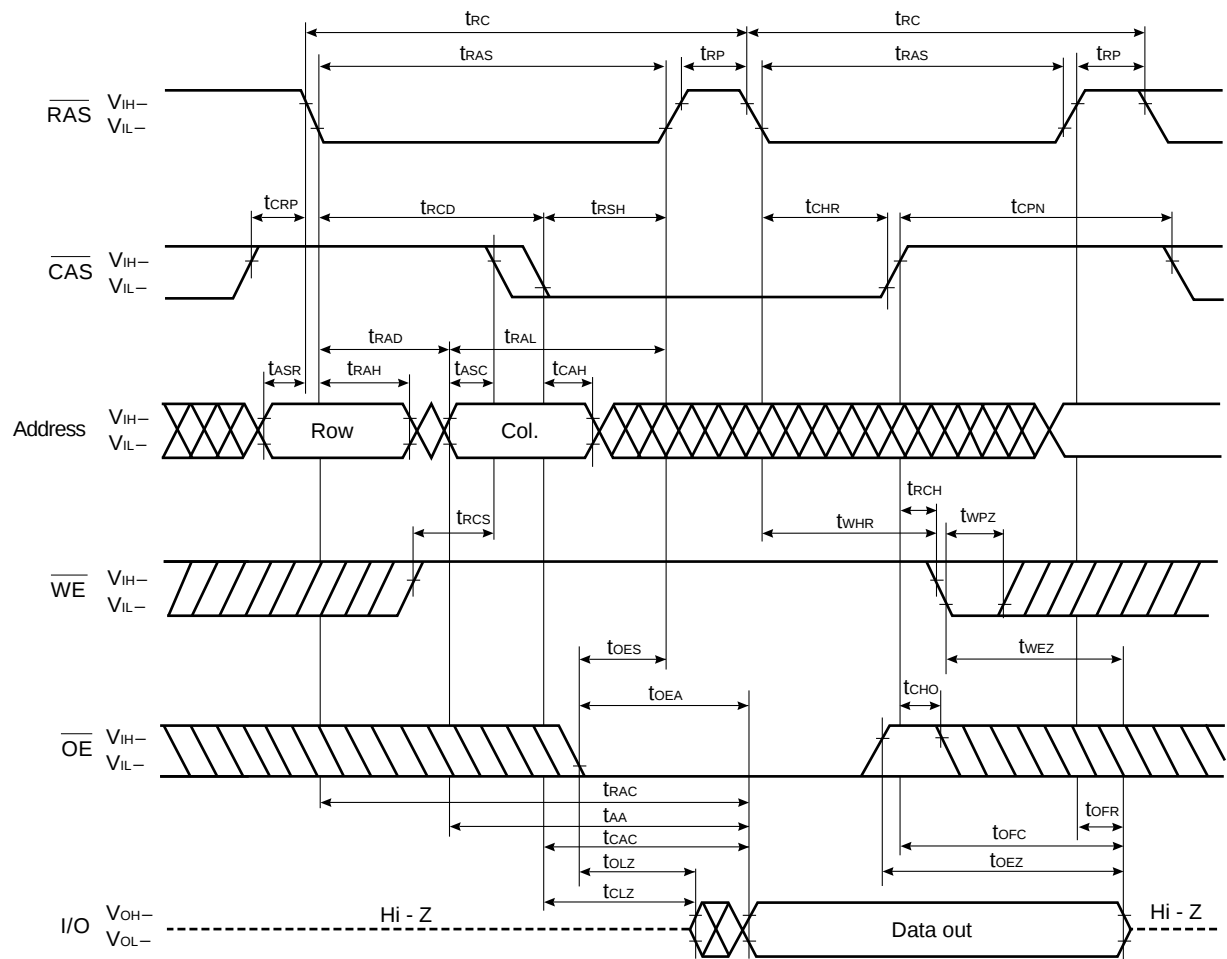
CAS Before RAS Refresh Cycle

Remark Address, $\overline{\text{OE}}$: Don't care I/O: Hi-Z

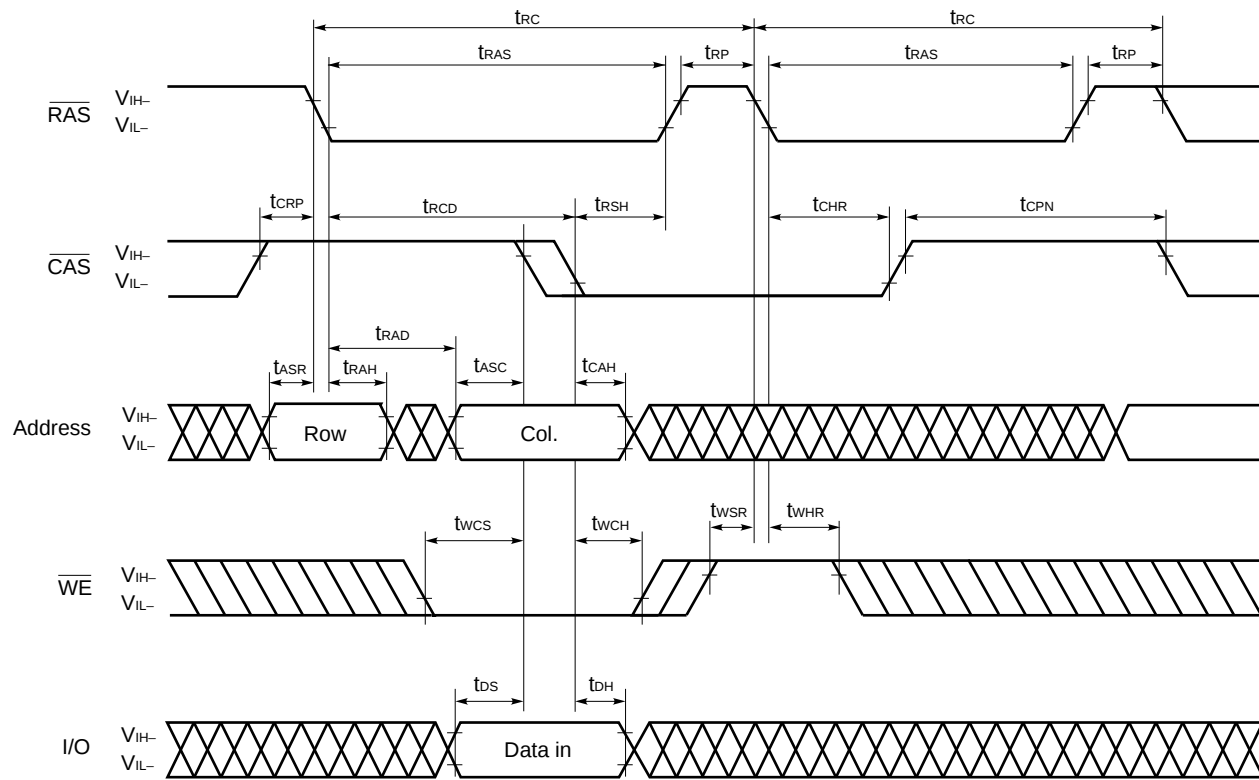
RAS Only Refresh Cycle

Remark $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)

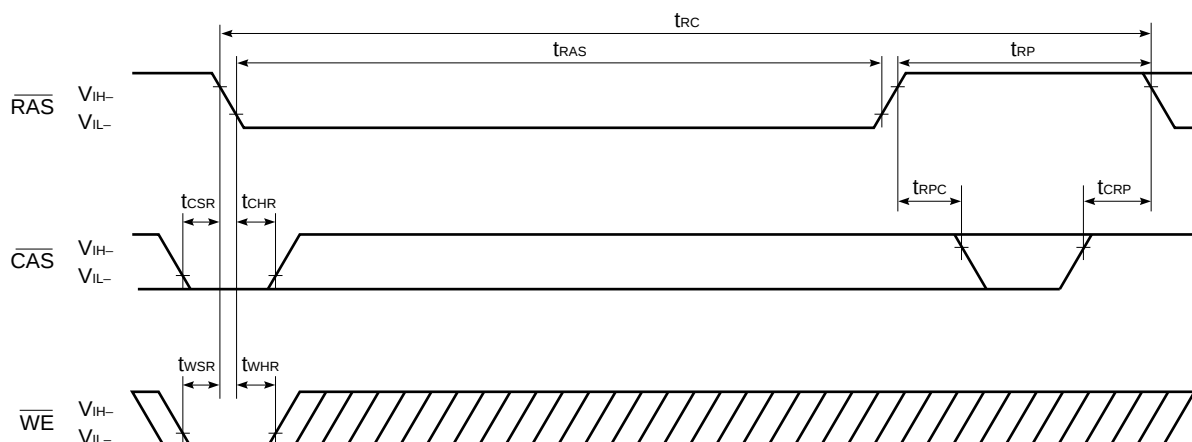


Hidden Refresh Cycle (Write)



Remark $\overline{\text{OE}}$: Don't care

Test Mode Set Cycle ($\overline{WE}$, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)



Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

Test Mode

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the $\times 16$ -bit organization during test mode. Don't care about the input levels of the $\overline{CAS}$ input A0, A1.

(1) Setting the mode

Executing the test mode cycle ($\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle) sets the test mode.

(2) Write/read operation

When either a "0" or a "1" is written to the input pin in test mode, this data is written to 16 bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell can be checked.

Output = "1": Normal write (all memory cells)

Output = "0": Abnormal write

(3) Refresh

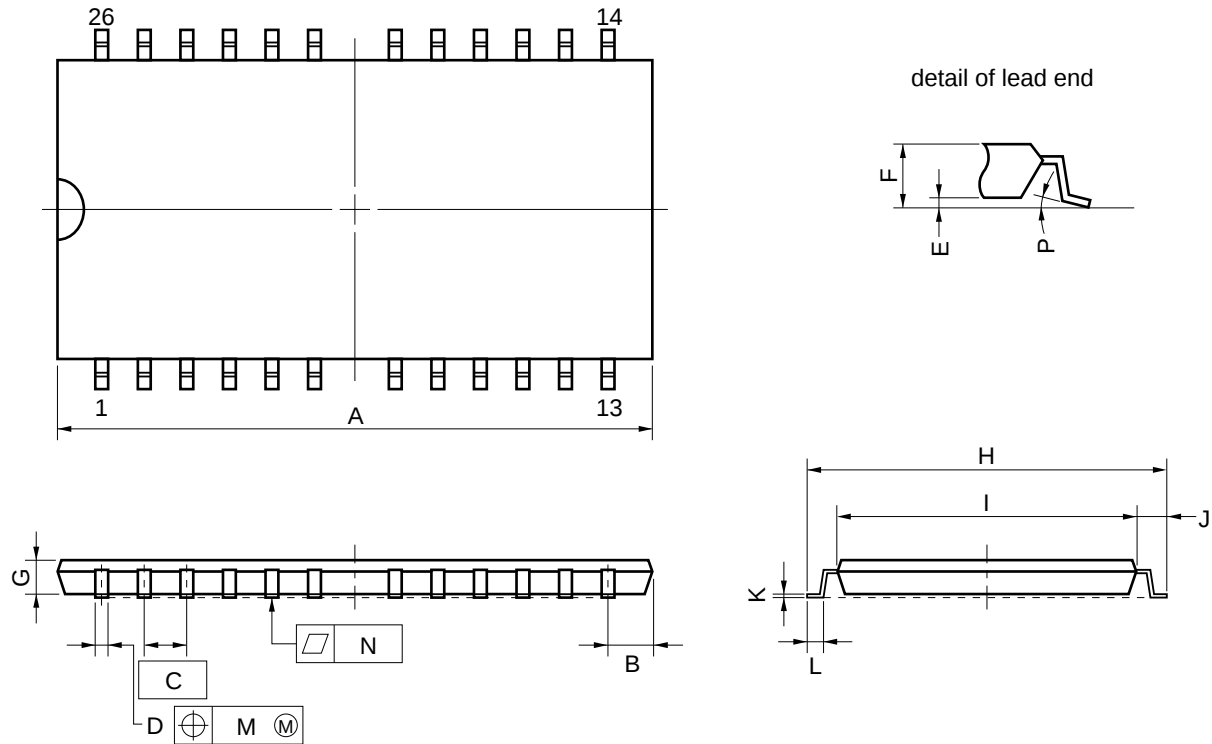
Refresh in the test mode must be performed with the $\overline{RAS}$ / $\overline{CAS}$ cycle or with the $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. The $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle use the same counter as the $\overline{CAS}$ before $\overline{RAS}$ refresh's internal counter.

(4) Mode Cancellation

The test mode is cancelled by executing one cycle of $\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

Package Drawings

26PIN PLASTIC TSOP(II) (300 mil)



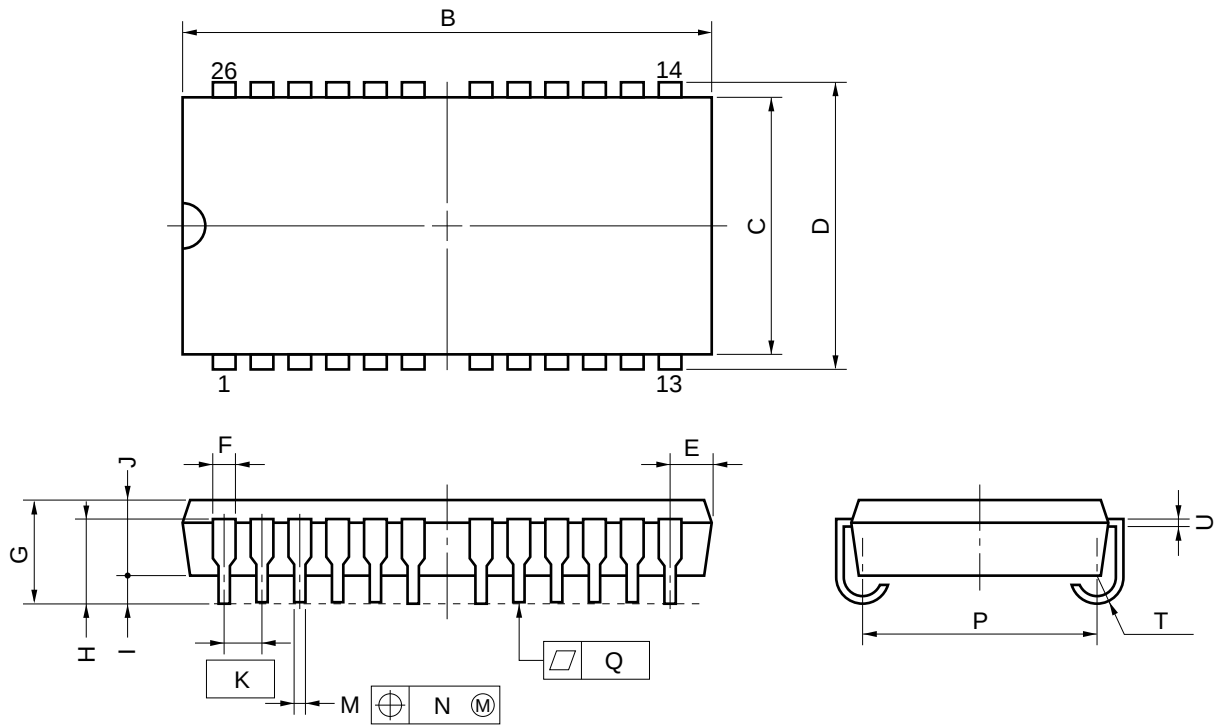
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.36 MAX.	0.684 MAX.
B	1.06 MAX.	0.042 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.42 ^{+0.08} _{-0.07}	0.017±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	9.22±0.2	0.363±0.008
I	7.62±0.1	0.300±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.145 ^{+0.025} _{-0.015}	0.006±0.001
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.21	0.009
N	0.10	0.004
P	3° ^{+7°} _{-3°}	3° ^{+7°} _{-3°}

S26G3-50-7JD1

26 PIN PLASTIC SOJ (300 mil)

**NOTE**

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	17.3 ^{+0.20} _{-0.25}	0.681 ^{+0.008} _{-0.010}
C	7.62	0.300
D	8.47±0.2	0.333 ^{+0.009} _{-0.008}
E	1.03±0.15	0.041 ^{+0.006} _{-0.007}
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	6.73±0.2	0.265±0.008
Q	0.10	0.004
T	R0.85	R0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}

S26LA-300A-1

★ Recommended Soldering Conditions

The following conditions (see tables below and next page) must be met for soldering conditions of the μPD42S17405, 4217405.

For more details, refer to our document “SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL” (C10535E).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD42S17405G3-7JD, 4217405G3-7JD: 26-pin plastic TSOP (II) (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 3 Exposure limit: 7 days ^{Note} (10 hours pre-baking is required at 125 °C afterwards)	IR35-107-3
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 3 Exposure limit :7 days ^{Note} (10 hours pre-baking is required at 125 °C afterwards)	VP15-107-3
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or lower (Per side of the package).	_____

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for “Partial heating method”.

μ PD42S17405LA, 4217405LA: 26-pin plastic SOJ (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 3 Exposure limit: 7 days ^{Note} (20 hours pre-baking is required at 125 °C afterwards)	IR35-207-3
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 3 Exposure limit: 7 days ^{Note} (20 hours pre-baking is required at 125 °C afterwards)	VP15-207-3
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or less (Per side of the package).	_____

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for “Partial heating method”.

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Corporation. NEC Corporation assumes no responsibility for any errors which may appear in this document.

NEC Corporation does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from use of a device described herein or any other liability arising from use of such device. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Corporation or others.

While NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customers must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.

NEC devices are classified into the following three quality grades:

"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

Anti-radioactive design is not implemented in this product.