TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

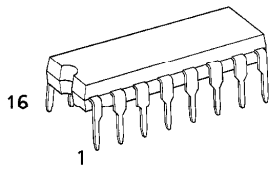
TC4521BP

TC4521BP 24 – STAGE FREQUENCY DIVIDER

TC4521BP is frequency divider consisting of 24 stages of flip-flop. The input section is equipped with an inverter to enable to use either RC oscillator circuit or crystal oscillator circuit and to accept pulse from external clock source.

Each flip-flop is inverted by the falling edge of the output of previous stage flip-flop and this can count up to the maximum of $2^{24}=16,777,216$.

Since six outputs, 2^{18}, 2^{19}, 2^{20}, 2^{21}, 2^{22}, and 2^{23} are available besides of 2^{24}, adjustment of frequency divided output can be achieved.

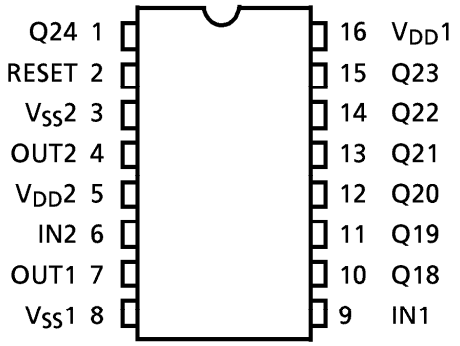


P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)

MAXIMUM RATINGS

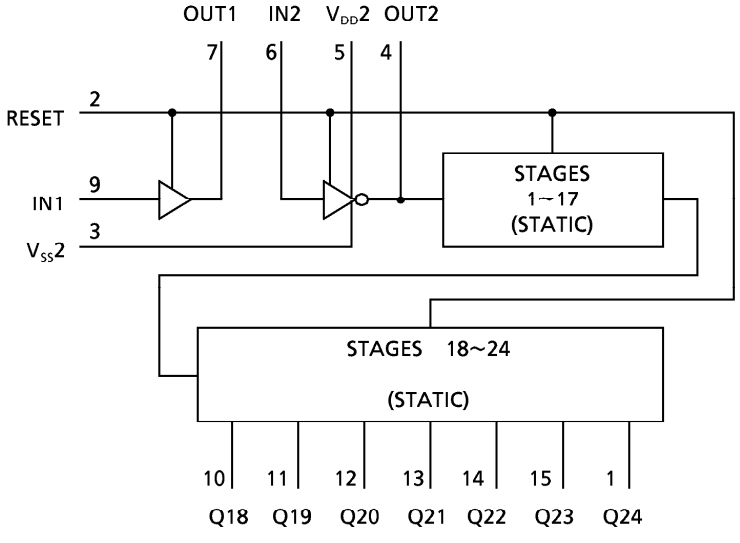
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	$V_{DD}1$	$V_{SS}1-0.5\sim V_{SS}1+20$	V
	$V_{DD}2$	$V_{SS}1-0.5\sim V_{DD}1+0.5$	
Input Voltage	V_{IN}	$V_{SS}1-0.5\sim V_{DD}1+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}1-0.5\sim V_{DD}1+0.5$	
DC Input Current	I_{IN}	± 10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_{opr}	−40~85	°C
Storage Temperature Range	T_{stg}	−65~150	°C

PIN ASSIGNMENT



(TOP VIEW)

BLOCK DIAGRAM

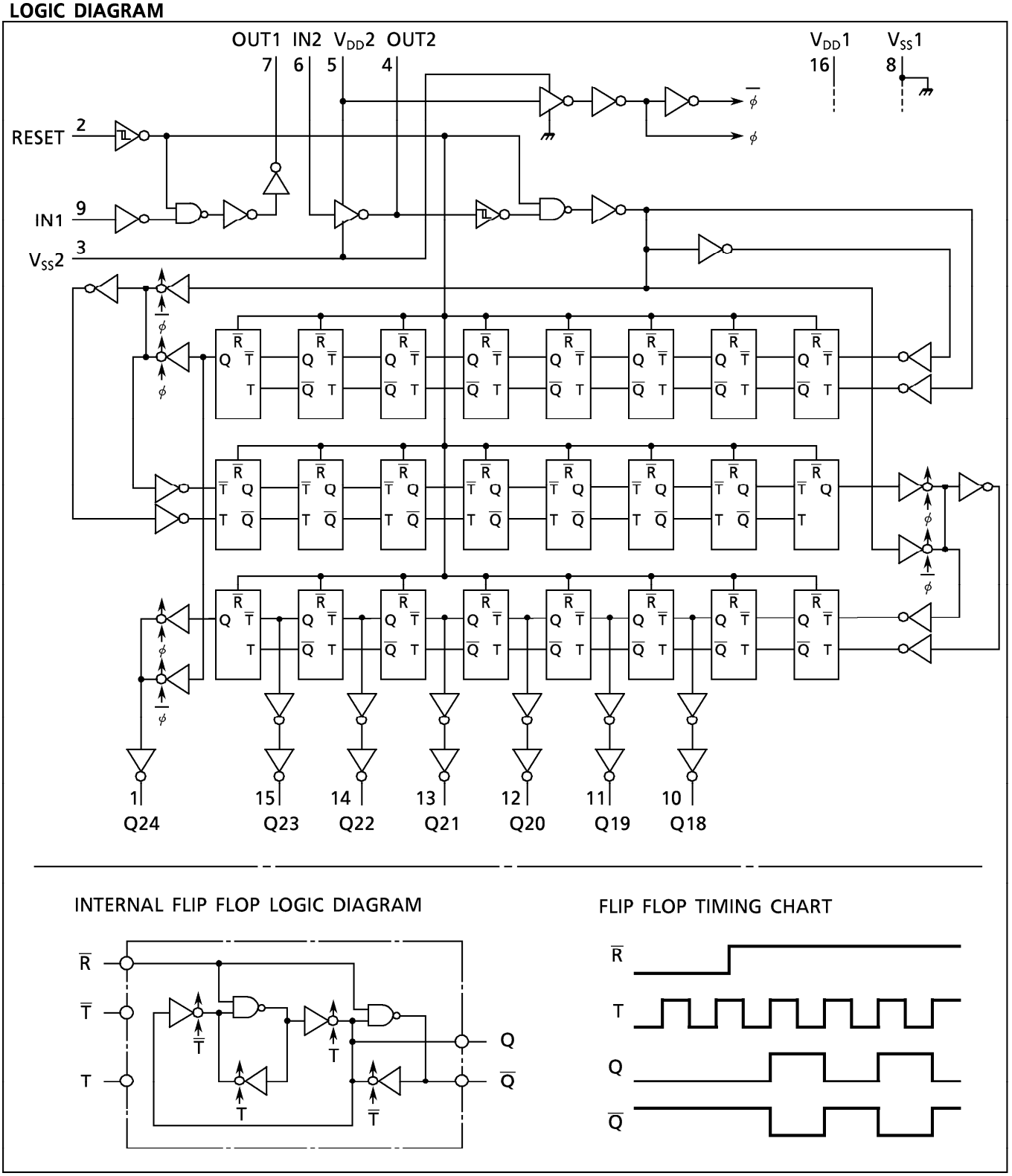


COUNT CAPACITY

OUTPUT	COUNT CAPACITY
Q18	2^{18} = 262,144
Q19	2^{19} = 524,288
Q20	2^{20} = 1,048,576
Q21	2^{21} = 2,097,152
Q22	2^{22} = 4,194,304
Q23	2^{23} = 8,388,608
Q24	2^{24} = 16,777,216

961001EBA2

LOGIC DIAGRAM



INTERNAL FLIP FLOP LOGIC DIAGRAM

FLIP FLOP TIMING CHART

961001EBA2'

RECOMMENDED OPERATING CONDITIONS ($V_{SS}1 = V_{SS}2 = 0V$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	$V_{DD}1, V_{DD}2$		3	—	18	V
Input Voltage	V_{IN}		0	—	$V_{DD}1$	V

STATIC ELECTRICAL CHARACTERISTICS ($V_{SS}1 = V_{SS}2 = 0V$, $V_{DD}1 = V_{DD}2$)

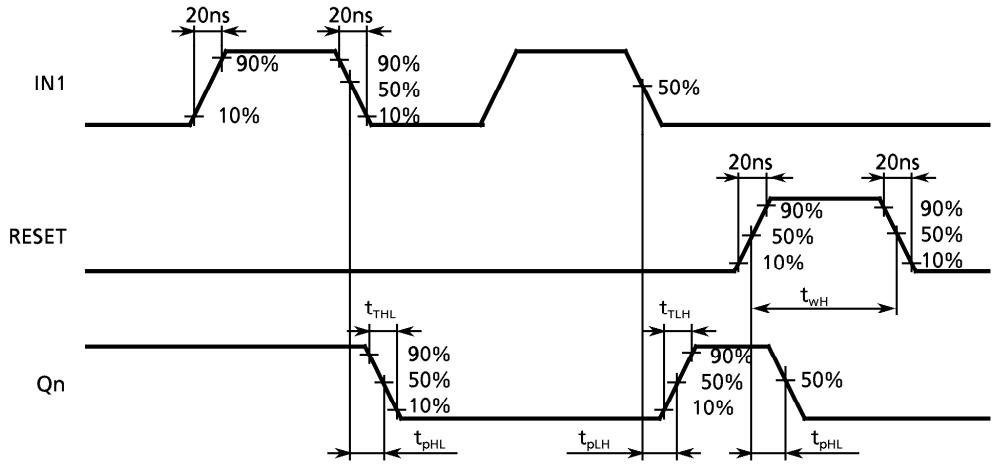
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	−40°C MIN.	−40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.00 10.00 15.00	— — —	4.95 9.95 14.95	— — —	V
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\| < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5 10 15	— — —	0.05 0.05 0.05	— — —	0.00 0.00 0.00	0.05 0.05 0.05	— — —	0.05 0.05 0.05	V
Output High Current	I_{OH}	$V_{OH} = 4.6V$ $V_{OH} = 2.5V$ $V_{OH} = 9.5V$ $V_{OH} = 13.5V$ $V_{IN} = V_{SS}, V_{DD}$	5 5 10 15	−0.61 −2.5 −1.5 −4.0	— — — —	−0.51 −2.1 −1.3 −3.4	−1.0 −4.0 −2.2 −9.0	— — — —	−0.42 −1.7 −1.1 −2.8	— — — —	mA
Output Low Current	I_{OL}	$V_{OL} = 0.4V$ $V_{OL} = 0.5V$ $V_{OL} = 1.5V$ $V_{IN} = V_{SS}, V_{DD}$	5 10 15	0.61 1.5 4.0	— — —	0.51 1.3 3.4	1.2 3.2 12.0	— — —	0.42 1.1 2.8	— — —	mA
Input High Voltage	V_{IH}	$V_{OUT} = 0.5V, 4.5V$ $V_{OUT} = 1.0V, 9.0V$ $V_{OUT} = 1.5V, 13.5V$ $\|I_{OUT}\| < 1\mu A$	5 10 15	3.5 7.0 11.0	— — —	3.5 7.0 11.0	2.75 5.5 8.25	— — —	3.5 7.0 11.0	— — —	V
Input Low Voltage	V_{IL}	$V_{OUT} = 0.5V, 4.5V$ $V_{OUT} = 1.0V, 9.0V$ $V_{OUT} = 1.5V, 13.5V$ $\|I_{OUT}\| < 1\mu A$	5 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.5 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	V
Input Current "H" Level	I_{IH}	$V_{IH} = 18V$	18	—	0.1	—	10^{-5}	0.1	—	1.0	μA
Input Current "L" Level	I_{IL}	$V_{IL} = 0V$	18	—	−0.1	—	-10^{-5}	−0.1	—	−1.0	μA
Quiescent Supply Current	I_{DD}	$V_{IN} = V_{SS}, V_{DD}$ *	5 10 15	— — —	5 10 20	— — —	0.005 0.010 0.015	5 10 20	— — —	150 300 600	μA

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta = 25°C, $V_{SS}1 = V_{SS}2 = 0V$, $V_{DD}1 = V_{DD}2$, $C_L = 50pF$)

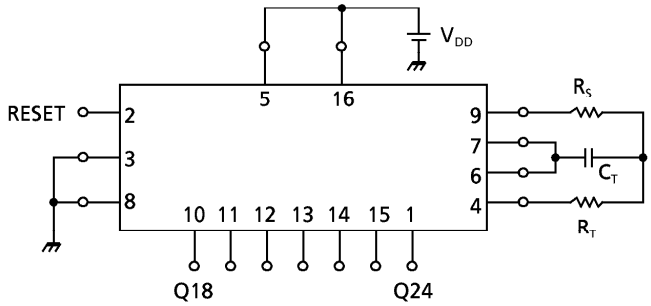
CHARACTERISTIC	SYMBOL	TEST CONDITION V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}	5	—	70	200	ns
		10	—	35	100	
		15	—	30	80	
Output Transition Time (High to Low)	t_{THL}	5	—	70	200	
		10	—	35	100	
		15	—	30	80	
Propagation Delay Time (IN2 - Q18)	t_{pLH} t_{pHL}	5	—	1.1	9.0	μs
		10	—	0.5	3.5	
		15	—	0.3	2.7	
Propagation Delay Time (IN2 - Q24)	t_{pLH} t_{pHL}	5	—	1.4	12	
		10	—	0.6	4.5	
		15	—	0.4	3.5	
Propagation Delay Time (RESET - Qn)	t_{pHL}	5	—	220	2600	ns
		10	—	100	1000	
		15	—	70	750	
Max. Clock Frequency	f_{CL}	5	3	9.5	—	MHz
		10	6	17.5	—	
		15	8	23.5	—	
Max. Clock Input Rise Time Max. Clock Input Fall Time	t_{rCL} t_{fCL}	5	No Limit			μs
		10				
		15				
Min. Clock Pulse Width	t_W	5	—	55	385	ns
		10	—	25	150	
		15	—	16	120	
Min. Pulse Width (RESET)	t_{WH}	5	—	60	385	
		10	—	26	150	
		15	—	20	120	
Input Capacitance	C_{IN}		—	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS



APPLICATION CIRCUIT

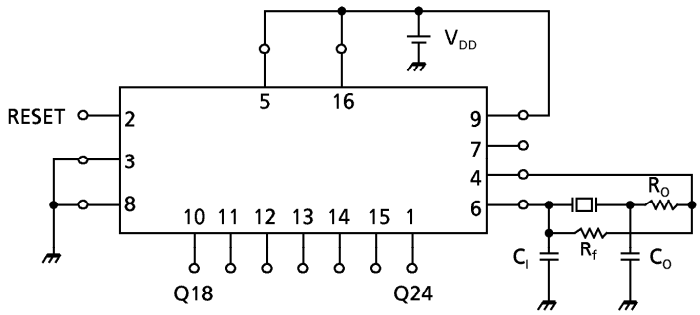
* When CR oscillation is used as time reference



$$R_S \geqq 2R_T$$

$$f_{OSC} \simeq \frac{1}{2.2R_T\ C_T}$$

* When crystal oscillation circuit is used as the time reference

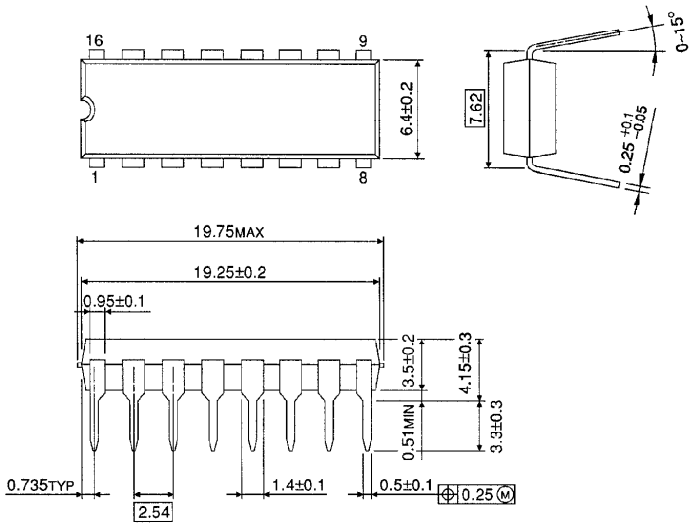


Typical data

X'tal (Hz)	C_I, C_O (pF)	R_O (Ω)
32.768k	23	500k
100k	60	100k
1M	45~50	100
4.194304M	12~15	0

$R_f = 10M\Omega$

DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A) Unit in mm



Weight : 1.00g (Typ.)