

Power Switching Regulator

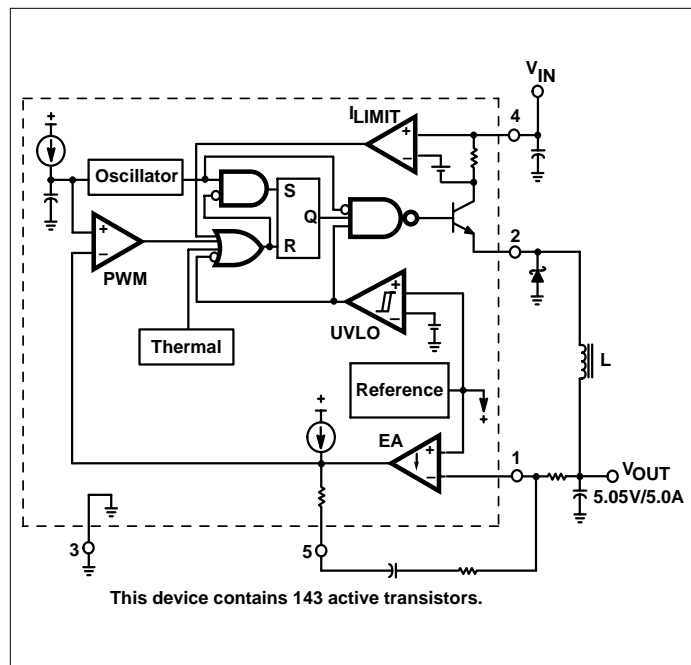
FEATURES

- Output Switch Current in Excess of 5.0A
- Fixed Frequency Oscillator (72kHz) with On-Chip Timing
- Provides 5.05V Output without External Resistor Divider
- Precision 2% Reference
- 0% to 95% Output Duty Cycle
- Cycle-by-Cycle Current Limiting
- Undervoltage Lockout with Hysteresis
- Internal Thermal Shutdown
- Operation from 7.5V to 40V
- Standby Mode Reduces Power Supply Current to 36 μ A
- Economical 5-Pin TO-220 Package with Two Optional Leadforms
- Also Available in 5-Pin DDPK Package

APPLICATIONS

- Automotive
- Computing
- Industrial Controllers
- Consumer Electronics
- Set-Top Boxes
- Network Boxes

FUNCTIONAL BLOCK DIAGRAM



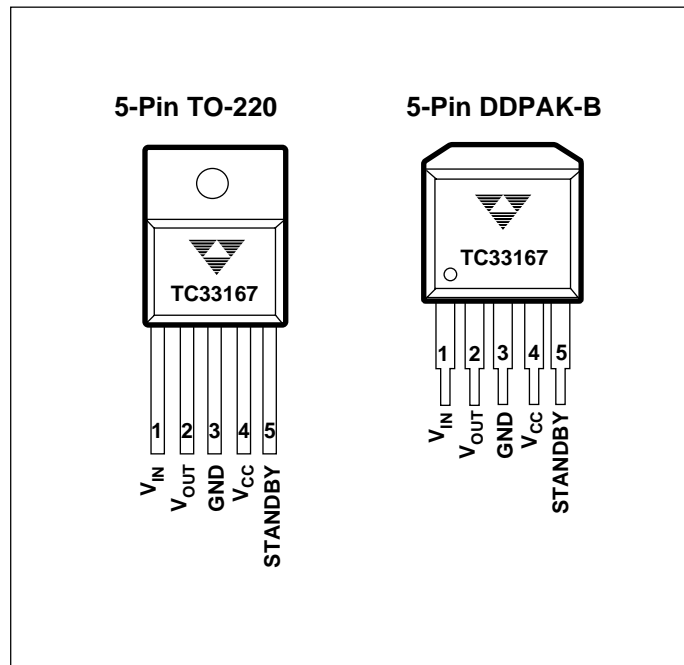
GENERAL DESCRIPTION

The TC33167 is a high performance fixed frequency power switching regulator that contains the primary functions required for DC/DC converters. This regulator is specifically designed to be incorporated in step-down and voltage-inverting configurations with a minimum number of external components and can also be used cost effectively in step-up applications. This device consists of an internal temperature compensated reference, fixed frequency oscillator with on-chip timing components, latching pulse width modulator for single pulse metering, high gain error amplifier, and a high current output switch. Protective features consist of cycle-by-cycle current limiting, undervoltage lockout, and thermal shutdown. Also included is a low power standby mode that reduces power supply current to 36 μ A.

ORDERING INFORMATION

Part Number	Package	Temperature Range
TC33167EAT	5-Pin TO-220	-40° to +85°C
TC33167ERT	5-Pin DDPK-B	-40° to +85°C

PIN CONFIGURATIONS



TC33167

ABSOLUTE MAXIMUM RATINGS*

Power Supply Voltage $V_{CC} = 40V$
 Switch Output Voltage $V_{OUT(SWITCH)} = -2.0$ to $+V_{IN}$
 Voltage Feedback and
 Compensation Input $V_{FB}, V_{COMP} = -1.0$ to $+7.0$
 Power Dissipation
 5-Pin TO-220 Package ($T_A = +25^\circ C$) Internally Limited
 Thermal Resistance (Junction to Ambient) $\theta_{JA} = 65^\circ C/W$
 Thermal Resistance(Junction to Case) .. $\theta_{JC} = 5.0^\circ C/W$

5-Pin DDPak-B Package ($T_A = +25^\circ C$) Internally Limited
 Thermal Resistance (Junction to Ambient) ... $\theta_{JA} = 70^\circ C/W$
 Thermal Resistance(Junction to Case) .. $\theta_{JC} = 5.0^\circ C/W$
 Operating Junction Temperature, T_J $+150^\circ C$
 Operating Ambient Temperature Range (Note 3) -40 to $+85^\circ C$
 Storage Temperature Range $T_{STG} = -65$ to $+150^\circ C$

*This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operation section of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods of time may affect device reliability.

ELECTRICAL CHARACTERISTICS: $V_{CC} = 5.0V$, $T_A = T_{LOW}$ to T_{HIGH} [Note 3], unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Oscillator						
f_{OSC}	Frequency ($V_{CC} = 7.5V$ to $40V$),	$T_A = +25^\circ C$ $T_A = T_{LOW}$ to T_{HIGH}	65 62	72 —	79 81	kHz
Error Amplifier						
$V_{FB(TH)}$	Voltage Feedback Input Threshold	$T_A = +25^\circ C$ $T_A = T_{LOW}$ to T_{HIGH}	4.95 4.85	5.05 —	5.15 5.20	V
Reg_{line}	Line Regulation	$V_{CC} = 7.5V$ to $40V$, $T_A = +25^\circ C$	—	0.03	0.078	%V
I_{IB}	Input Bias Current	$V_{FB} = V_{FB(TH)} + 0.15V$	—	0.15	1.0	μA
PSSR	Power Supply Rejection Ratio	$V_{CC} = 10V$ to $20V$, $f = 120Hz$	60	80	—	dB
V_{OH}	Output Voltage Swing	High State ($I_{SOURCE} = 75\mu A$, $V_{FB} = 4.5V$	4.2	4.9	—	V
V_{OL}		Low State $I_{SINK} = 0.4mA$, $V_{FB} = 5.5V$	—	1.6	1.9	
PWM Comparator						
$DC_{(MAX)}$	Duty Cycle ($V_{CC} = 20V$)	Maximum ($V_{FB} = 0V$)	92	95	100	%
$DC_{(MIN)}$		Minimum ($V_{COMP} = 1.9V$)	0	0	0	
Switch Output						
V_{SAT}	Output Voltage Source Saturation	$V_{CC} = 7.5V$, $I_{SOURCE} = 5.0A$	—	$V_{CC} - 1.5$	$V_{CC} - 1.8$	V
$I_{SW(OFF)}$	Off-State Leakage	$V_{CC} = 40V$, Pin 2 = GND	—	0	100	μA
$I_{PKSWITCH}$	Current Limit Threshold	$V_{CC} = 7.5V$	5.5	6.5	8.0	A
t_r	Switching Times ($V_{CC} = 40V$, $I_{PK} = 5.0A$, $L = 225\mu H$, $T_A = +25^\circ C$)	Output Voltage Rise Time	—	100	200	nsec
t_f		Output Voltage Fall Time	—	50	100	
Undervoltage Lockout						
$V_{TH(UVLO)}$	Startup Threshold	V_{CC} Increasing, $T_A = +25^\circ C$	5.5	5.9	6.3	V
$V_{H(UVLO)}$	Hysteresis	V_{CC} Decreasing, $T_A = +25^\circ C$	0.6	0.9	1.2	V
Total Device						
I_{CC}	Power Supply Current ($T_A = +25^\circ C$)	Standby ($V_{CC} = 12V$, $V_{COMP} < 0.15V$) Operating ($V_{CC} = 40V$, Pin 1 = GND for maximum duty cycle)	— —	36 40	100 60	μA mA

NOTES: 1. Maximum package power dissipation limits must be observed to prevent thermal shutdown activation.
 2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
 3. $T_{LOW} = -40^\circ C$, $T_{HIGH} = +85^\circ C$

INTRODUCTION

The TC33167 is a monolithic power switching regulator that is optimized for DC-to-DC converter applications. This device operates as a fixed frequency, voltage mode regulator containing all the active functions required to directly implement step-down and voltage-inverting converters with a minimum number of external components. It can also be used cost effectively in step-up converter applications. Potential markets include automotive, computer, industrial, and cost sensitive consumer products. A description of each section of the device is given below with the representative block diagram shown in Figure 1.

Oscillator

The oscillator frequency is internally programmed to 72 kHz by capacitor C_T and a trimmed current source. The charge to discharge ratio is controlled to yield a 95% maximum duty cycle at the Switch Output. During the discharge of C_T , the oscillator generates an internal blanking pulse that holds the inverting input of the AND gate high, disabling the output switch transistor. The nominal oscillator peak and valley thresholds are 4.1V and 2.3V respectively.

Pulse Width Modulator

The Pulse Width Modulator consists of a comparator with the oscillator ramp voltage applied to the noninverting input, while the error amplifier output is applied into the inverting input. Output switch conduction is initiated when C_T is discharged to the oscillator valley voltage. As C_T charges to a voltage that exceeds the error amplifier output, the latch resets, terminating output transistor conduction for the duration of the oscillator ramp-up period. This PWM/Latch combination prevents multiple output pulses during a given oscillator clock cycle. Figures 2 and 22 illustrate the switch output duty cycle versus the compensation voltage.

Current Sense

The TC33167 utilizes cycle-by-cycle current limiting as a means of protecting the output switch transistor from overstress. Each on cycle is treated as a separate situation. Current limiting is implemented by monitoring the output switch transistor current buildup during conduction, and upon sensing an overcurrent condition, immediately turning off the switch for the duration of the oscillator ramp-up period.

The collector current is converted to a voltage by an internal trimmed resistor and compared against a reference by the Current Sense comparator. When the current limit threshold is reached, the comparator resets the PWM latch.

The current limit threshold is typically set at 6.5 A.

Figure 25 illustrates switch output current limit threshold versus temperature.

Error Amplifier and Reference

A high gain Error Amplifier is provided with access to the inverting input and output. This amplifier features a typical DC voltage gain of 80dB, and a unity gain bandwidth of 600kHz with 70 degrees of phase margin (Figure 19). The noninverting input is biased to the internal 5.05V reference, and is not pinned out. The reference has an accuracy of $\pm 2.0\%$ at room temperature. To provide 5.0V at the load, the reference is programmed 50mV above 5.0V to compensate for a 1.0% voltage drop in the cable and connector from the converter output. If the converter design requires an output voltage greater than 5.05V, resistor R_1 must be added to form a divider network at the feedback input as shown in Figures 1 and 6. The equation for determining the output voltage with the divider network is:

$$V_{OUT} = 5.05 \left(\frac{R_2}{R_1} \right) + 1$$

External loop compensation is required for converter stability. A simple low-pass filter is formed by connecting a resistor (R_2) from the regulated output to the inverting input, and a series resistor-capacitor (R_F , C_F) between Pins 1 and 5. The compensation network component values shown in each of the applications circuits were selected to provide stability over the tested operating conditions. The step-down converter (Figure 6) is the easiest to compensate for stability. The step-up (Figure 8) and voltage-inverting (Figure 10) configurations operate as continuous conduction flyback converters, and are more difficult to compensate. The simplest way to optimize the compensation network is to observe the response of the output voltage to a step load change, while adjusting R_F and C_F for critical damping. The final circuit should be verified for stability under four boundary conditions. These conditions are minimum and maximum input voltages, with minimum and maximum loads.

By clamping the voltage on the error amplifier output (Pin 5) to less than 150mV, the internal circuitry will be placed into a low power standby mode, reducing the power supply current to 36 μ A with a 12V supply voltage. Figure 26 illustrates the standby supply current versus supply voltage.

The Error Amplifier output has a 100 μ A current sourcepull-up that can be used to implement soft-start. Figure 5 shows the current source charging capacitor C_{SS} through a series diode. The diode disconnects C_{SS} from the feedback loop when the 1.0M resistor charges it above the operating range of Pin 5.

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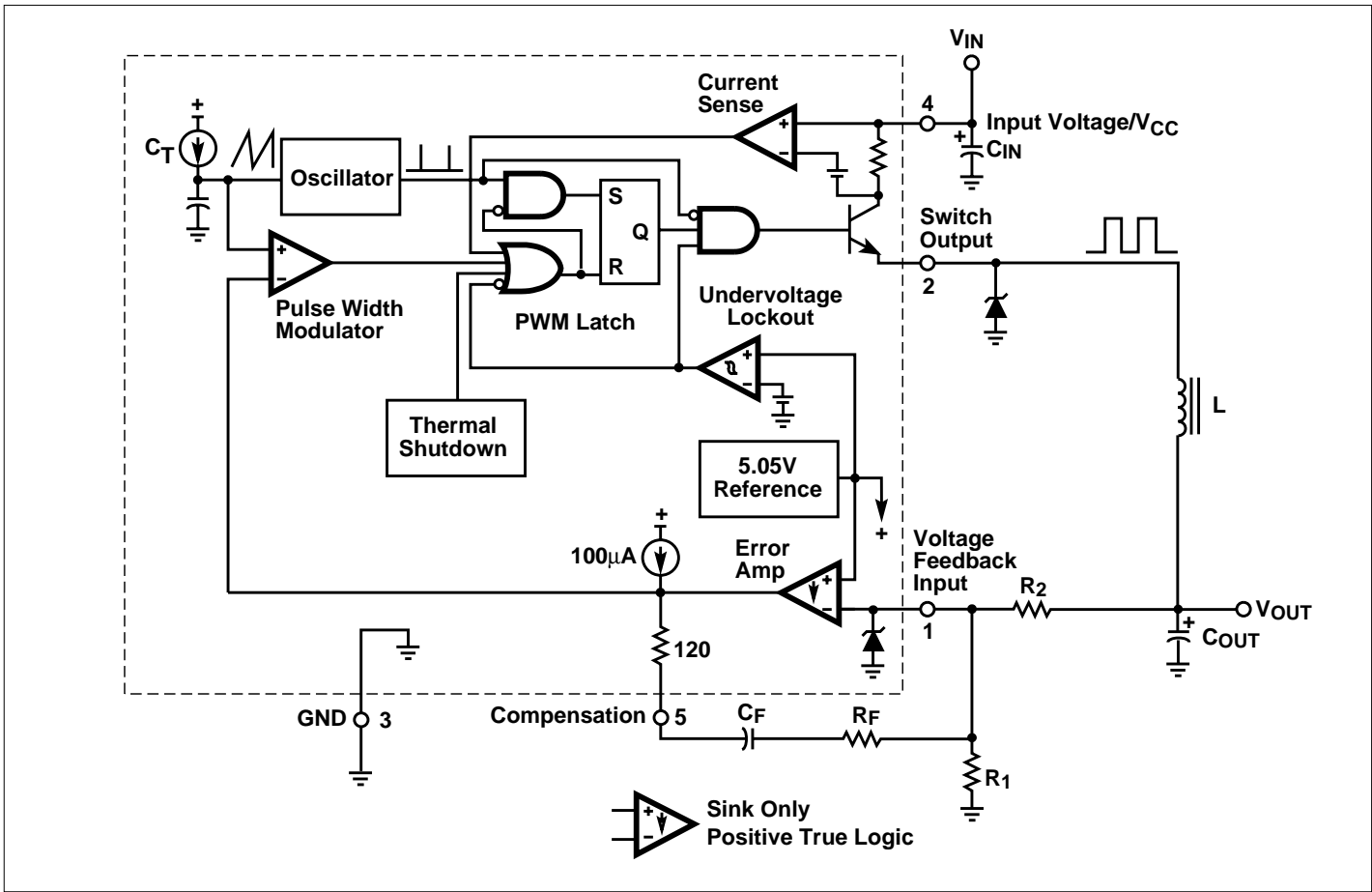


Figure 1. Representative Block Diagram

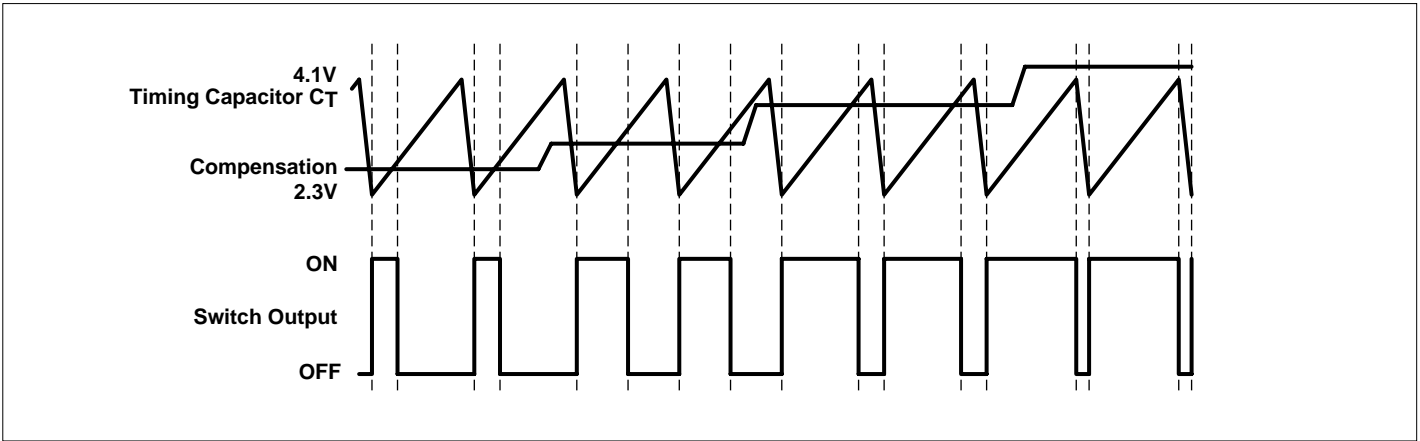


Figure 2. Timing Diagram

Switch Output

The output transistor is designed to switch a maximum of 40V, with a minimum peak collector current of 5.5 A. When configured for step-down or voltage-inverting applications, as in Figures 6 and 10, the inductor will forward bias the output rectifier when the switch turns off. Rectifiers with a high forward voltage drop or long turn on delay time should not be used. If the emitter is allowed to go sufficiently negative, collector current will flow, causing additional device heating and reduced conversion efficiency. Figure 24 shows that by clamping the emitter to 0.5 V, the collector current will be in the range of 100μA over temperature. A 1N5825 or equivalent Schottky barrier rectifier is recommended to fulfill these requirements.

Undervoltage Lockout

An Undervoltage Lockout comparator has been incorporated to guarantee that the integrated circuit is fully functional before the output stage is enabled. The internal reference voltage is monitored by the comparator which enables the output stage when V_{CC} exceeds 5.9V. To prevent erratic output switching as the threshold is crossed, 0.9V of hysteresis is provided.

Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C the latch is forced into a 'reset' state, disabling the output switch. This feature is provided to prevent catastrophic failures from accidental device overheating. **It is not intended to be used as a substitute for proper heatsinking.** The TC33167 is contained in a 5-Pin TO-220 type package. The tab of the package is common with the center pins (Pin 3) and is normally connected to ground.

DESIGN CONSIDERATIONS

Do not attempt to construct a converter on wire-wrap or plug-in prototype boards. Special care should be taken to separate ground paths from signal currents and ground paths from load currents. All high current loops should be kept as short as possible using heavy copper runs to minimize ringing and radiated EMI. For best operation, a tight component layout is recommended. Capacitors C_{IN} , C_{OUT} , and all feedback components should be placed as close to the IC as physically possible. It is also imperative that the Schottky diode connected to the Switch Output be located as close to the IC as possible.

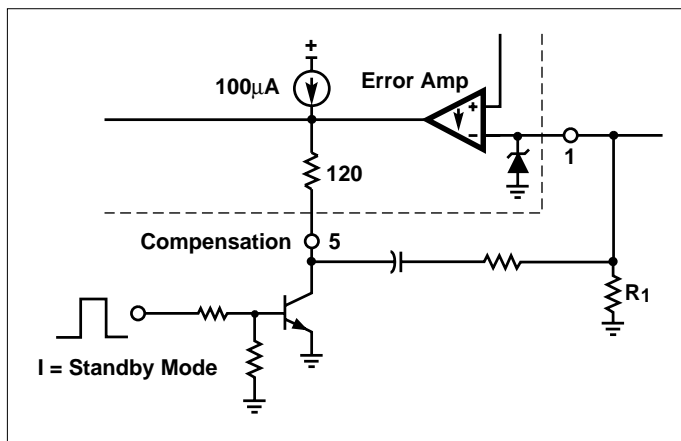


Figure 3. Low Power Standby Circuit

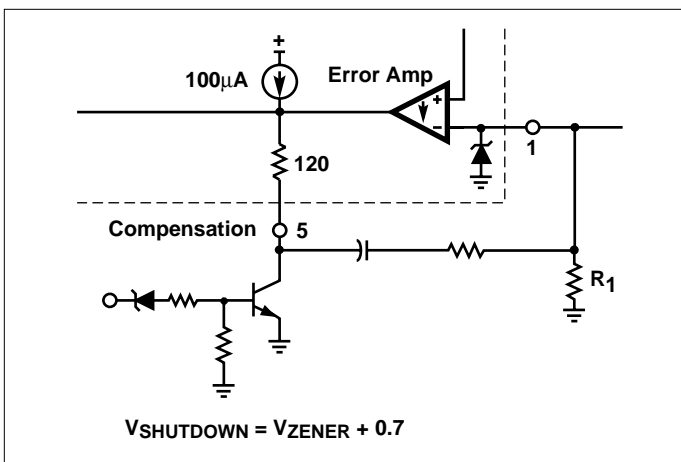


Figure 4. Over Voltage Shutdown Circuit

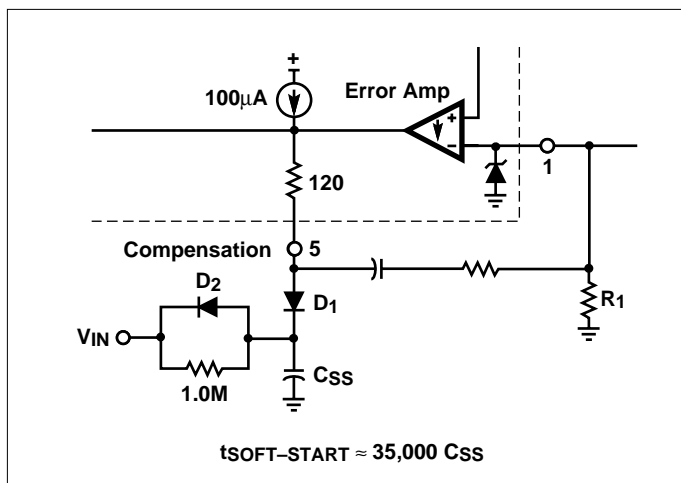
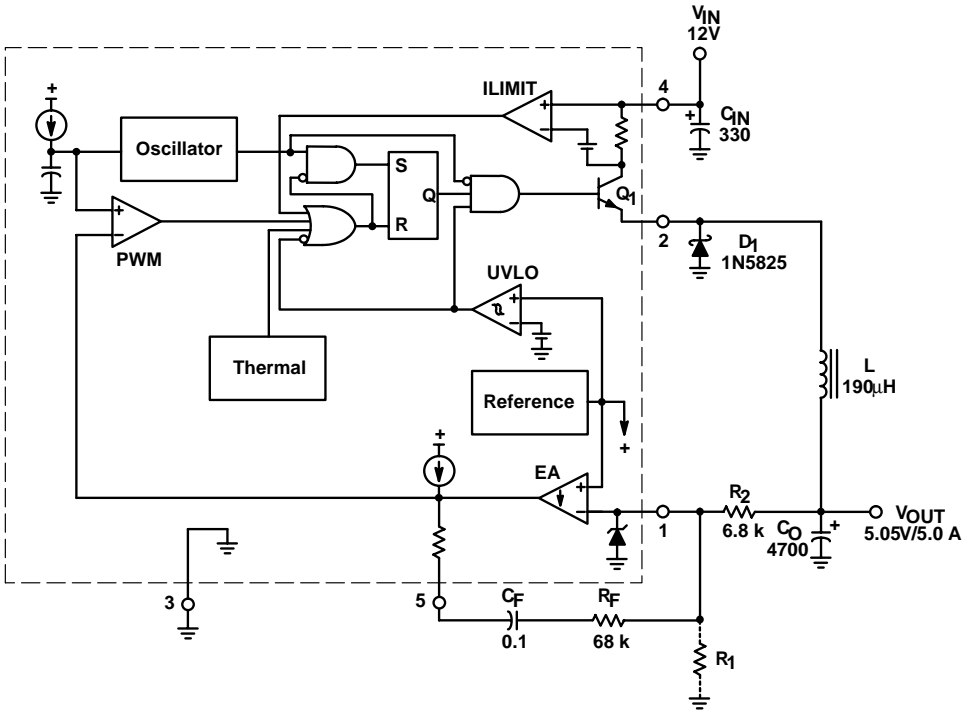


Figure 5. Soft-Start Circuit

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Test	Conditions	Results
Line Regulation	$V_{IN} = 10V \text{ to } 36V, I_{OUT} = 5.0A$	$4.0mV = \pm 0.039\%$
Load Regulation	$V_{IN} = 12V, I_{OUT} = 0.25A \text{ to } 5.0A$	$1.0mV = \pm 0.01\%$
Output Ripple	$V_{IN} = 12V, I_{OUT} = 5.0A$	$20mV_{pp}$
Short Circuit Current	$V_{IN} = 12V, R_L = 0.1\Omega$	$6.5A$
Efficiency	$V_{IN} = 12V, I_{OUT} = 5.0A$ $V_{IN} = 24V, I_{OUT} = 5.0A$	78.9% 82.6%

L = Coilcraft M1496-A or General Magnetics Technology GMT-0223, 42 turns if #16 AWG on Magnetics Inc. 58350-A2 core.
Heatsink = Aavid Engineering Inc. 5903B, or 5930B.

The Step-Down Converter application is shown in Figure above. The output switch transistor Q1 interrupts the input voltage, generating squarewave at the LC_O filter input. The filter averages the squarewaves, producing a DC output voltage that can be set to any level between V_{IN} and V_{REF} by controlling the percent conduction time of Q1 to that of the total oscillator cycle time. If the converter design requires an output voltage greater than 5.05V, resistor R₁ must be added to form a divider network at the feedback input.

Figure 6. Step-Down Converter

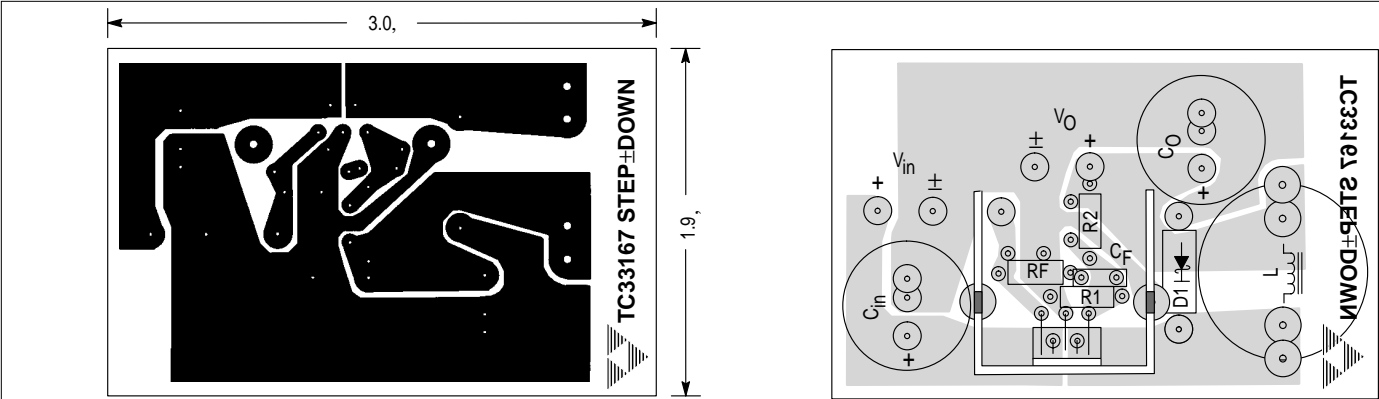


Figure 7. Step-Down Converter Printed Circuit Board and Component Layout

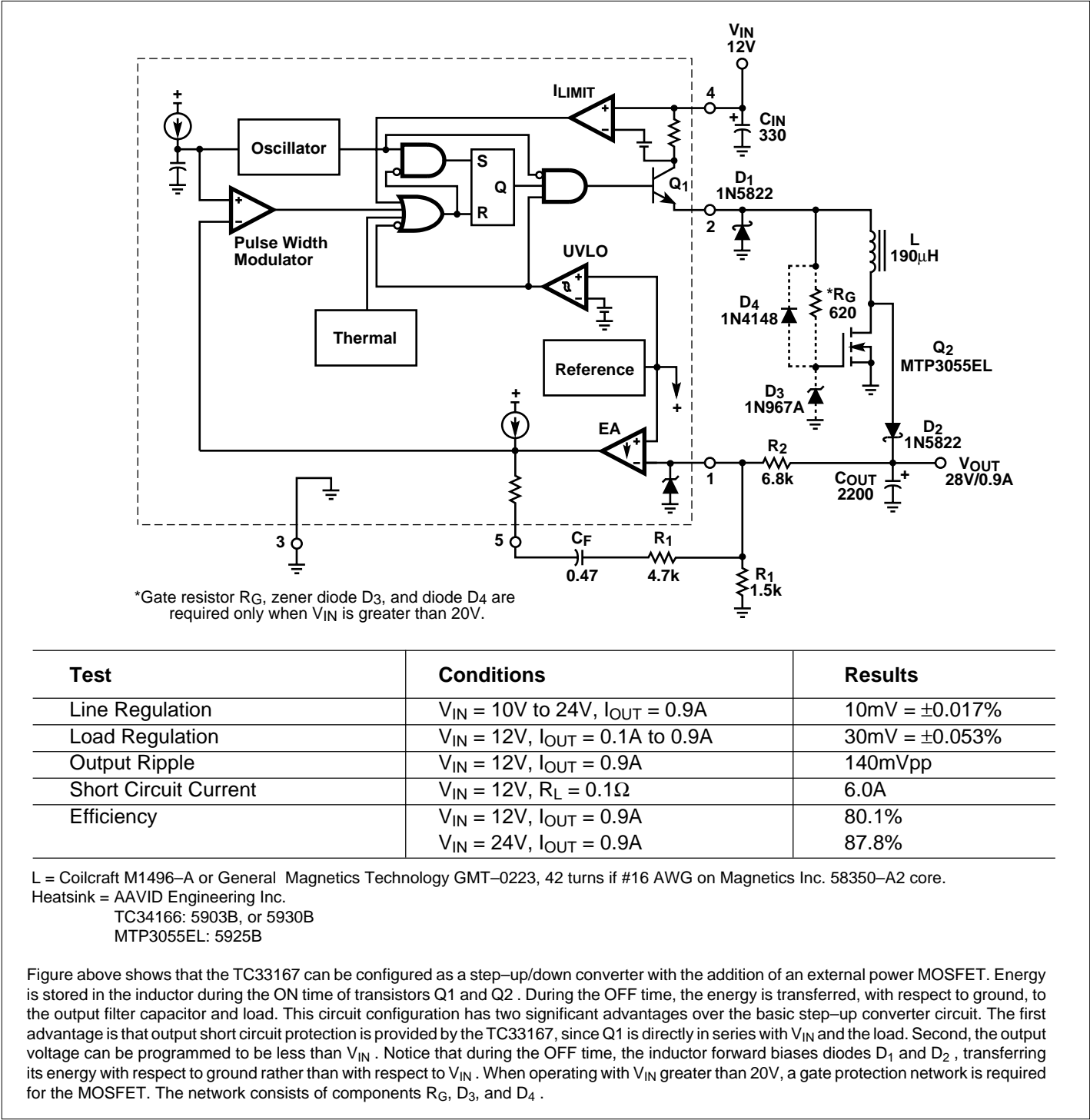


Figure 8. Step-Up / Down Converter

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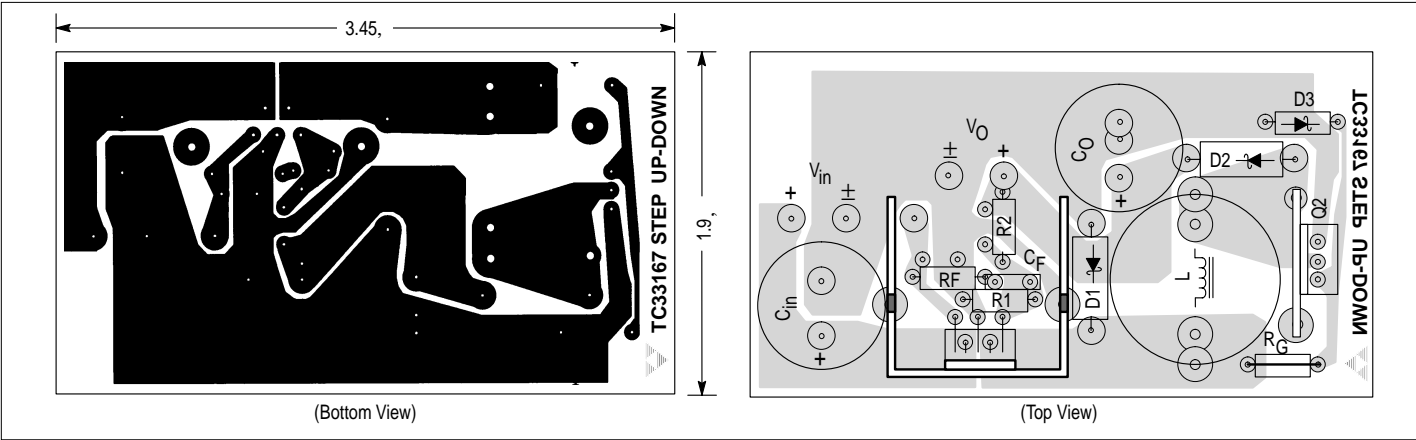


Figure 9. Step-Up/Down Converter Printed Circuit Board and Component Layout

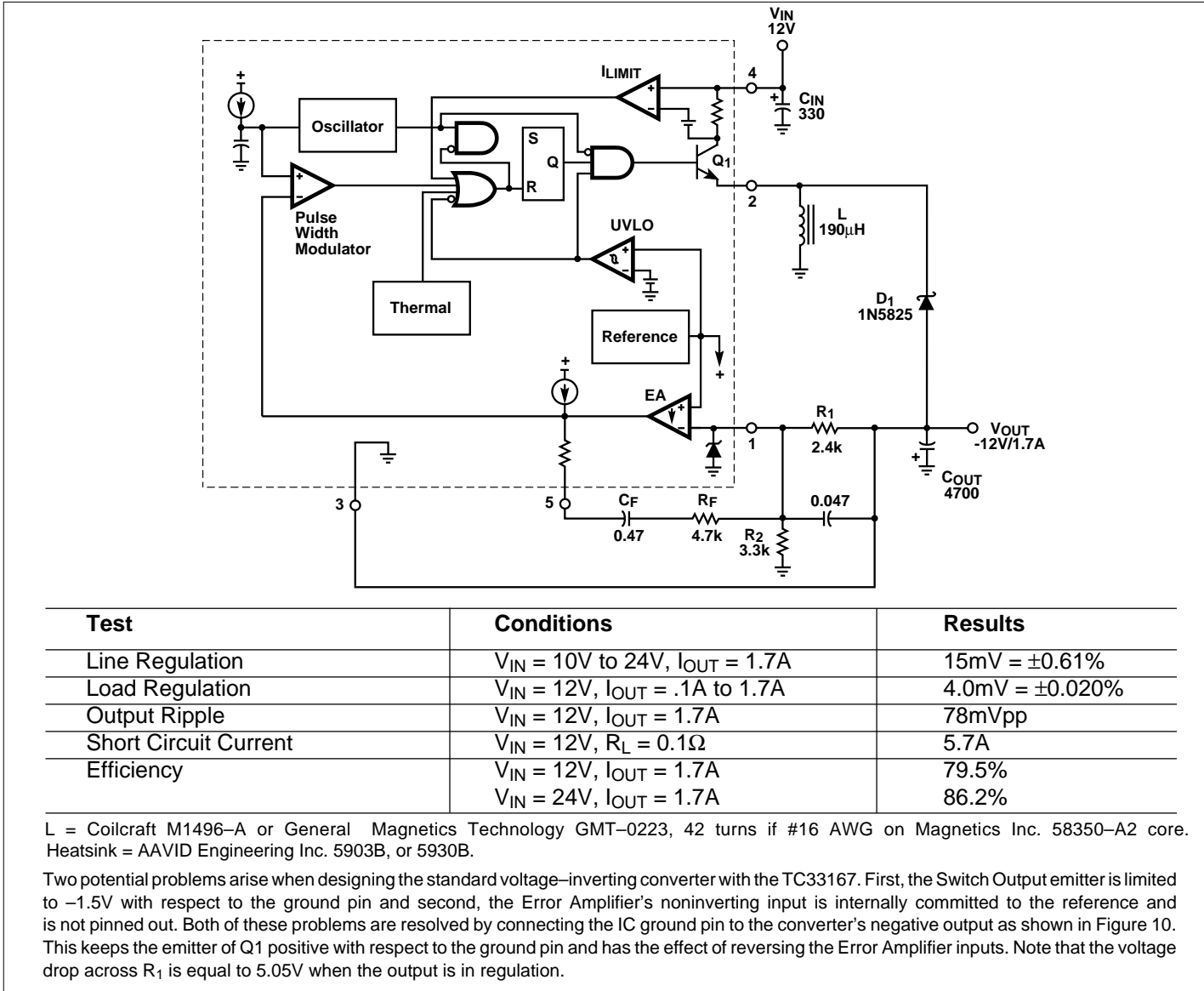


Figure 10. Voltage Inverting Converter

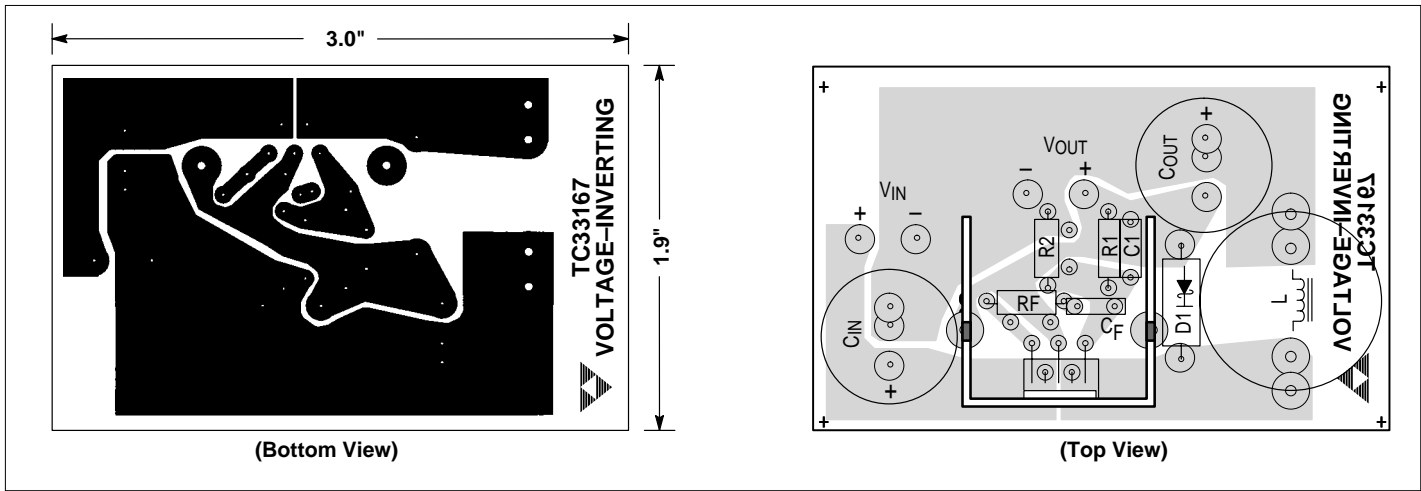


Figure 11. Voltage-Inverting Converter Printed Circuit Board and Component Layout

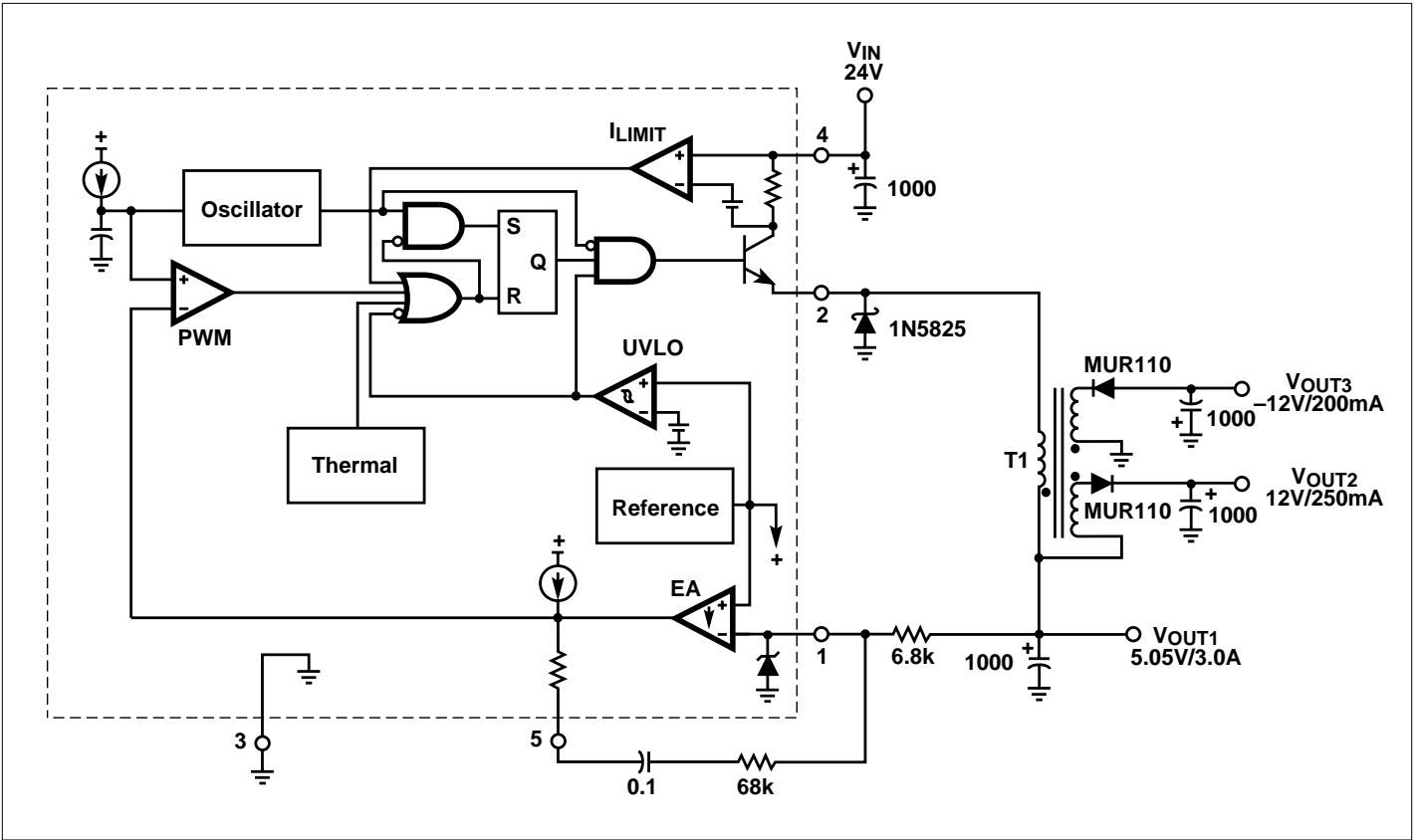


Figure 12. Triple Output Converter

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Tests	Conditions	Results
Line Regulation	5.0V $V_{IN} = 15V \text{ to } 30V$, $I_{OUT1} = 3.0A$, $I_{OUT2} = 250mA$, $I_{OUT3} = 200mA$ 12V -12V	3.0mV = $\pm 0.029\%$ 572mV = $\pm 2.4\%$ 711mV = $\pm 2.9\%$
Load Regulation	5.0V $V_{IN} = 24V$, $I_{OUT1} = 30mA \text{ to } 3.0A$, $I_{OUT2} = 250mA$, $I_{OUT3} = 200mA$ 12V $V_{IN} = 24V$, $I_{OUT1} = 3.0A$, $I_{OUT2} = 100mA \text{ to } 250mA$, $I_{OUT3} = 200mA$ -12V $V_{IN} = 24V$, $I_{OUT1} = 3.0A$, $I_{OUT2} = 250mA$, $I_{OUT3} = 75mA \text{ to } 200mA$	1.0mV = $\pm 0.009\%$ 409mV = $\pm 1.5\%$ 528mV = $\pm 2.0\%$
Output Ripple	5.0V $V_{IN} = 24V$, $I_{OUT1} = 3.0A$, $I_{OUT2} = 250mA$, $I_{OUT3} = 200mA$ 12V -12V	75mV _{PP} 20mV _{PP} 20mV _{PP}
Short Circuit Current	5.0V $V_{IN} = 24V$, $R_L = 0.1\Omega$ 12V -12V	6.5A 2.7A 2.2A
Efficiency	TOTAL $V_{IN} = 24V$, $I_{OUT1} = 3.0A$, $I_{OUT2} = 250mA$, $I_{OUT3} = 200mA$	84.2%

T1 = Primary: Coilcraft M1496-A or General Magnetics Technology GMT-0223, 42 turns of #16 AWG on Magnetics Inc. 58350-A2 core.

T1 = Secondary: V_{OUT2} — 65 turns of #26 AWG

T1 = Secondary: V_{OUT3} — 96 turns of #28 AWG

Heatsink = AAVID Engineering Inc. 5903B, or 5930B.

Multiple auxiliary outputs can easily be derived by winding secondaries on the main output inductor to form a transformer. The secondaries must be connected so that the energy is delivered to the auxiliary outputs when the Switch Output turns off. During the OFF time, the voltage across the primary winding is regulated by the feedback loop, yielding a constant Volts/Turn ratio. The number of turns for any given secondary voltage can be calculated by the following equation:

$$\# \text{ TURNS}_{(SEC)} = \frac{V_{OUT(SEC)} + V_F(SEC)}{\left(\frac{V_{OUT(PRI)} + V_F(PRI)}{\# \text{ TURNS}_{(PRI)}} \right)}$$

Note that the 12 V winding is stacked on top of the 5.0V output. This reduces the number of secondary turns and improves load regulation. For best auxiliary regulation, the auxiliary outputs should be less than 33% of the total output power.

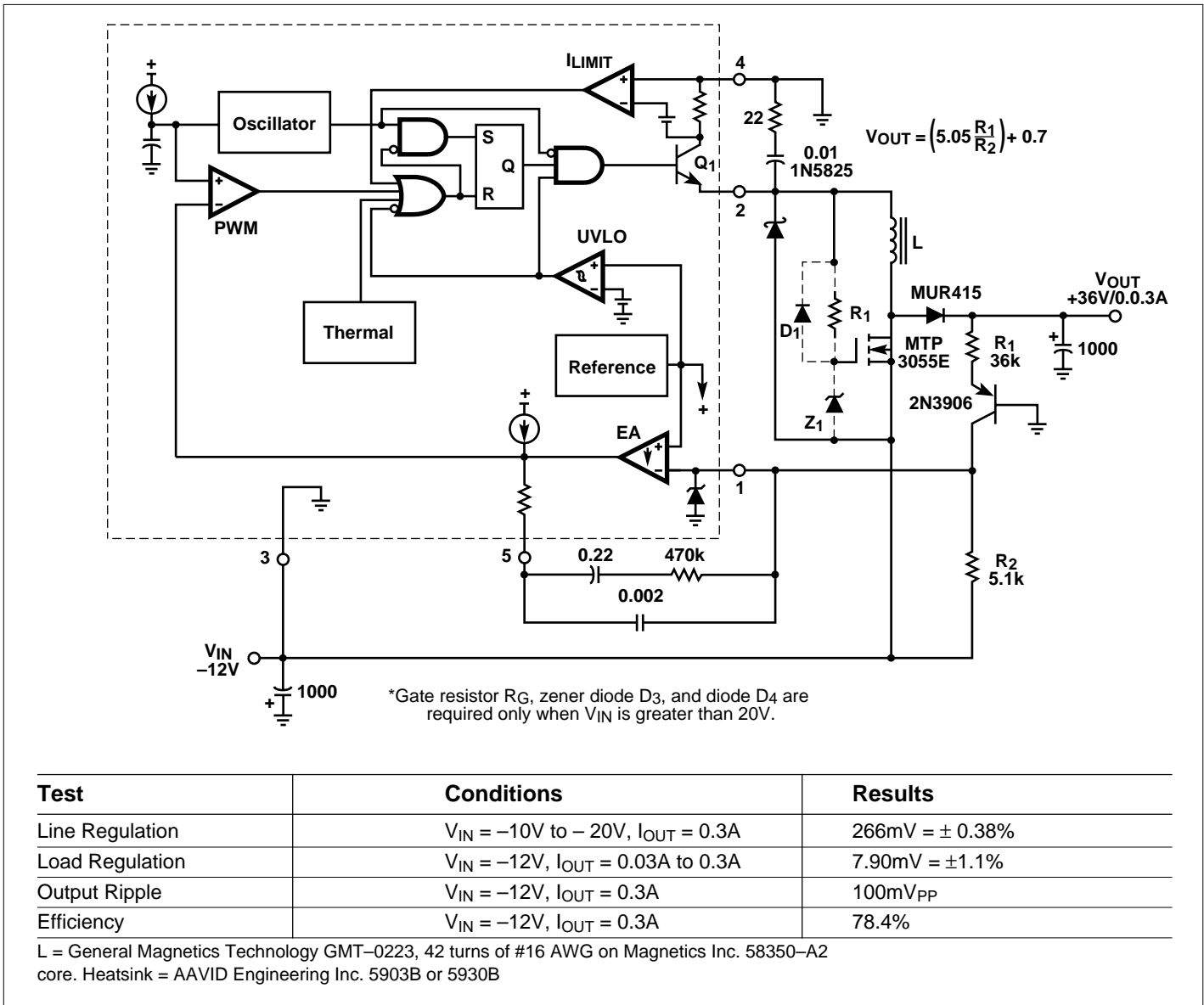
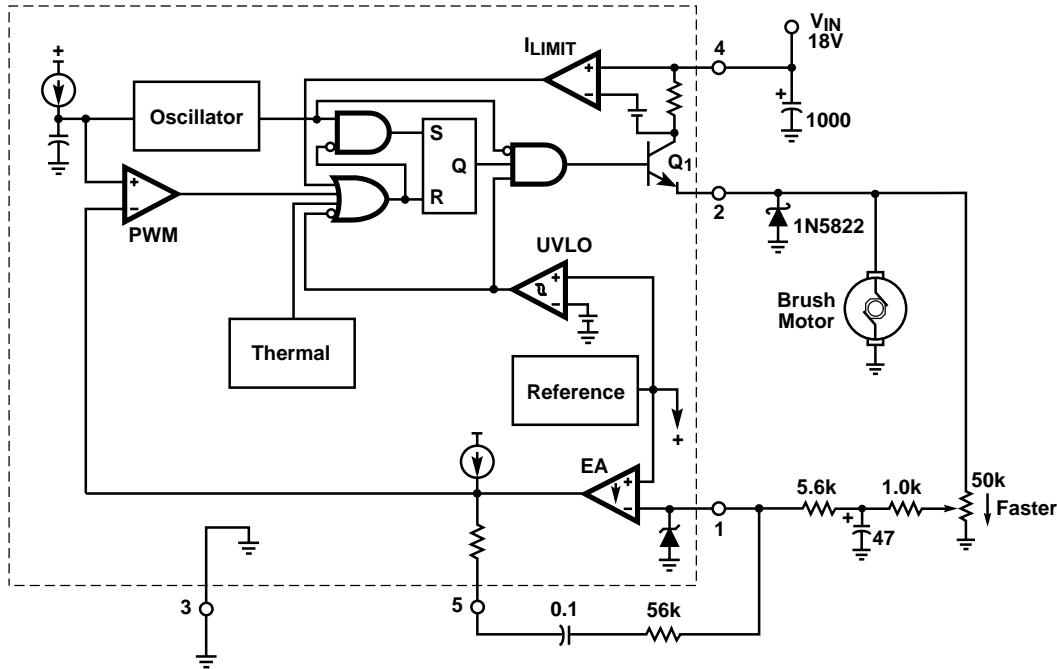


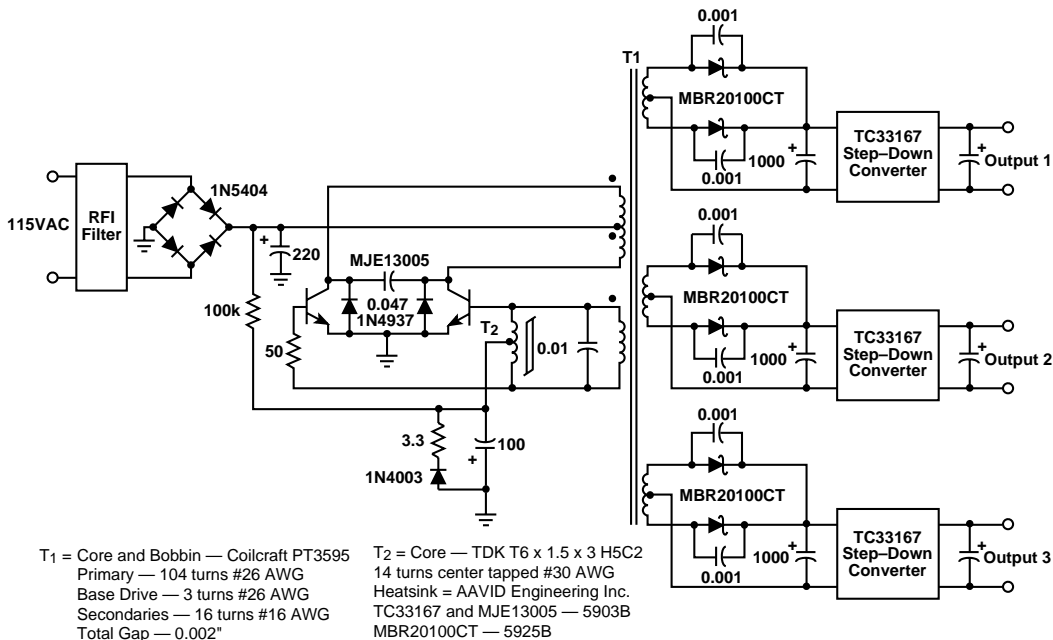
Figure 13. Negative Input/Positive Output Regulator

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Test	Conditions	Results
Low Speed Line Regulation	$V_{IN} = 12V \text{ to } 24V$	1760 RPM $\pm 1\%$
High Speed Line Regulation	$V_{IN} = 12V \text{ to } 24V$	3260 RPM $\pm 6\%$

Figure 14. Variable Motor Speed Control with EMF Feedback Sensing



T₁ = Core and Bobbin — Coilcraft PT3595
Primary — 104 turns #26 AWG
Base Drive — 3 turns #26 AWG
Secondaries — 16 turns #16 AWG
Total Gap — 0.002"

T₂ = Core — TDK T6 x 1.5 x 3 H5C2
14 turns center tapped #30 AWG
Heatsink = AAVID Engineering Inc.
TC33167 and MJE13005 — 5903B
MBR20100CT — 5925B

The TC33167 can be used cost effectively in off-line applications even though it is limited to a maximum input voltage of 40V. Figure 15 shows a simple and efficient method for converting the AC line voltage down to 24V. This preconverter has a total power rating of 125W with a conversion efficiency of 90%. Transformer T₁ provides output isolation from the AC line and isolation between each of the secondaries. The circuit self-oscillates at 50kHz and is controlled by the saturation characteristics of T₂. Multiple TC33167 post regulators can be used to provide accurate independently regulated outputs for a distributed power system.

Figure 15. Off-Line Preconverter

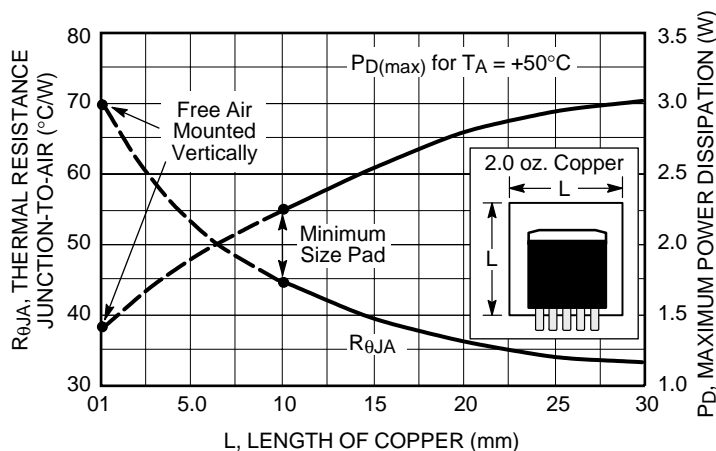


Figure 16. DDPAK Thermal Resistance and Maximum Power Dissipation vs. P.C.B. Copper Length

Calculation	Step-Down	Step-Up/Down	Voltage-Inverting
$\frac{t_{ON}}{t_{OFF}}$ (Notes 1, 2)	$\frac{V_{OUT} - V_F}{V_{IN} - V_{SAT} - V_{OUT}}$	$\frac{V_{OUT} - V_{F1} + V_{F2}}{V_{IN} - V_{SATQ1} - V_{SATQ2}}$	$\frac{ V_{OUT} + V_F}{V_{IN} - V_{SAT}}$
t_{ON}	$\frac{t_{ON}}{t_{OFF}} \cdot \frac{1}{f_{OSC} \left(\frac{t_{ON}}{t_{OFF}} + 1 \right)}$	$\frac{t_{ON}}{t_{OFF}} \cdot \frac{1}{f_{OSC} \left(\frac{t_{ON}}{t_{OFF}} + 1 \right)}$	$\frac{t_{ON}}{t_{OFF}} \cdot \frac{1}{f_{OSC} \left(\frac{t_{ON}}{t_{OFF}} + 1 \right)}$
Duty Cycle (Note 3)	$t_{ON} f_{OSC}$	$t_{ON} f_{OSC}$	$t_{ON} f_{OSC}$
I_{Lavg}	I_{OUT}	$I_{OUT} \left(\frac{t_{ON}}{t_{OFF}} + 1 \right)$	$I_{OUT} \left(\frac{t_{ON}}{t_{OFF}} + 1 \right)$
$I_{pk(SWITCH)}$	$I_L avg + \frac{\Delta I_L}{2}$	$I_L avg + \frac{\Delta I_L}{2}$	$I_L avg + \frac{\Delta I_L}{2}$
L	$\left(\frac{V_{IN} - V_{SAT} - V_{OUT}}{\Delta I_L} \right) t_{ON}$	$\left(\frac{V_{IN} - V_{SATQ1} - V_{SATQ2}}{\Delta I_L} \right) t_{ON}$	$\left(\frac{V_{IN} - V_{SAT}}{\Delta I_L} \right) t_{ON}$
$V_{RIPPLE(pp)}$	$\Delta I_L \sqrt{\left(\frac{1}{8f_{OSC} C_O} \right)^2 + (ESR)^2}$	$\left(\frac{t_{ON}}{t_{OFF}} + 1 \right) \sqrt{\left(\frac{1}{f_{OSC} C_O} \right)^2 + (ESR)^2}$	$\left(\frac{t_{ON}}{t_{OFF}} + 1 \right) \sqrt{\left(\frac{1}{f_{OSC} C_O} \right)^2 + (ESR)^2}$
V_{OUT}	$V_{REF} \left(\frac{R_2}{R_1} + 1 \right)$	$V_{REF} \left(\frac{R_2}{R_1} + 1 \right)$	$V_{REF} \left(\frac{R_2}{R_1} + 1 \right)$

NOTES: 1. V_{SAT} – Switch Output source saturation voltage, refer to Figure 23

2. V_F – Output rectifier forward voltage drop. Typical value for 1N5822 Schottky barrier rectifier is 0.35 V.

3. Duty cycle is calculated at the minimum operating input voltage and must not exceed the guaranteed minimum DC (max) specification of 0.92.

The following converter characteristics must be chosen:

V_{OUT} – Desired output voltage.

I_{OUT} – Desired output current.

ΔI_L – Desired peak-to-peak inductor ripple current. For maximum output current especially when the duty cycle is greater than 0.5, it is suggested that ΔI_L be chosen minimum current limit threshold of 5.5A. If the design goal is to use a minimum inductance value, let $\Delta I_L = 2 (I_L avg)$. This will proportionally reduce the converter's output current capability.

$V_{RIPPLE(pp)}$ – Desired peak-to-peak output ripple voltage. For best performance, the ripple voltage should be kept to less than 2% of V_{OUT} . Capacitor C_O should be a low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.

Figure 17. Design Equations Table

TC33167

TYPICAL CHARACTERISTICS

Figure 17. Voltage Feedback Input Threshold versus Temperature

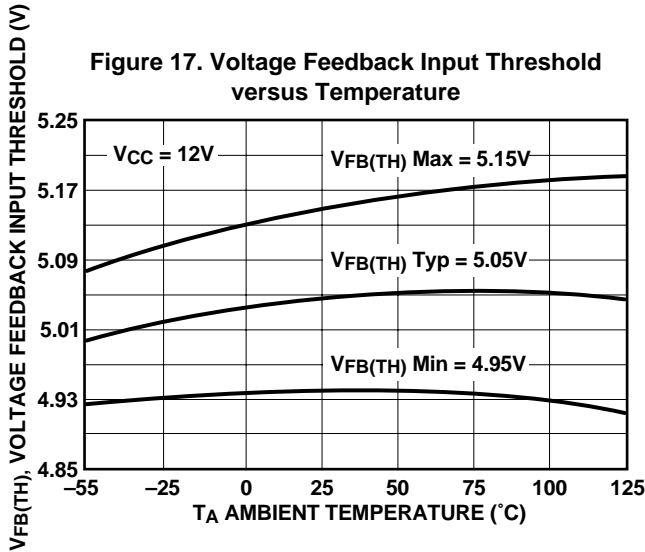


Figure 18. Voltage Feedback Input Bias Current versus Temperature

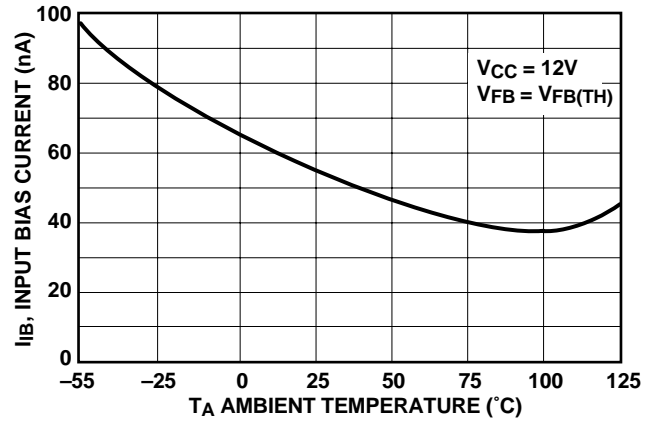


Figure 19. Error Amp Open Loop Gain and Phase versus Frequency

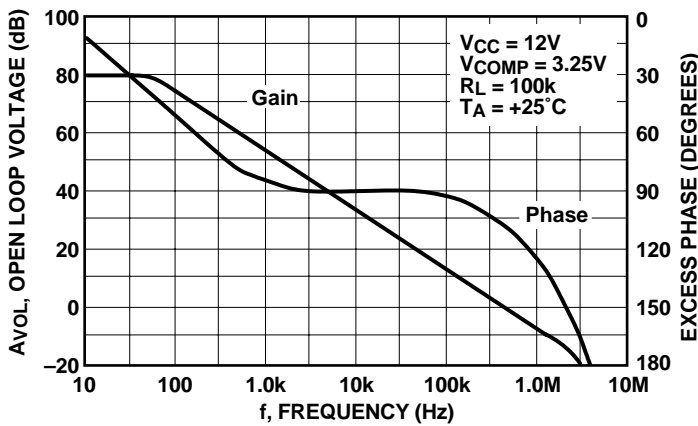


Figure 20. Error Amp Output Saturation versus Sink Current

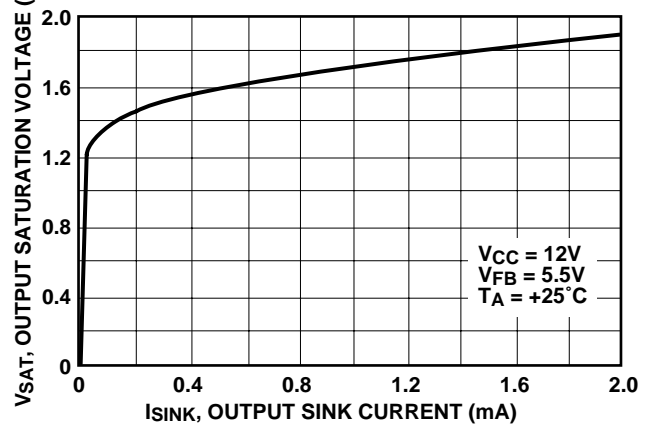


Figure 21. Oscillator Frequency Change versus Temperature

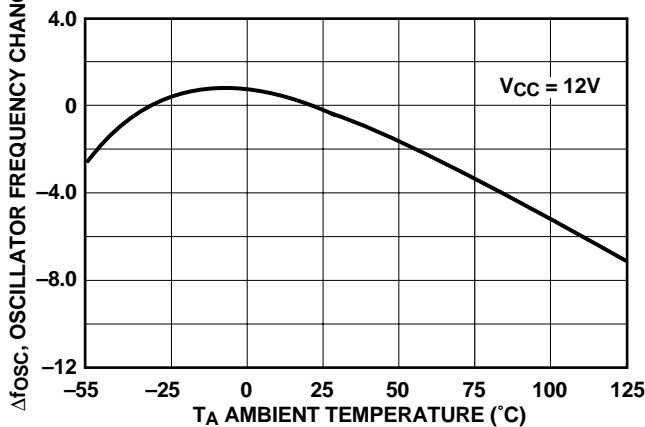
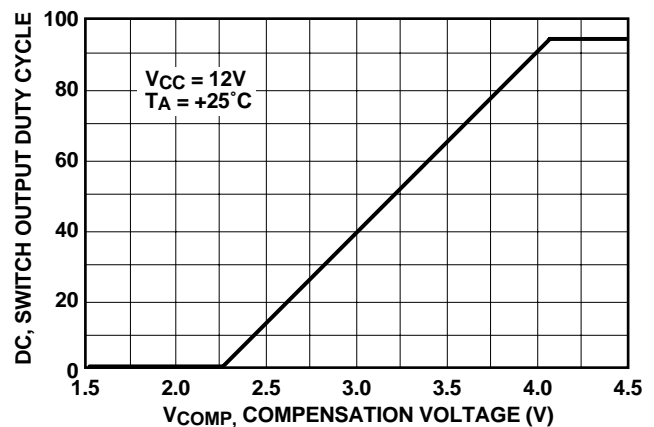


Figure 22. Switch Output Duty Cycle versus Compensation Voltage



TYPICAL CHARACTERISTICS

Figure 23. Switch Output Source Saturation versus Source Current

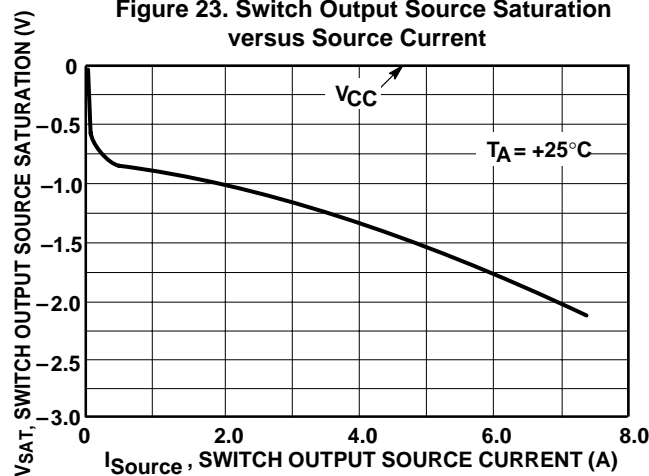


Figure 24. Negative Switch Output Voltage versus Temperature

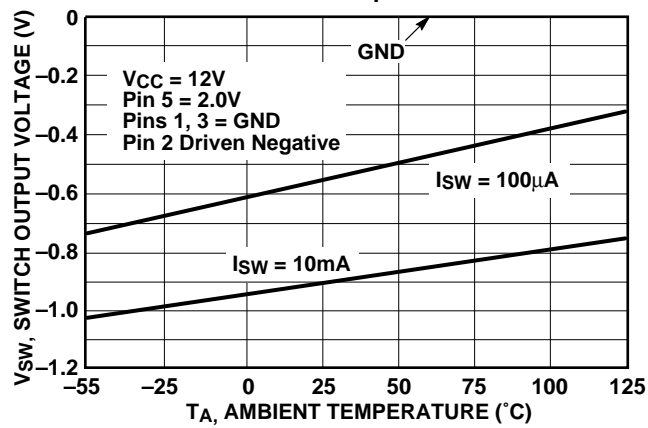


Figure 25. Switch Output Current Limit Threshold versus Temperature

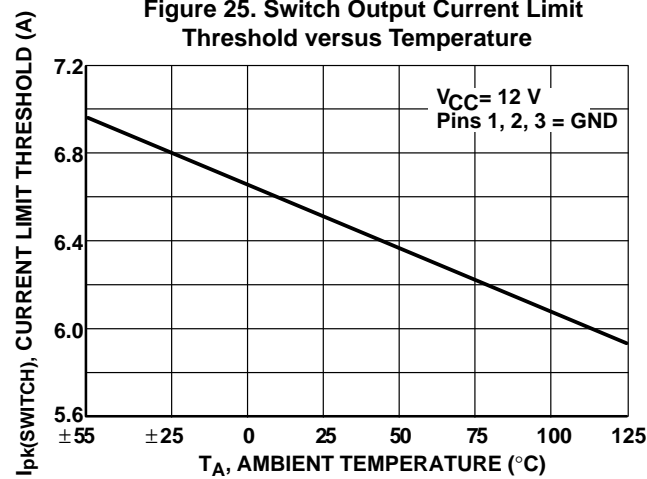


Figure 26. Standby Supply Current versus Supply Voltage

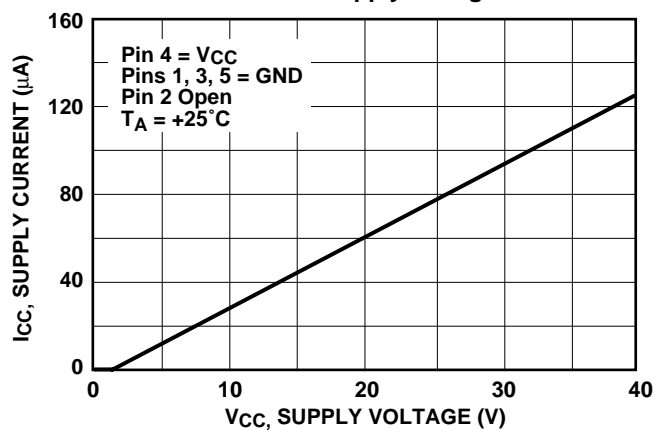


Figure 27. Undervoltage Lockout Threshold versus Temperature

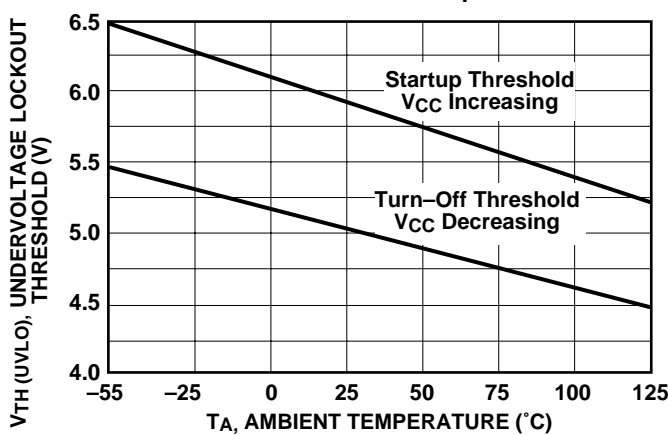
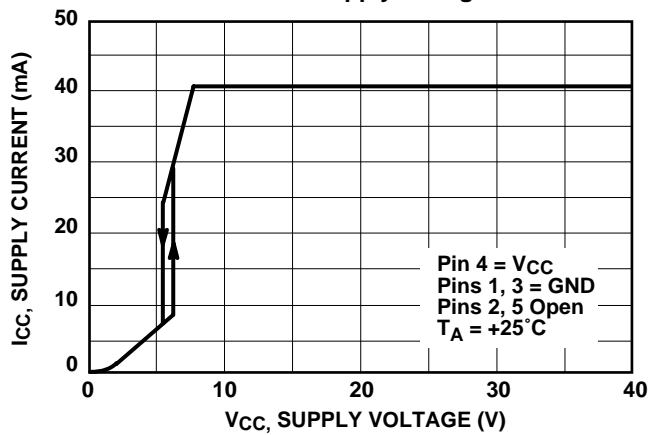
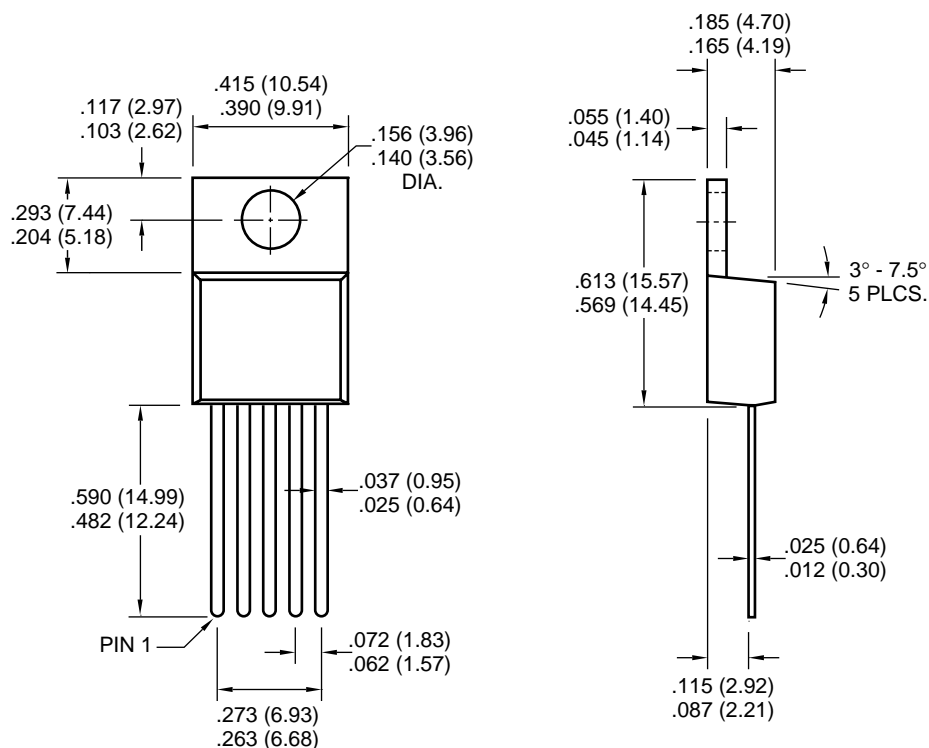


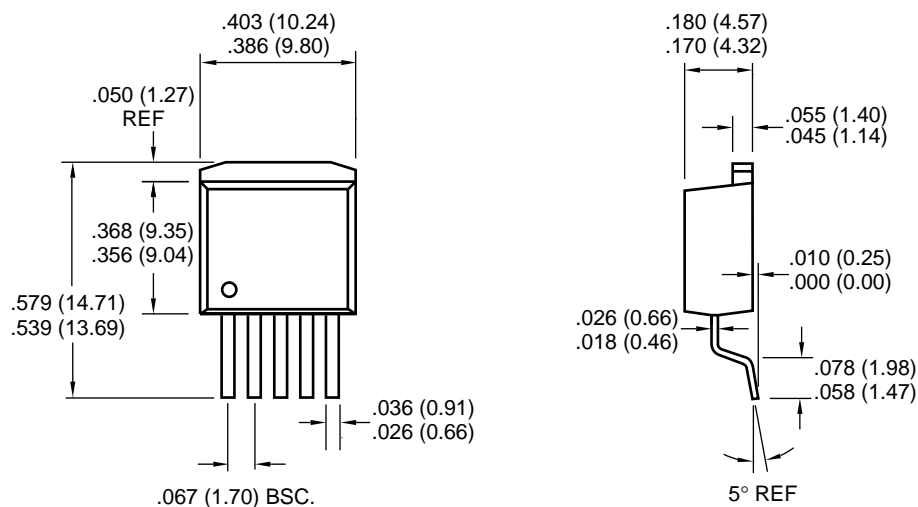
Figure 28. Operating Supply Current versus Supply Voltage



5-Pin TO-220



5-Pin DDPAK-B



Dimensions: inches (mm)

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