ISM 2.4 GHz Front End IC

Description

The T7024 is a monolithic SiGe transmit/ receive front end IC with power amplifier, low-noise amplifier and T/R switch driver. It is especially designed for operation in TDMA systems like Bluetooth, DECT, IEE 802.11 FHSS WLAN, home RF and ISM proprietary radios.

Due to the ramp-control feature and a very low quiescent current an external switch transistor for V_S is not required.

Electrostatic sensitive device.
Observe precautions for handling.

Features

- Single 3-V supply voltage
- High-power-added efficient power amplifier (P_{out} typ. 23 dBm)
- Ramp-controlled output power
- Low-noise preamplifier (NF typ. 2.3 dB)
- Biasing for external PIN diode T/R switch
- Current-saving standby mode
- Few external components
- PSSO20 plastic package with down set paddle heat slug or HP-VFQFP-N20

Block Diagram

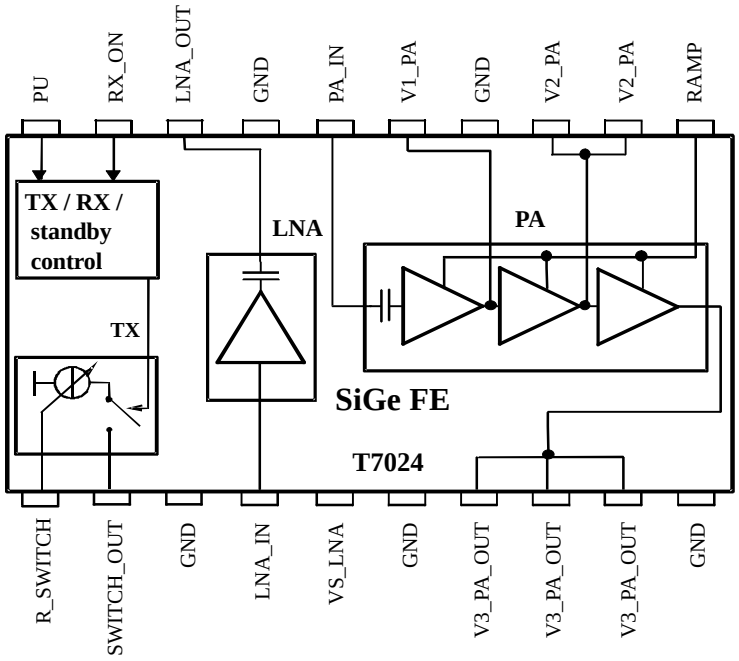


Figure 1. Block diagram

Ordering Information

Extended Type Number	Package	Remarks
T7024-TRS	PSSO20	Tube
T7024-TRQ	PSSO20	Taped and reeled
T7024-PGS	HP-VFQFP-N20	Tube
T7024-PGQ	HP-VFQFP-N20	Taped and reeled
T7024-DB	Flipchip	

Preliminary Information

Pin Description

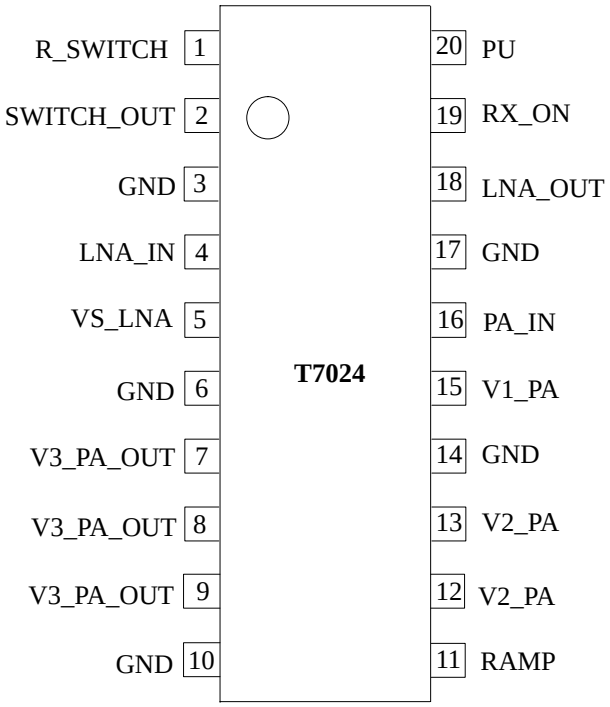


Figure 2. Pinning PSSO20

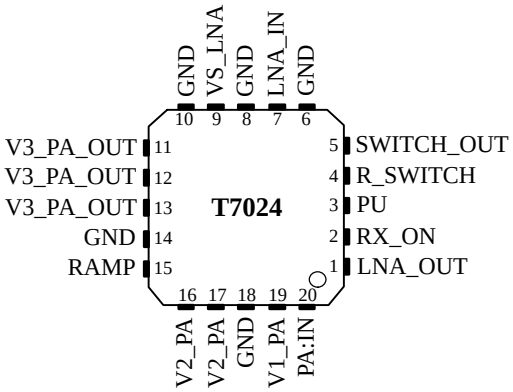


Figure 3. Pinning HP–VFQFP–N20

Pin SSO20	Pin N20	Symbol	Function
1	4	R_SWITCH	Resistor to GND sets the PIN diode current
2	5	SWITCH_OUT	Switched current output for PIN diode
3	6	GND	Ground
4	7	LNA_IN	Low-noise amplifier input
5	9	VS_LNA	Supply voltage input for low-noise amplifier
6	8	GND	Ground
7	11	V3_PA_OUT	Inductor to power supply and matching network for power amplifier output
8	12		
9	13		
10	10	GND	Ground
11	15	RAMP	Power ramping control input
12	16	V2_PA	Inductor to power supply for power amplifier
13	17		
14	14	GND	Ground
15	19	V1_PA	Supply voltage for power amplifier
16	20	PA_IN	Power amplifier input
17	18	GND	Ground
18	1	LNA_OUT	Low-noise amplifier output
19	2	RX_ON	RX active high
20	3	PU	Power-up active high
Slug	Slug	GND	Ground

Pad Description

Pad	Symbol	Function	X–Coordinate of Pad *) (μm)	Y–Coordinate of Pad *) (μm)
1	R_SWITCH	Resistor to GND sets the PIN diode current	0	400
2	SWITCH_OUT	Switched current output for PIN diode	400	400
3	GND	Ground	0	0
4	LNA_IN	Low–noise amplifier input	400	0
5	GND	Ground	800	0
6	VS_LNA	Supply voltage input for low–noise amplifier	1200	0
7	GND	Ground	1600	0
8	GND	Ground	2000	0
9	V3_PA_OUT	Inductor to power supply and matching network for power amplifier output	2400	0
10	GND	Ground	2780	150
11	GND	Ground	2780	550
12	RAMP	Power ramping control input	2780	950
13	V2_PA	Inductor to power supply for power amplifier	2450	1200
14	GND	Ground	2050	1200
15	GND	Ground	1650	1200
16	V1_PA	Supply voltage for power amplifier	1250	1200
17	PA_IN	Power amplifier input	850	1200
18	GND	Ground	400	1200
19	LNA_OUT	Low–noise amplifier output	0	1200
20	RX_ON	RX active high	0	800
21	PU	Power–up active high	400	800

*) relative to centre of Pad 3

Pad Location

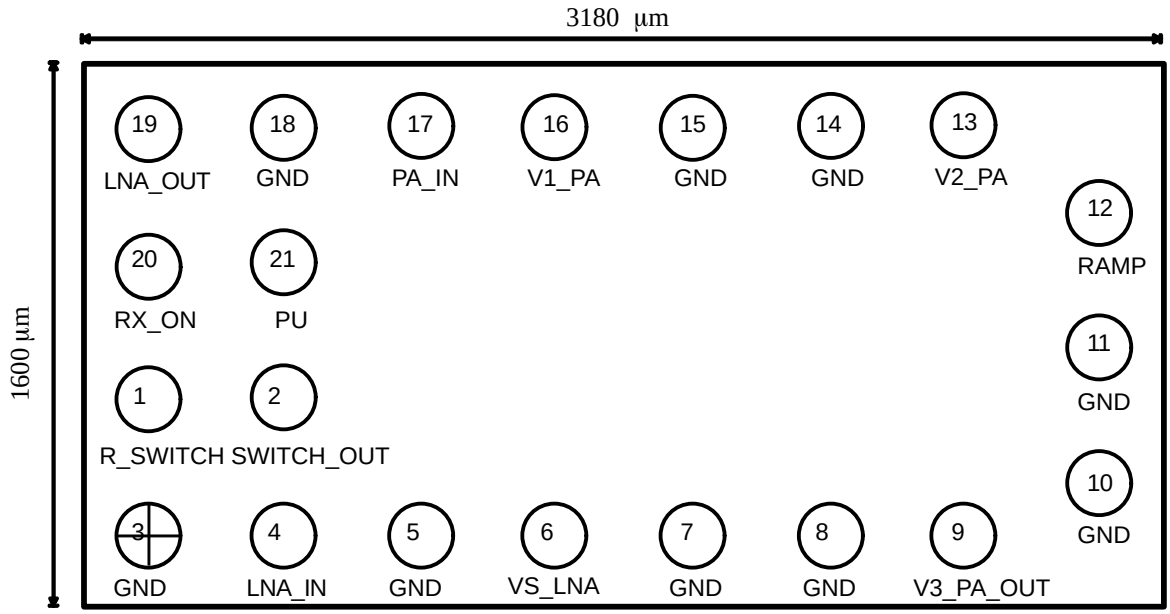


Figure 4. Pad location

Absolute Maximum Ratings

All voltages are referred to ground (Pins GND and slug), no RF

Parameters		Symbol	Value	Unit
Supply voltage	Pins VS_LNA, V1_PA, V2_PA and V3_PA_OUT	V_S	6	V
Junction temperature		T_j	150	°C
Storage temperature		T_{stg}	–40 to +125	°C
RF input power LNA		P_{inLNA}	LNA – 5 dBm	dBm
RF input power PA		P_{inPA}	PA + 10 dBm	dBm

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction ambient PSSOP20	R_{thJA}	19	K/W
Junction ambient HP–VFQFP–N20	R_{thJA}	27	K/W

Operating Range

All voltages are referred to ground (Pins GND and slug). Power supply points are VS_LNA, V1_PA, V2_PA, V3_PA_OUT. The following table represents the sum of all supply currents depending on the TX/RX mode.

Parameters		Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Pins V1_PA, V2_PA and V3_PA_OUT	V_S	2.7	3.0	4.6	V
Supply voltage	Pin VS_LNA	V_S	2.7	3.0	5.5	V
Supply current	TX RX	I_S I_S		190 8		mA mA
Standby current	PU = 0	I_S		10		µA
Ambient temperature		T_{amb}	–25	+25	+70	°C

Electrical Characteristics

Test conditions (unless otherwise specified): V_S = 3.0 V, T_{amb} = 25°C

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Power amplifier [1)]						
Supply voltage	Pins VS_LNA, V1_PA, V2_PA and V3_PA_OUT	V_S	2.7	3.0	4.6	V
Supply current	TX	I_{S_TX}		190		mA
	RX (PA off), $V_{RAMP} \leqq 0.1$ V	I_{S_RX}			10	µA
Standby current	Standby	$I_{S\_standby}$			10	µA
Frequency range	TX	f	2.4		2.5	GHz

Electrical Characteristics (continued)

Test conditions (unless otherwise specified): V_S = 3.0 V, T_{amb} = 25°C

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Gain-control range	TX	ΔGp	60	42		dB
Power gain max.	TX	Gp	28	30	33	dB
Power gain min.	Pin PA_IN to V3_PA_OUT	Gp	–40		–17	dB
Ramping voltage max.	TX, power gain (max) Pin RAMP	$V_{RAMP\ max}$	1.7	1.75	1.83	V
Ramping voltage min.	TX, power gain (min) Pin RAMP	$V_{RAMP\ min}$		0.1		V
Power-added efficiency	TX	PAE	30	35		%
Saturated output power	TX, input power = 0 dBm referred to Pins V3_PA_OUT	P_{sat}	22.5	23	23.5	dBm
Input matching [2]	TX Pin PA_IN	Load VSWR		<1.5:1	1.5 : 1	
Output matching [2]	TX Pins V3_PA_OUT	Load VSWR		<1.5:1	1.5 : 1	
Harmonics @P 1dBCP	TX Pins V3_PA_OUT	2 fo			–30	dBc
Harmonics @P 1dBCP	TX Pins V3_PA_OUT	3 fo			–30	dBc
T/R–switch driver (current programming by external resistor from R_SWITCH to GND)						
Switch-out current output	Standby Pin SWITCH_OUT	$I_{S\_O\_standby}$			1	µA
	RX	$I_{S\_O\_RX}$			1	µA
	TX @ 100 Ω	$I_{S\_O\_100}$		1.7		mA
	TX @ 1.2 kΩ	$I_{S\_O\_1k2}$		7		mA
	TX @ 33 kΩ	$I_{S\_O\_33k}$		17		mA
	TX @ ∞	$I_{S\_O\_\infty}$		19		mA
Low-noise amplifier [3]						
Supply voltage	All Pin VS_LNA	V_S	2.7	3.0	5.5	V
Supply current	RX	I_S		8	9	mA
Supply current (LNA and control logic)	TX (control logic active) Pin VS_LNA	I_S			0.5	mA
Standby current	Standby Pin VS_LNA	$I_{S\_standby}$		1	10	µA
Frequency range	RX	f	2.4		2.5	GHz
Power gain	RX Pin LNA_IN to LNA_OUT	Gp	15	16	19	dB
Noise figure	RX	NF		2.3	2.5	dB

Electrical Characteristics (continued)

Test conditions (unless otherwise specified): V_S = 3.0 V, T_{amb} = 25°C

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Gain compression	RX, referred to Pin LNA_OUT	O1dB	–9	–7	–6	dBm
3rd-order input interception point	RX	IIP3	–16	–14	–13	dBm
Input matching [4]	RX Pin LNA_IN	VSWR in		<2:1	2:1	
Output matching [4]	RX Pin LNA_OUT	VSWR out		<2:1	2:1	
Logic input levels (RX_ON, PU)						
High input level	= '1' Pins RX_ON and PU	V_{iH}	2.4		$V_{S, LNA}$	V
Low input level	= '0'	V_{iL}	0		0.5	V
High input current	= '1' V_{iH} = 2.4 V	I_{iH}		40	60	µA
Low input current	= '0'	I_{iL}			0.2	µA

Note: 1) Power amplifier shall be unconditional stable, maximum duty cycle 100%, true cw operation, maximum load mismatch and duration t.b.d.
2) With external matching network, load impedance 50 Ω
3) Low-noise amplifier shall be unconditional stable
4) with external matching components

Control Logic for LNA and T/R-Switch Driver

	PU
Power up	1
Standby	0

	RX_ON
RX mode	1
TX mode	0

Typical Operating Characteristics

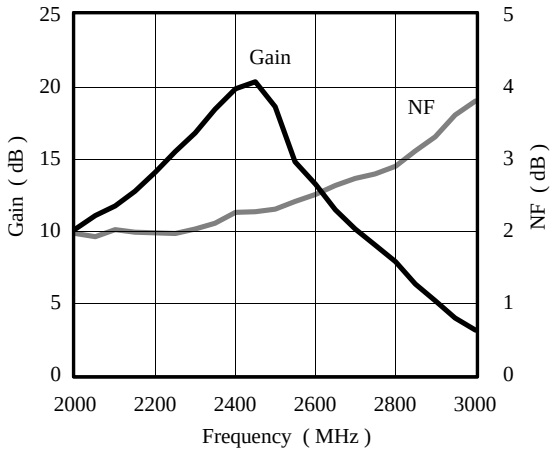


Figure 5. Gain and noise figure vs. frequency

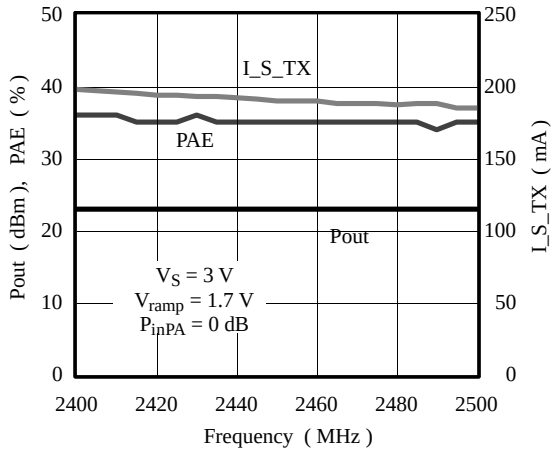


Figure 8. Output power and PAE vs. frequency

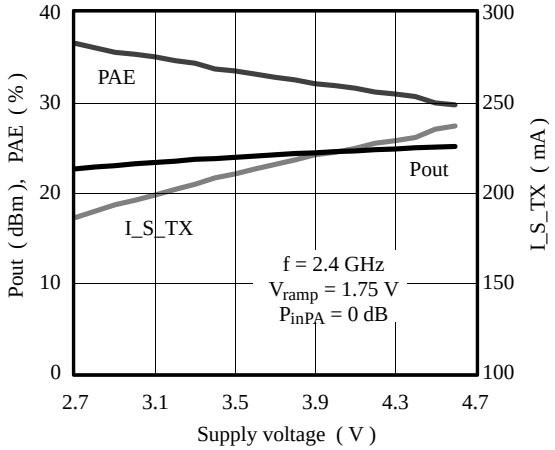


Figure 6. Output power and PAE vs. supply voltage

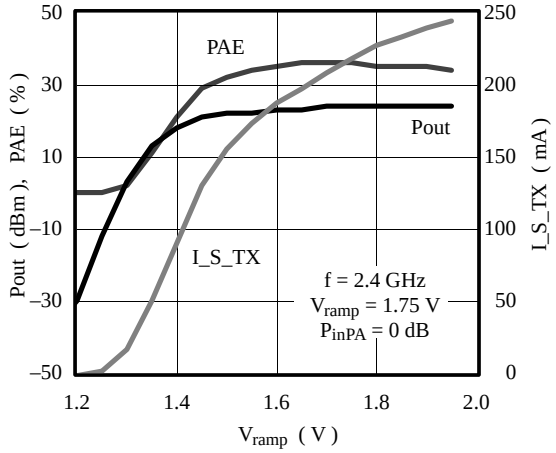


Figure 9. Output power and PAE vs. ramp voltage

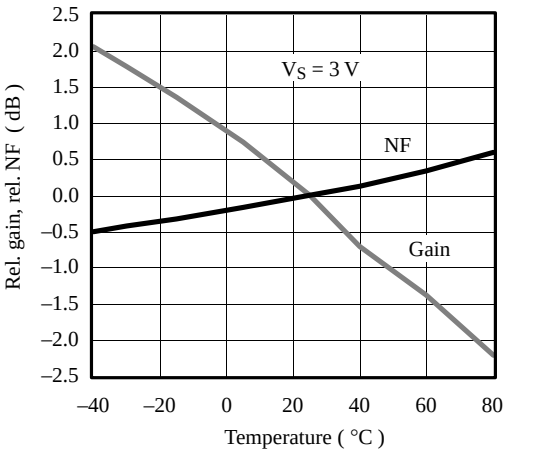


Figure 7. NF and gain vs. temperature

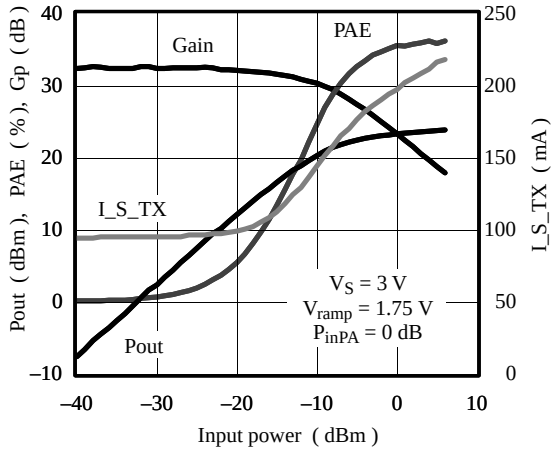


Figure 10. Output power and PAE vs. input power

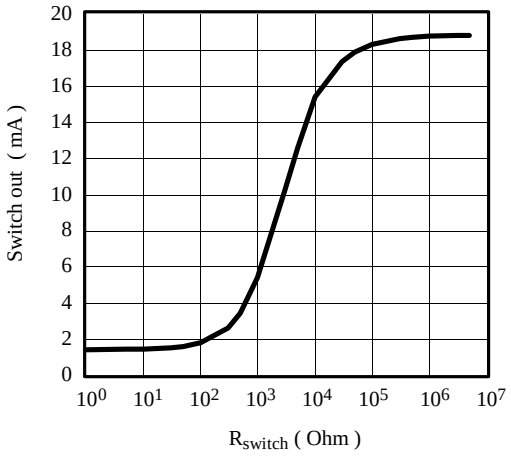


Figure 11. Typical switch-out current vs. R_{switch}

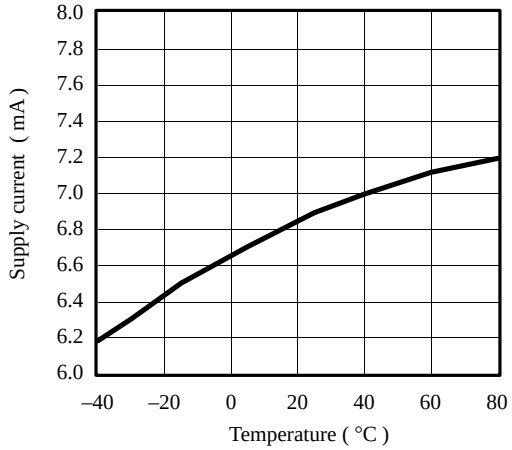


Figure 12. Supply current vs. temperature

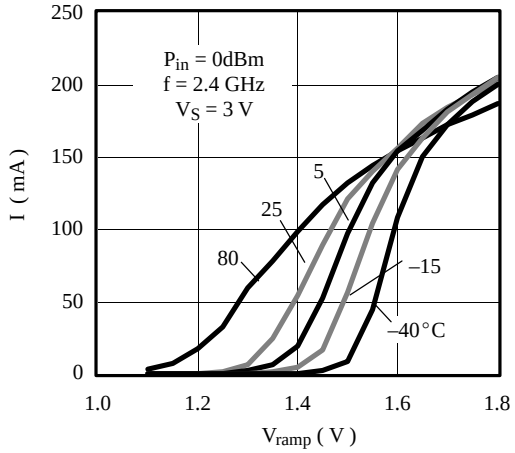


Figure 13. Current vs. V_{ramp} and temperature

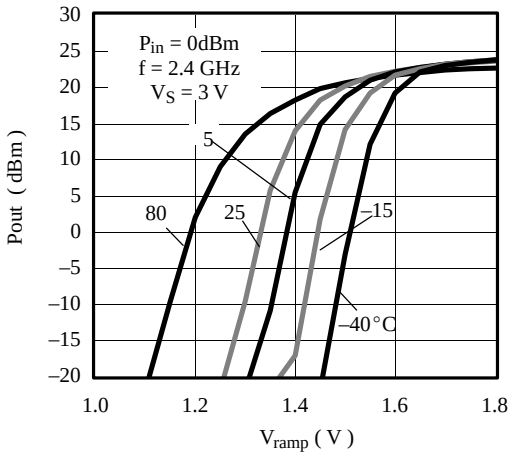


Figure 14. P_{out} vs. V_{ramp} and temperature

Input / Output Circuits

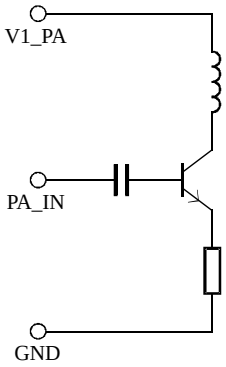


Figure 15.

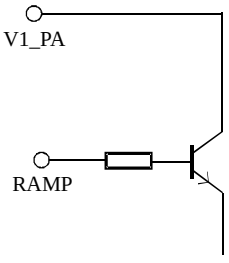


Figure 16.

Input / Output Circuits (continued)

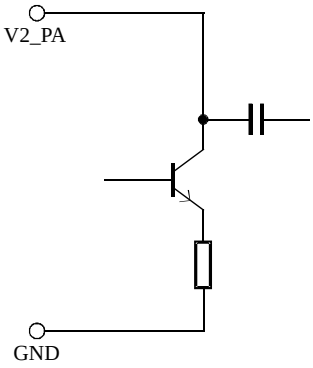


Figure 17.

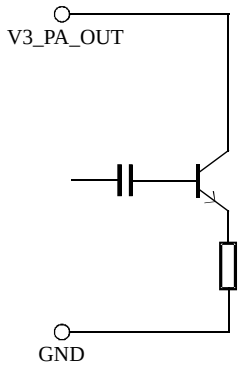


Figure 18.

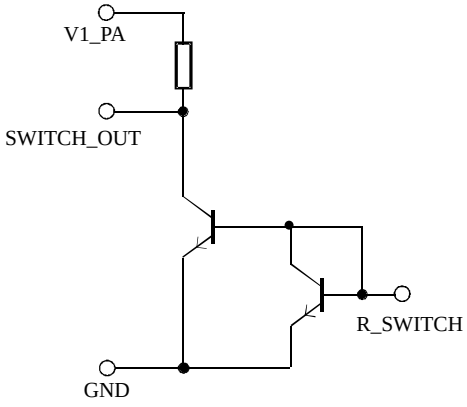


Figure 19.

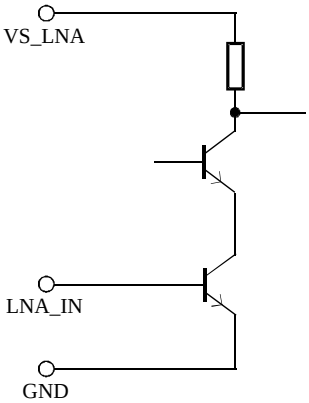


Figure 20.

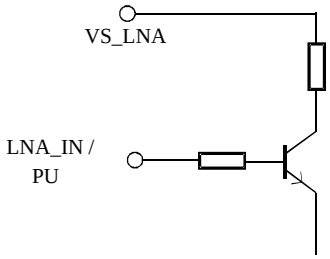


Figure 21.

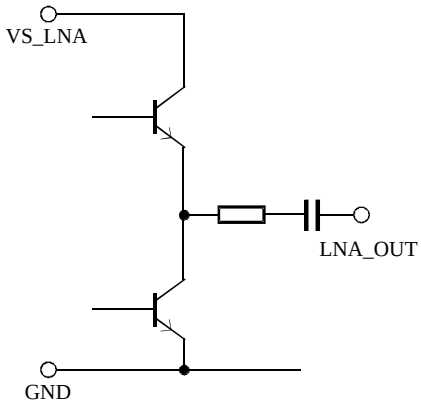


Figure 22.

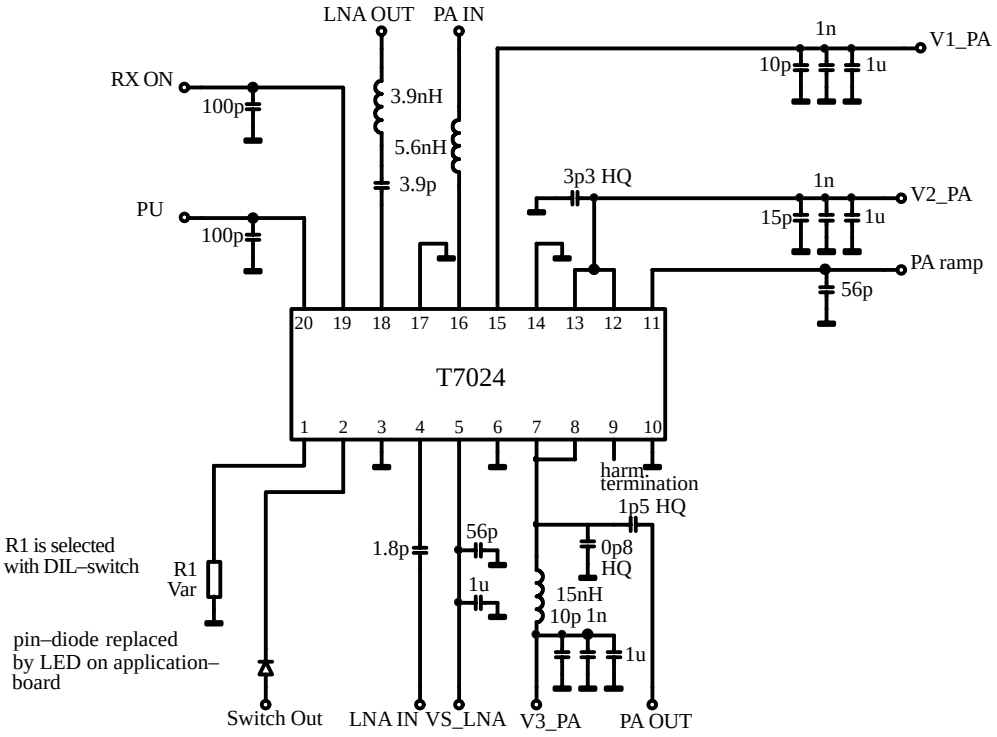


Figure 23. Application board SS020

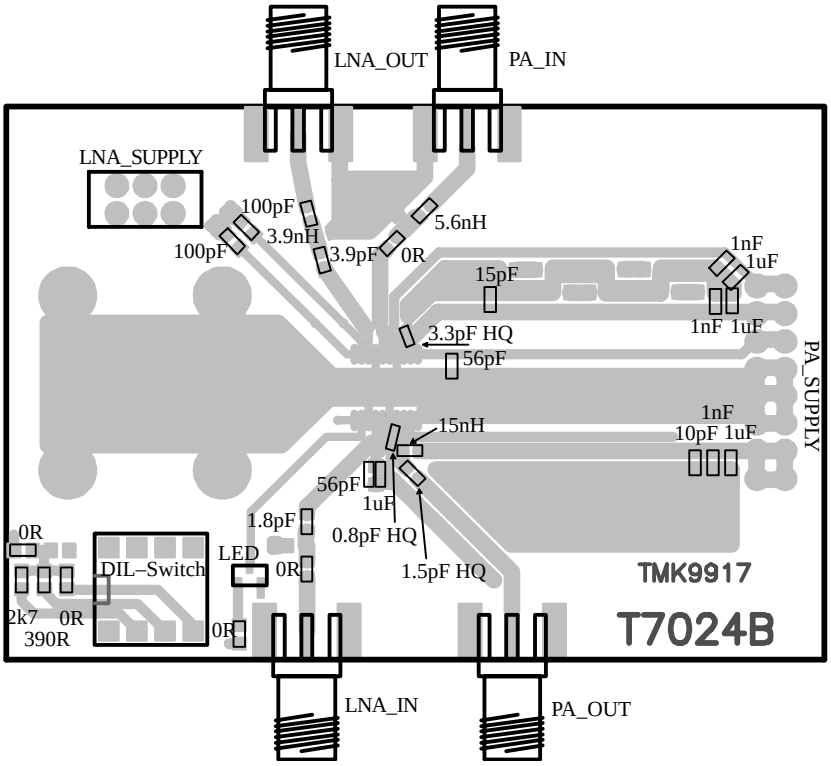


Figure 24. Layout for SSO20

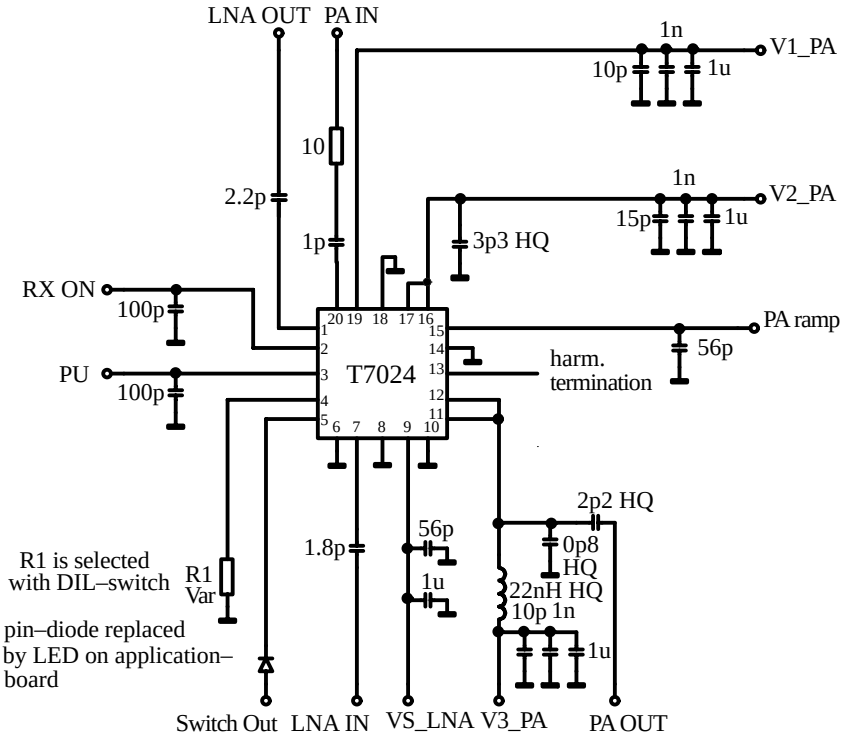


Figure 25. Application board N20

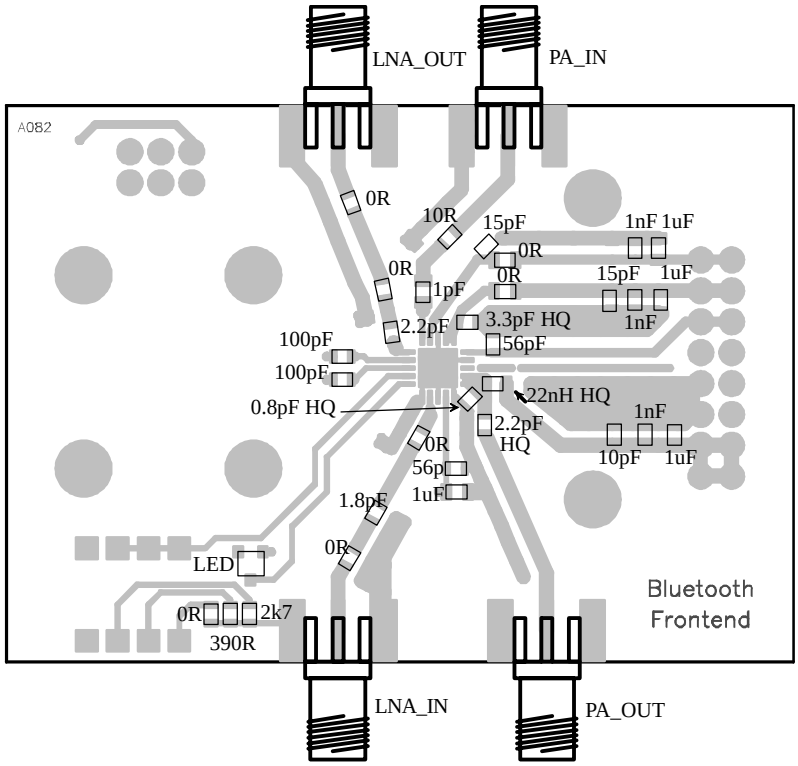
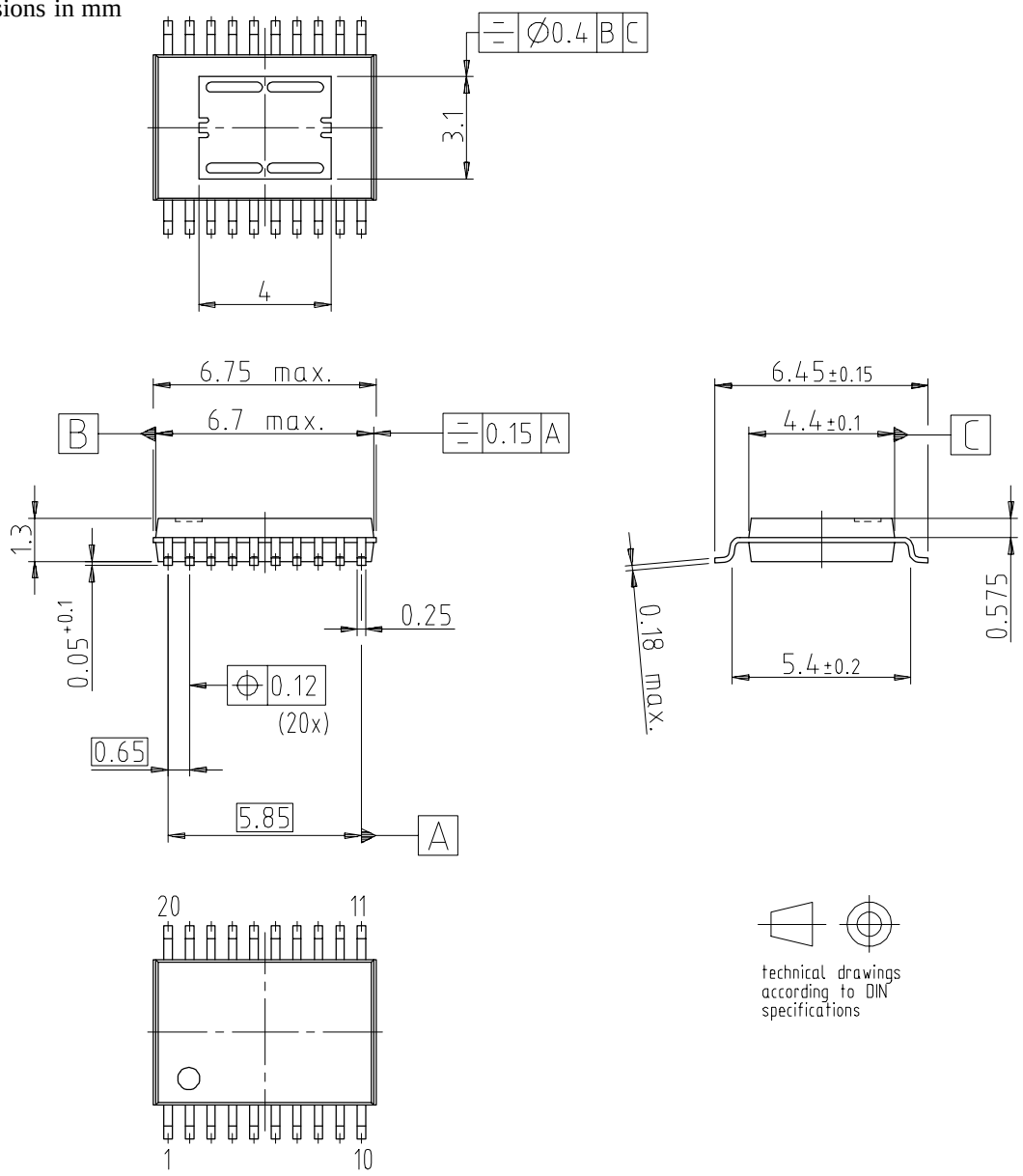


Figure 26. Layout for N20

Package Information

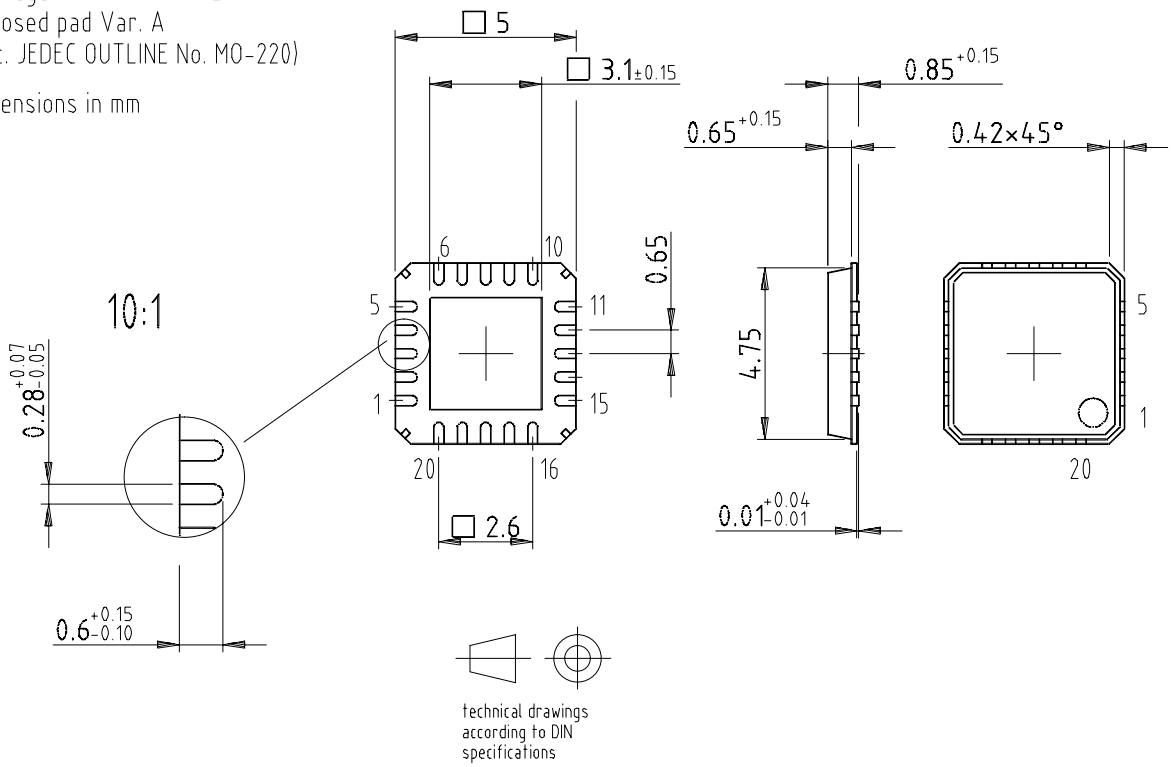
Package PSSO20
Dimensions in mm



Preliminary Information

Package: HP-VFQFP-N20
Exposed pad Var. A
(acc. JEDEC OUTLINE No. MO-220)

Dimensions in mm



Preliminary Information

Ozone Depleting Substances Policy Statement

It is the policy of **Atmel Germany GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Atmel Germany GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Atmel Germany GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

Data sheets can also be retrieved from the Internet: http://www.atmel–wm.com

Atmel Germany GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany
Telephone: 49 (0)7131 67 2594, Fax number: 49 (0)7131 67 2423