TC3001

ETHERNET SILICON 10BASE-T FILTER & BUFFER

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Ethernet Silicon 10Base-T Filter & Buffer

1. Features

- IEEE802.3 10BaseT Compatible.
- High output impedance in disable mode (Ideal for 100/10 Fast Ethernet applications).
- Light input loading (1 CMOS Load) to host.
- 16 Pin SSOP.
- Need only one simple Transformer for Isolation.
- Independent Transmit and Receive functions.
- Pre-distortion of 5MHZ signals included.
- For LAN card, PCMCIA, HUB, Switches, and 100/10 Fast Ethernet applications.
- Loopback function for diagnostics.
- Optional automatic polarity correction.
- Optional single-ended/differential signaling on TXIP/TXIN and RXOP/RXON.
- Patented .

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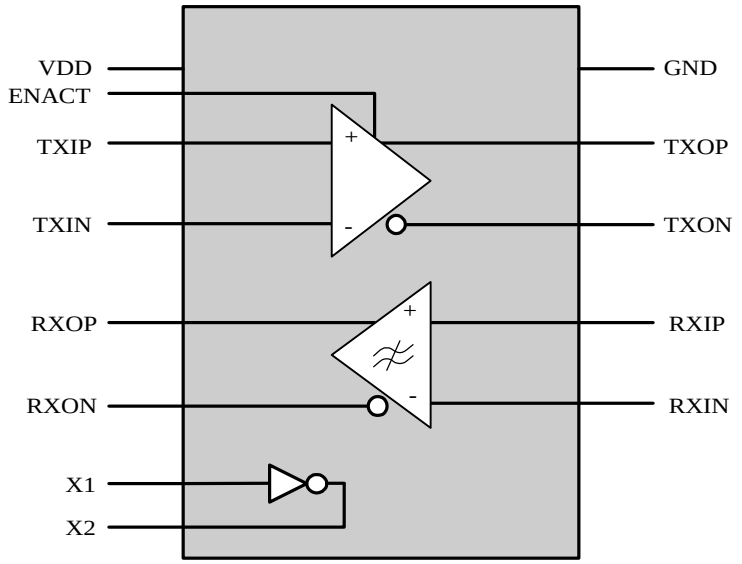
2. General Description

Conventional 10BaseT filters are made of many tiny coils and capacitors connected in ladder form. This type of passive filters have no voltage or current gain, and have low impedance unsuitable for 100MHZ/10MHZ Fast Ethernet applications. The bulky size of these filters also made them unsuitable for demanding PCMCIA spacing requirements.
Very strong output buffers are needed to "Drive" these passive filters and at the same time meeting IEEE analog templates. Simultaneous switching noises and power consumption become un-manageable when the number of output buffers in a chip increase. These noises cause harmonic contents to increase beyond certain pre-described levels. All these difficulties made it almost impossible for a system designer to include all buffers into his 100% digital "Custom" IC designs.
TC3001 with 1 set of active filters and buffers in one package both solves all these problems and serves as a friendly interface between digital IC and 10BaseT unshielded twisted pair (UTP) media.
With TC3001, many new design concepts can be realized. For example, a "Custom" intelligent HUB or Etherswitch implemented in 100% digital FPGA'S or gate arrays. Cost reduction of conventional dumb HUBs. Space-reduction, and cost reduction of PCMCIA designs. Finally, 100/10 fast Ethernet applications with existing 10BaseT transceivers.
Examples:

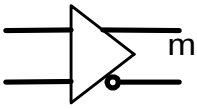
(1). An 8 port dumb HUB with single chip controller may have difficulty passing FCC using low cost 2-layer PCB board, due to simultaneous switching noises occur inside the controller chip. Using TC3001's should help to improve the FCC situation.

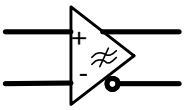
(2). In LAN + Modem PCMCIA designs, precious spacing was consumed by big and flat passive 10BaseT filter. This type of filter has potential thermal stress problem during SMT process. With TC3001 and a transformer, more space can be put back to use by other circuitry.

3. TC3001 Block Diagram



TC3001

Where  means filtering function, and  means Buffer.

 means Buffer with filtering function.

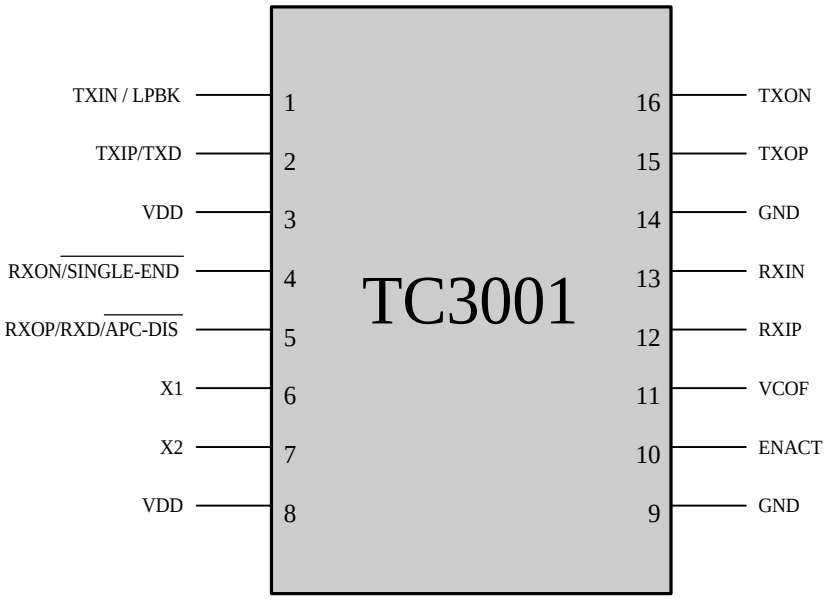
The transmitter converts digital Manchester encoded data from third party twisted pair interface controller to the twisted pair cable. The circuit provides pre-distorted and filtered waveforms so that the outputs are made to appear as if it had passed through 5-7th order external passive filter, thereby only a isolation pulse transformer is needed.

The receiver converts the manchester-encoded data from the twisted pair cable to TTL digital level signal and passes it to twisted pair interface controller. The receiver includes the squelch function which is used to prevent noise from activating the receiver. The input voltage should exceed ±400mV Vp-p and pulse width exceed 25ns for 3 bits times for unsquelch to occur. While in the unsquelch state, the receiver circuit looks for the start of idle signal at the end of packet.

The enable/disable signal pin ENACT in low state puts TXOP and TXON into high impedance tri-state. This is very useful in the 100MHZ/10MHZ situation. A Fast Ethernet signal can operate normally in the same twisted pair cable, with 10BaseT portion in high impedance state. No over loading situation will occur. Any conventional 10BaseT transceiver with a TC3001 is suitable for 100/10 Fast Ethernet applications.

A 20MHZ clock signal is needed at X1 pin for internal precision delay reference. No extra crystal or oscillator is needed. One needs only to bring from existing 20MHZ clock on board to the X1 pin. In the case of multiple TC3001's applications such as HUBs, X2 pin of the first TC3001 should connect to X1 pin of the 2nd TC3001, and X2 pin of the 2nd TC3001 should connect to X1 pin of the 3rd TC3001, and so on, to prevent over loading of the 20MHZ clock source. Phase difference between TC3001's does not matter.

4. TC3001 Pin Diagram



5. TC3001 Pin Description

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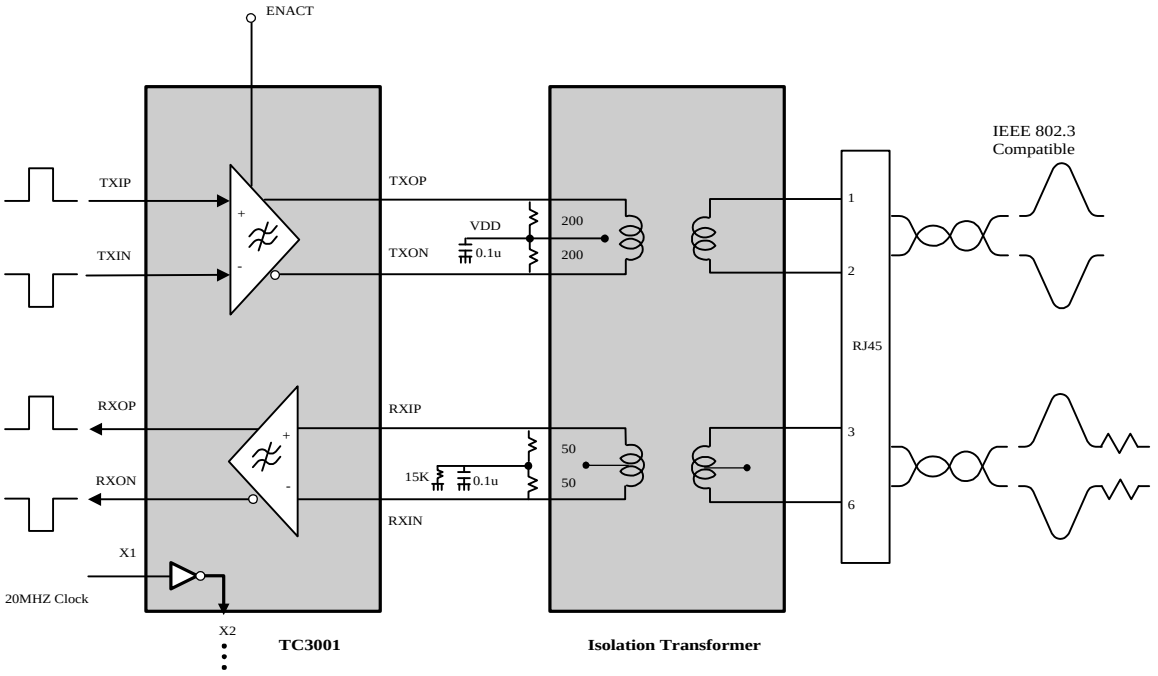
Pin No.	Pin Name	I/O	Description
1	TXIN	I	The differential digital manchester coded data input, negative.
	LPBK	I	If single-ended signaling mode is selected, this pin becomes loopback select input. Setting this pin to high enables loopback of transmit data TXD onto the receive data path RXD.
2	TXIP	I	The differential digital manchester coded data input, positive.
	TXD		Single-ended digital manchester coded data input if single-ended signaling mode is selected.
16,15	TXON/TXOP	O	The differential wave-filtered data output pins to the twisted pair cable.
4	RXON	O	The differential digital manchester coded data output to the twisted pair interface controller, negative.
	$\overline{\text{S-END}}$	I	Single-ended signaling mode select input used to select differential or single-ended signaling on TXI and RXO. This pin is sampled during power-on reset. When setting low, single-ended signaling mode is selected. Pullup internally.
5	RXOP	O	The differential digital manchester coded data output to the twisted pair interface controller, positive.
	RXD		Single-ended digital manchester coded data output if single-ended signaling mode is selected.
	$\overline{\text{APC-DIS}}$	I	Automatic-polarity correction disable input. This pin is sampled during power-on reset. When setting low, automatic-polarity correction function is disabled. Pullup internally.

(2 of 2)

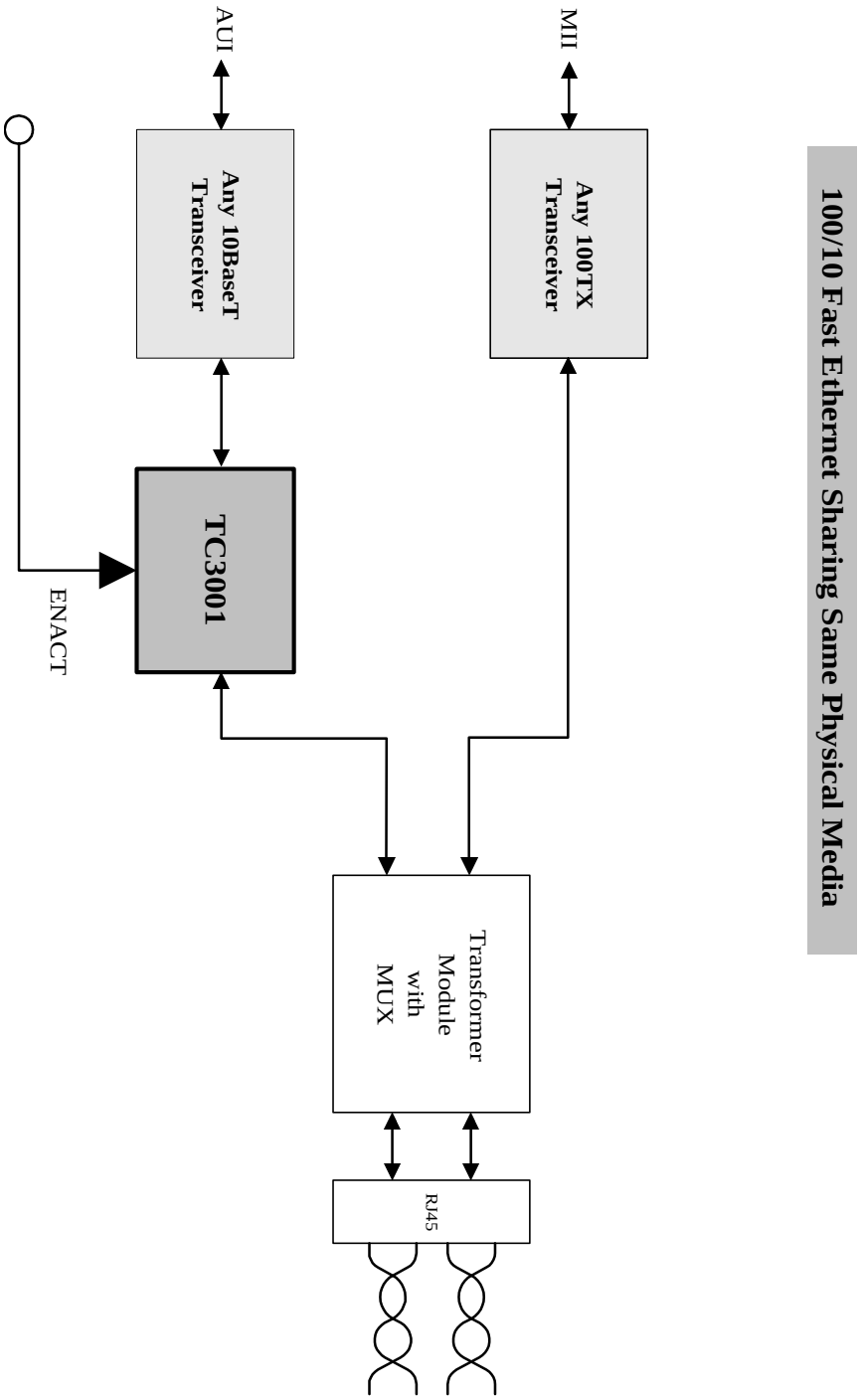
Pin No.	Pin Name	I/O	Description
13,12	RXIN/RXIP	I	The differential manchester coded data input pins from the twisted pair cable.
6	X1	I	20MHZ clock input pin.
7	X2		20MHZ clock output pin.
10	ENACT	I	Input high enables transmitter output driver. Input low disables transmitter output drivers, and makes TXON/TXOP at tri-state. Pullup internally.
11	VCOF	I/O	Filter input pin for internal phase locked loop circuit.
3,8	VDD		power 5V pin.
14,9	GND		Ground pin.

6. Application Diagram (10BaseT Filter with Buffering and Disable Mode)

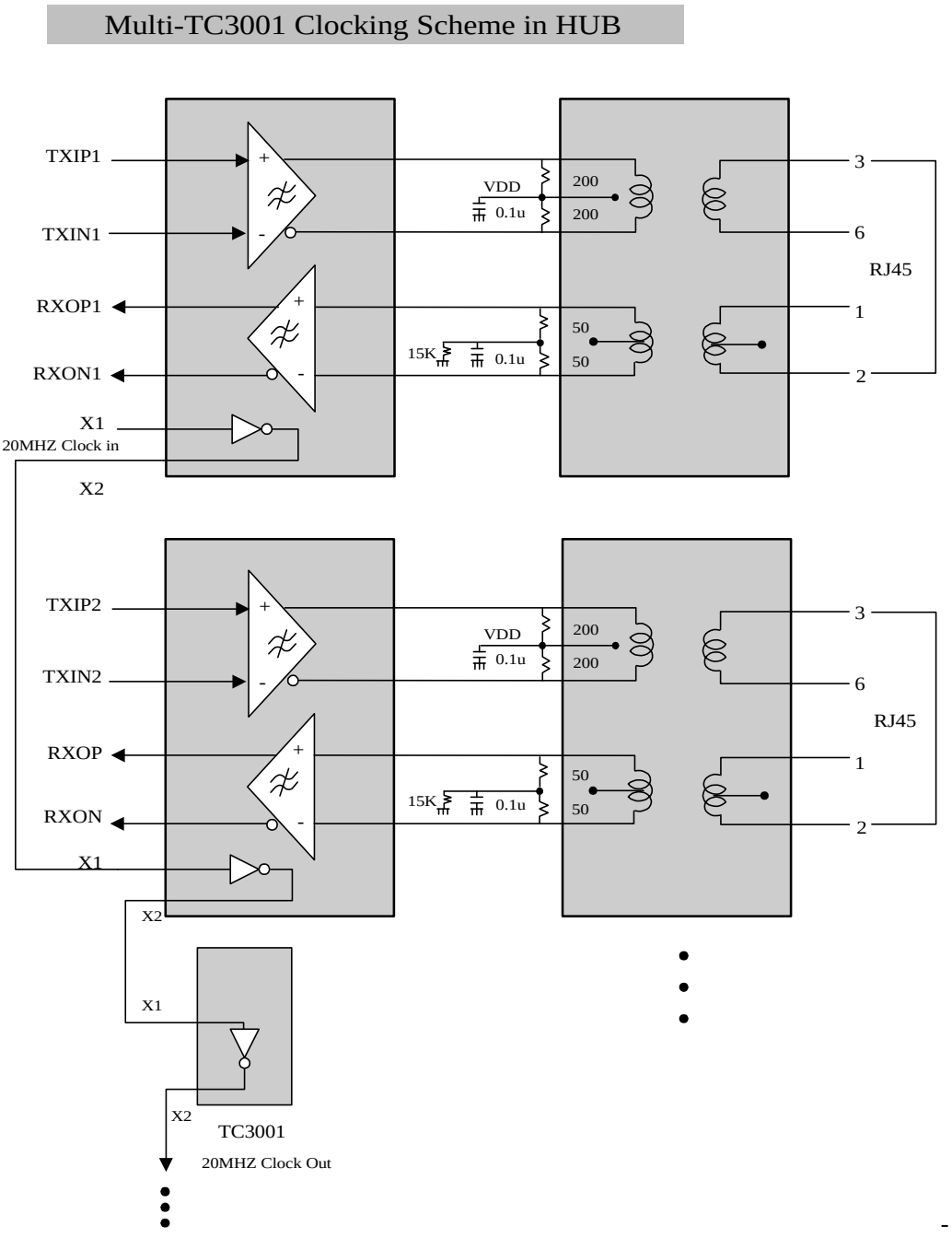
Basic configuration



6.1 Application Diagram (10BaseT Filter with Buffering and Disable Mode)

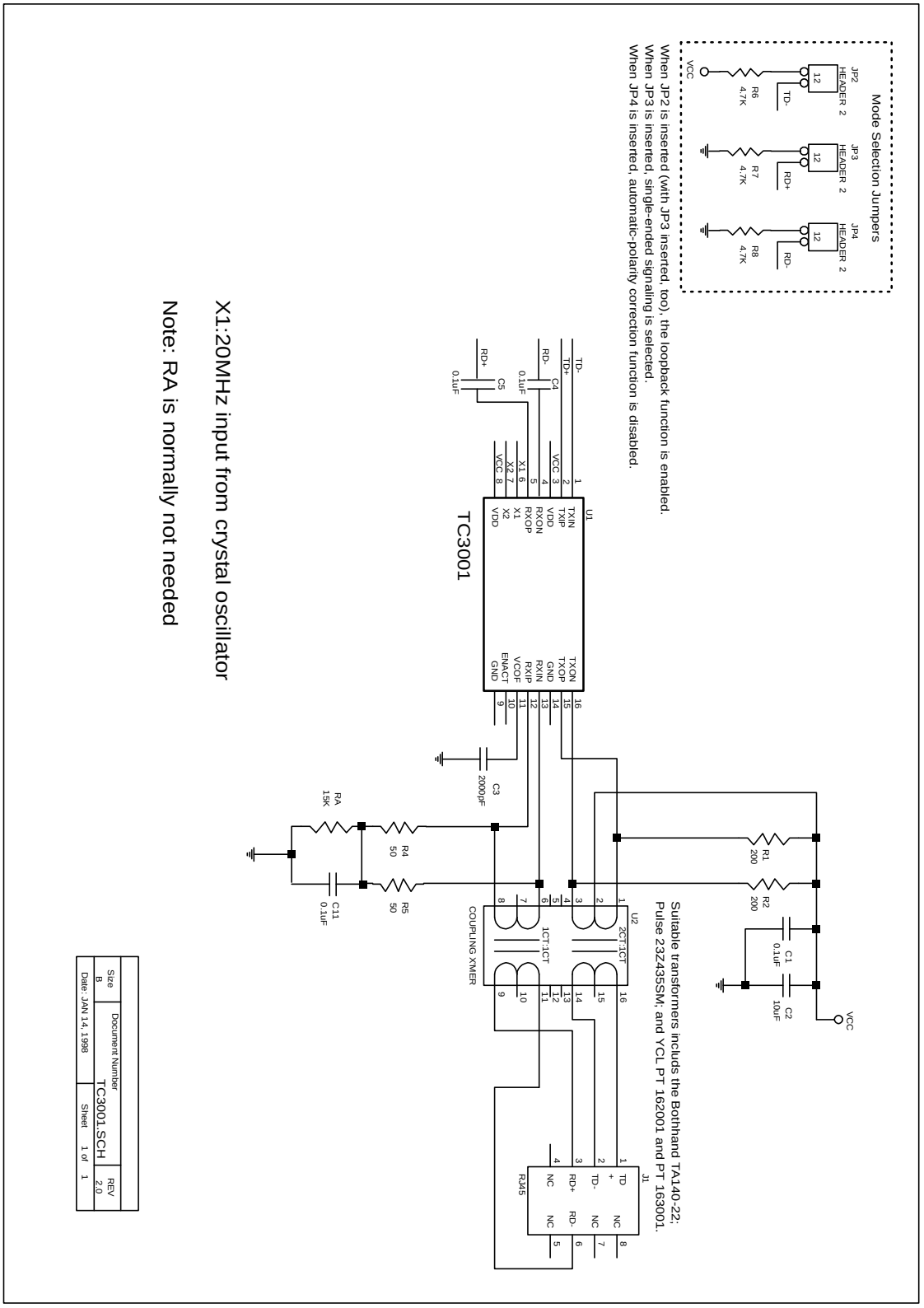


6.2 Application Diagram (10BaseT Filter with Buffering and Disable Mode)



Each TC3001 is connected in series through X1 in and X2 out to next one. This scheme enables the 20MHZ clock to "See" only one CMOS loading. The relative phases between TC3001's are not important. This clock is used for internal precision delay reference only.

6.3 Application Diagram



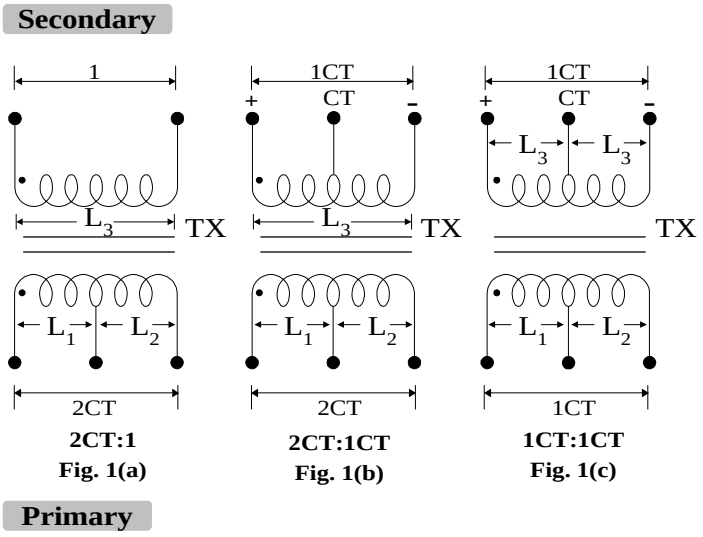
7. Isolation Transformer Specification / Manufacturers

Manufacturer	Part Number
Bothhand	TA140-22B(W/Choke)
PULSE	23Z435SM
YCL	PT162001(W/Choke), PT163001(W/Choke)

(All the Spec. of part number above are Transmit : 2CT:1CT, Receive : 1CT:1CT)

Specifications :

Turn Ratio	(Transmit)2CT:1or 2CT:1CT, or 1CT:1CT ; (Receive)1CT:1CT
Isolation	2000Vrms



Note:

Refer to Fig. 1(a) above, L1 = L2 = L3. Where L1 and L2 on the primary side, and L3 on the secondary side are used in TC3001. Therefore, Ratio L1 , L2 , L3 is refered to as 2CT:1.

Refer to Fig 1(b), with 2CT:1CT, use only +/- pin, and leave CT pin open. Or one can refer to Fig. 1(c) with 1CT:1CT, use + pin and CT pin , or use - pin and CT pin.

8. Oscillator Specification / Manufacturers

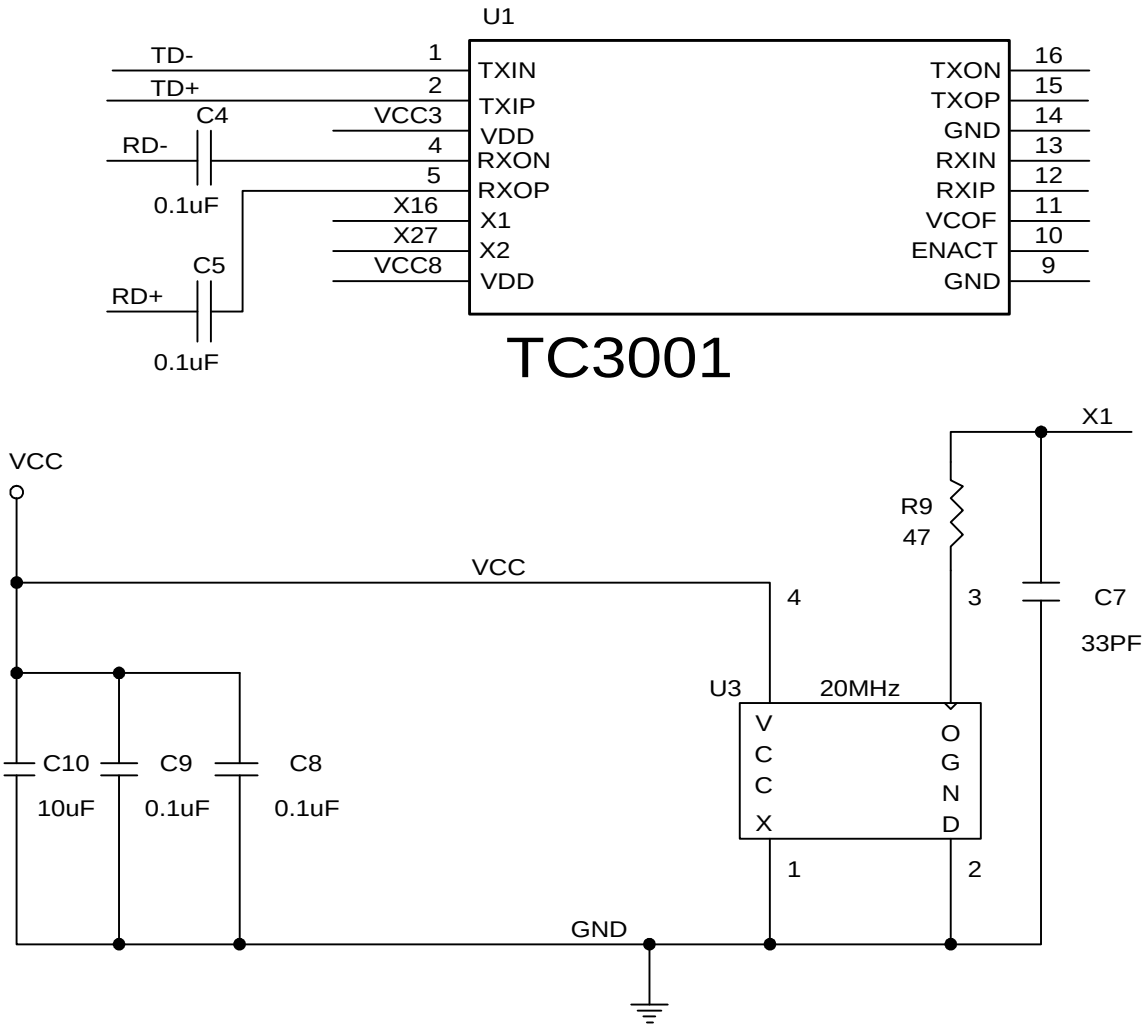
Recommended Manufacturer	Part Number
TXC	505NT
T&0	9502-C
USI	UC7-2A

Specifications :

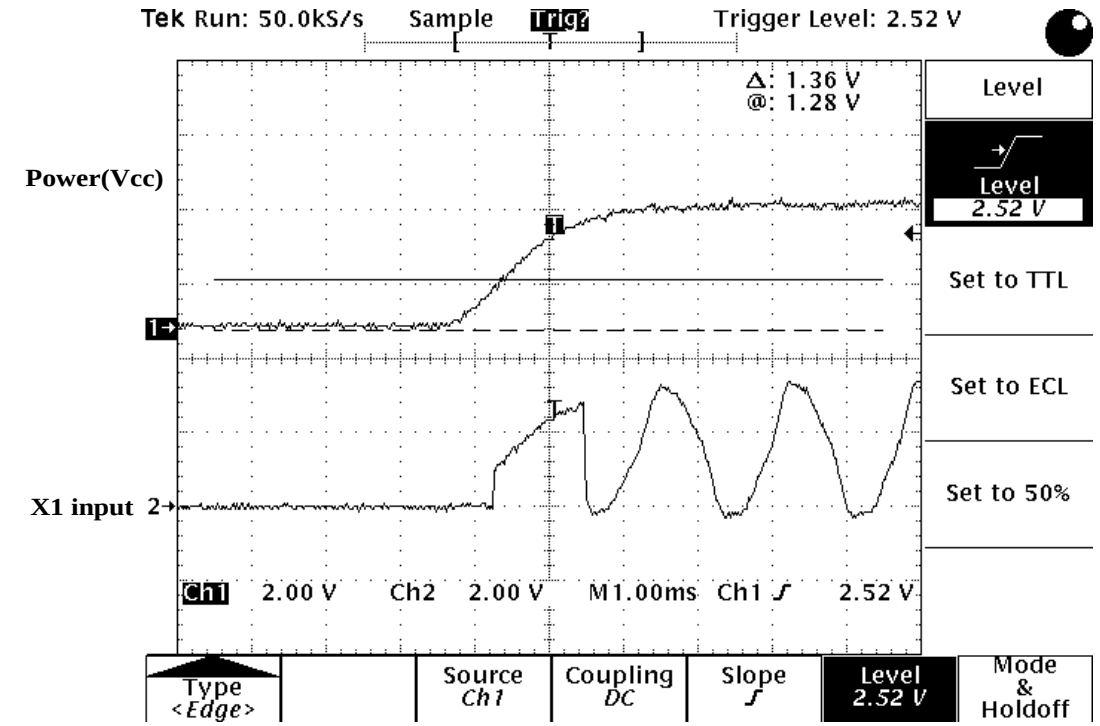
*** Stable Time**	600us Maximum	
Output Voltage Logic High (VoH)	CMOS Load	90% VDD Minimum
	TTL Load	2.4 VDD Minimum
Output voltage Logic Low (VoL)	CMOS Load	10% VDD Maximum
	TTL Load	0.4 VDD Maximum

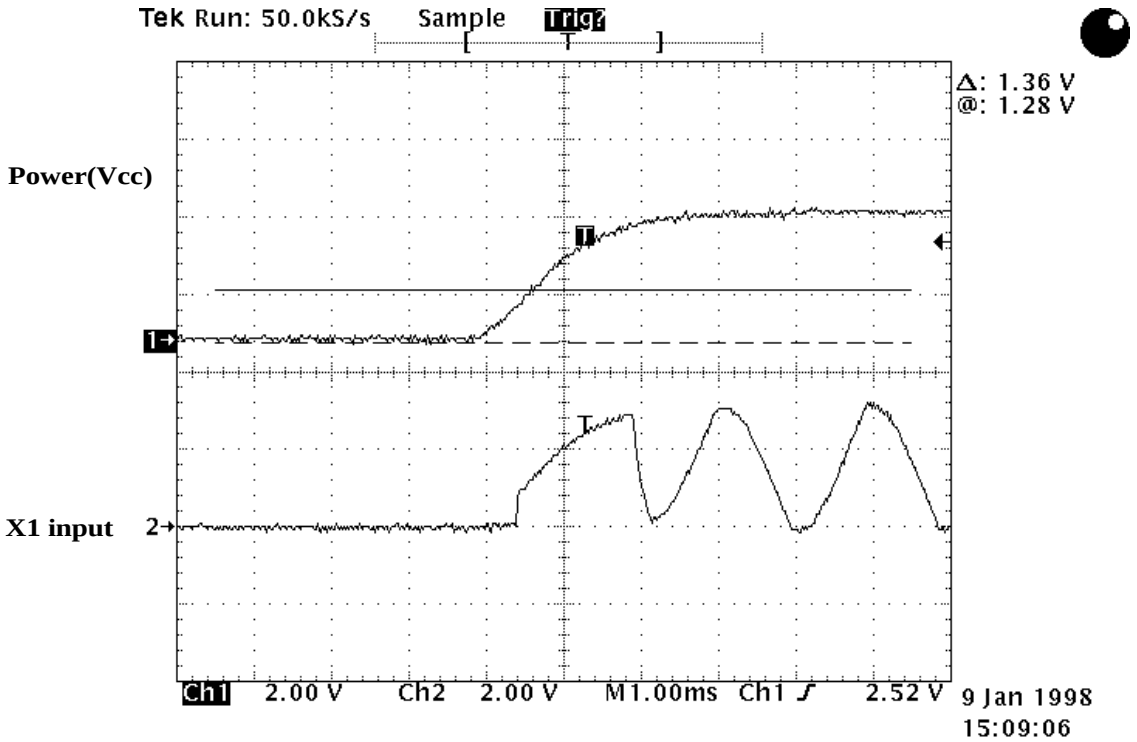
Note : The stable time is defined as the duration from power (VCC=5V) triggered point at 2.5V to the time the OSC. Coming out with stable CMOS load output waveform. Reference to circuits & waveform.

8.1 Osillator Specification / Manufacturers

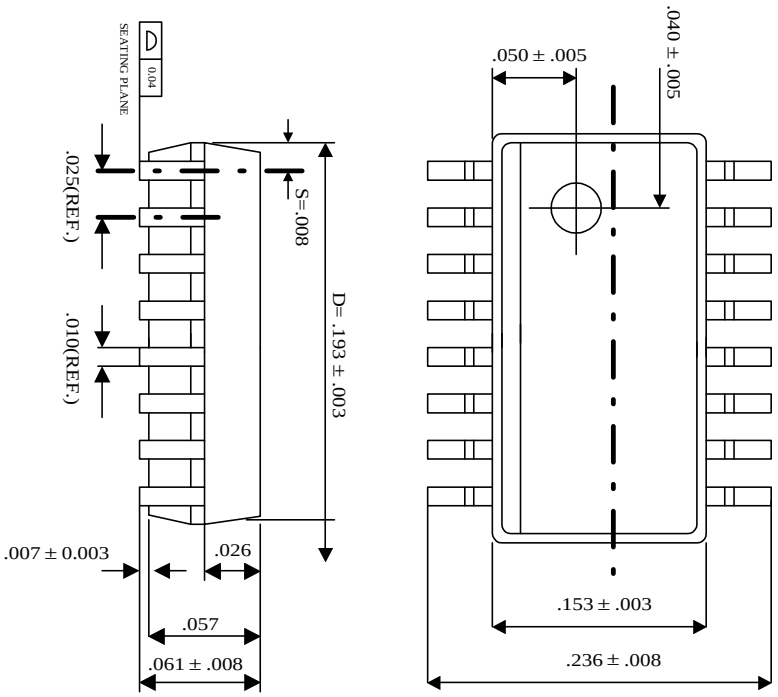


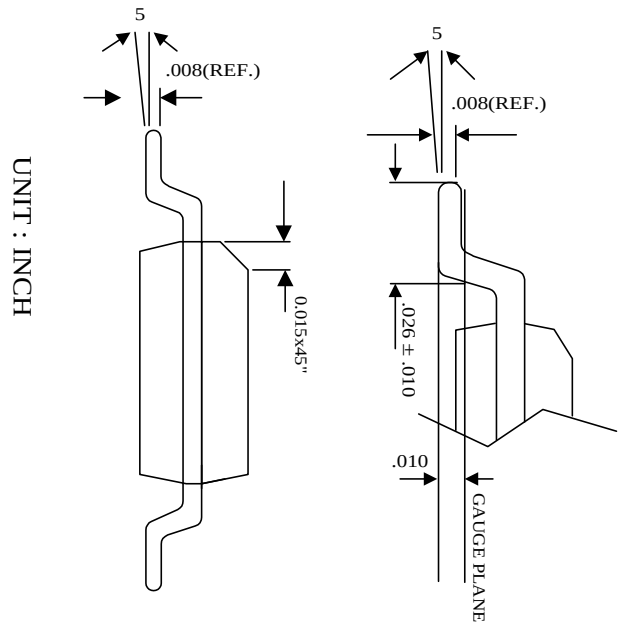
8.2 Oscillator Specification / Manufacturers





9. TC3001 Physical Dimension





UNIT : INCH

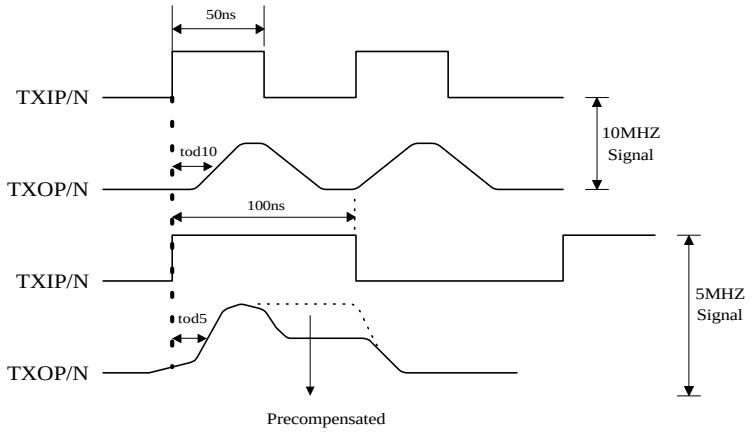
10. Absolute Maximum Ratings (Exceeding these values may cause permanent damage)

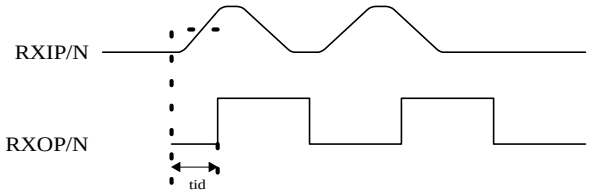
Voltage on Any Pin with Respect to Ground	-0.5V	to	7V
Storage Temperature	-40℃	to	125℃

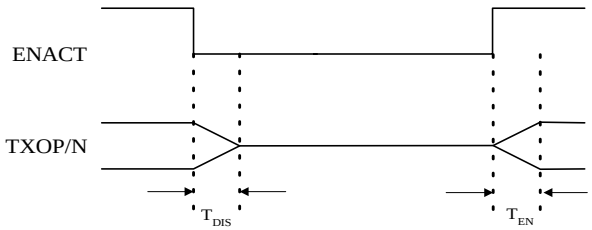
10.1 Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (VDD)	Vcc	4.75	5.0	5.25	V
Operating temperature	Top	0		70	℃

11. Switching Characteristics







Symbol	Parameter	Min.	Typ.	Max.	Unit
Tod10	Transmitter Filter Delay for 10MHZ			55	ns
Tod5	Transmitter Filter Delay for 5MHZ			55	ns
Tid	Receiver Filter Delay			300	ns
Tdis	TXOP / TXON Disable time			TBD*	ns
Ten	TXOP / TXON Enable time			TBD*	ns

* To be determined

Receiver Filter Specification

The receiver, while in the idle state, shall reject as RXIP/RXIN input the following signals:

1. A RXIP/RXIN signal consisting of a continuous 1 MHz sine wave with a peak amplitude of 299 mV when measured across a 121Ω resistive load.
2. A RXIP/RXIN signal consisting of a continuous 5 MHz sine wave with a peak amplitude of 299 mV when measured across a 121Ω resistive load.
3. A RXIP/RXIN signal consisting of a continuous 10 MHz sine wave with a peak amplitude of 312 mV when measured across a 121Ω resistive load.
4. A RXIP/RXIN signal consisting of a continuous 15 MHz sine wave with a peak amplitude of 423 mV when measured across a 121Ω resistive load.
5. A RXIP/RXIN signal consisting of a continuous 20 MHz sine wave with a peak amplitude of 769 mV when measured across a 121Ω resistive load.
6. A RXIP/RXIN signal consisting of a continuous 25 MHz sine wave with a peak amplitude of 1.416 V when measured across a 121Ω resistive load.
7. A RXIP/RXIN signal consisting of a continuous 30 MHz sine wave with a peak amplitude of 2.411 V when measured across a 121Ω resistive load.
8. A RXIP/RXIN signal consisting of a continuous 0.5 MHz sine wave with a peak-to-peak amplitude of 6.1 V.
9. A RXIP/RXIN signal consisting of a continuous 1 MHz sine wave with a peak-to-peak amplitude of 6.1 V.
10. A RXIP/RXIN signal consisting of a continuous 1.9 MHz sine wave with a peak-to-peak amplitude of 6.1 V.
11. A RXIP/RXIN signal consisting of a single cycle 2 MHz sine wave with a peak-to-peak amplitude of 6.1 V preceded and followed by 4 BT of silence.
12. A RXIP/RXIN signal consisting of a single cycle 5 MHz sine wave with a peak-to-peak amplitude of 6.1 V preceded and followed by 4 BT of silence.
13. A RXIP/RXIN signal consisting of a single cycle 10 MHz sine wave with a peak-to-peak amplitude of 6.1 V preceded and followed by 4 BT of silence.
14. A RXIP/RXIN signal consisting of a single cycle 15 MHz sine wave with a peak-to-peak amplitude of 6.1 V preceded and followed by 4 BT of silence.

12. Electrical Characteristics

(TA = 0-70°C, VDD = 5V ± 5%, GND = 0.0V, unless otherwise specified)

D.C. CHARACTERISTICS

Parameter	Signals (TTL Levels)	Min.	Typ.	Max.	Unit	Conditions
VIL	ENACT, TXIP/TXIN			0.8V	V	VDD=5V
VIH	ENACT, TXIP/TXIN	2.0			V	VDD=5V
VOL	RXON/RXOP			0.4	V	IOL=8mA
VOH	RXON/RXOP	2.4			V	IOH=4mA
IIL	ENACT, TXIP/TXIN			5	uA	VIN=1.0V
IIH	ENACT, TXIP/TXIN			43	uA	VIN=VDD
IOZ	TXON/TXOP		0.16		uA	ENACT=0.0V
IDD(idle) Without 20MHz CLK		2		5	mA	VDD=5V
IDD(idle) With 20MHz CLK			11		mA	VDD=5V Load=100Ω at TXOP/TXON
IDD(active)				75	mA	VDD=5V Load=100Ω at TXOP/TXON Frame Gap=9.6uS
X2 fan out				80	pf	VDD=5V

TWISTED PAIR INTERFACE CHARACTERISFICS

Parameter	Signals (TTL Levels)	Min.	Typ.	Max.	Unit	Conditions
VRXI	RXIP/RXIN Differential Input Voltage	0.4			Vpk	VDD=5V 5MHz Signal Input
VTXO	TXOP/TXON Differential Output Voltage	2.3		2.9	Vpk	VDD=5V

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