# SRAM

# 32K X 8 LOW POWER CMOS STATIC RAM

## FEATURES

ßbHigh speed access time: 12/15ns

ßbLow power supply current :

- Operating : 90mA(max)
- Standby : 10uA

ßbPower supply : +5V (± 10%)

ßbFully static operation – No clock or refreshing required

ßbAll inputs and outputs directly LVTTL compatible

ßbCommon I/O capability

ßbData retention voltage : 1.5V (min)

ßbAvailable packages :28-pin SOJ, SOP, TSOP-I (8x13.4mm forward type and reverse type).

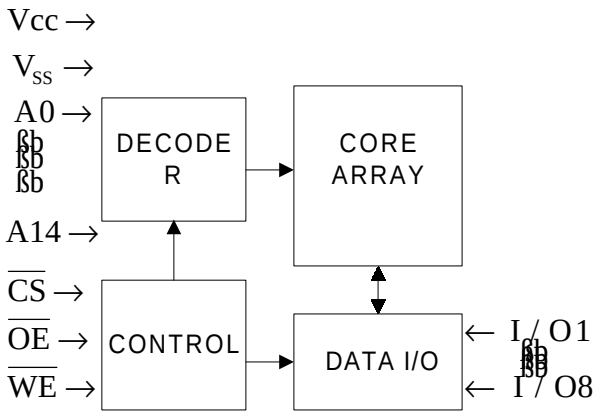
## PART NUMBER EXAMPLES

| | PACKAGE | SPEED |
|---|---|---|
| T15M256C-12J | SOJ | 12ns |
| T15M256C-12D | SOP | 12ns |
| T15M256C-15P | TSOP-I(Forward) | 15ns |
| T15M256C-15R | TSOP-I(Reverse) | 15ns |

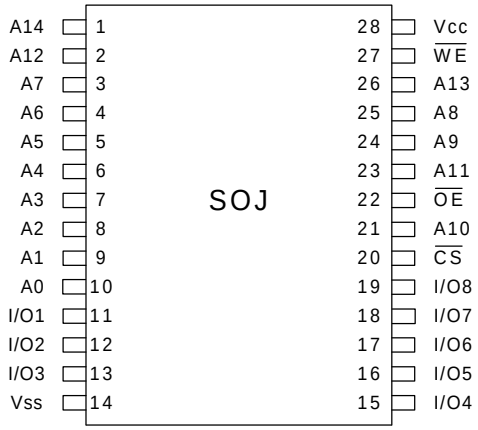
## GENERAL DESCRIPTION

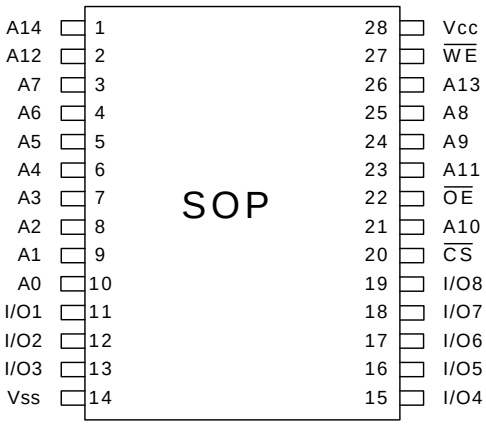
The T15M256C is a low power CMOS static RAM. organized as 32,768 x 8 bits that operates on a single +5-volt power supply. Low operating and standby current . Data retention is guaranteed at a power supply voltage as low as 1.5V. This device is packaged in a standard 28-pin SOJ, SOP, TSOP-I forward and reverse type.

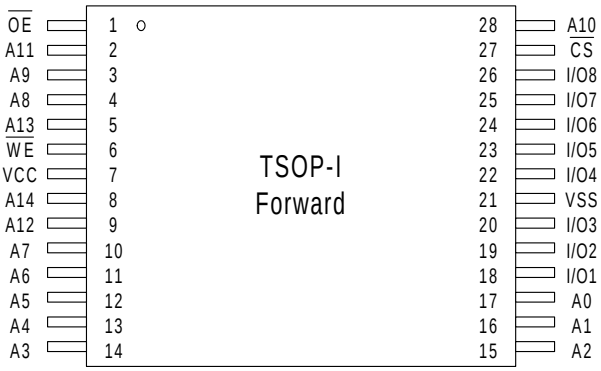
## BLOCK DIAGRAM

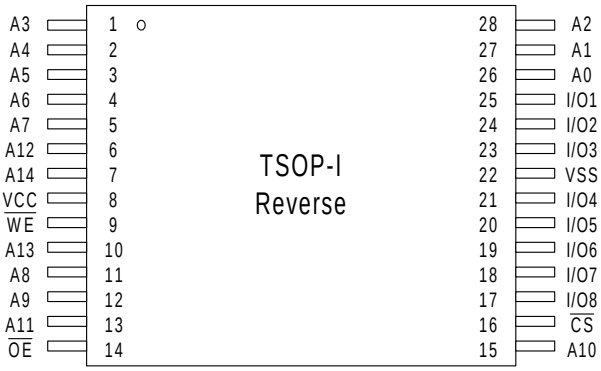


## PIN CONFIGURATION




## PIN DESCRIPTION

| SYMBOL | DESCRIPTION |
|---|---|
| A0 - A14 | Address Inputs |
| I/O1 - I/O8 | Data Inputs/Outputs |
| $\overline{CS}$ | Chip Select Inputs |
| $\overline{WE}$ | Write Enable |
| $\overline{OE}$ | Output Enable |
| Vcc | Power Supply |
| Vss | Ground |

## DC CHARACTERISTICS ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
|---|---|---|
| Supply Voltage to Vss Potential | -0.5 to + 7V | V |
| Inputs to Vss Potential | -0.5 to Vcc +0.5 | V |
| Power Dissipation | 0.7 | W |
| Storage Temperature | -60 to +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYM | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Supply Voltage | Vcc | 4.5 | 5 | 5.5 | V |
| Input Voltage, low | $V_{IL}$ | -0.3 | - | 0.8 | V |
| Input Voltage, high | $V_{IH}$ | 2.2 | - | Vcc+0.3 | V |
| Ambient Temperature | $T_A$ | -40 | - | 85 | °C |

## TRUTH TABLE

| $\overline{CS}$ | $\overline{OE}$ | $\overline{WE}$ | MODE | I/O1- I/O8 | Power |
|---|---|---|---|---|---|
| H | X | X | Not Selected | High-Z | Standby |
| L | H | H | Output Disable | High-Z | Active |
| L | L | H | Read | Data Out | Active |
| L | X | L | Write | Data In | Active |

## OPERATING CHARACTERISTICS

(Vcc = +5V / ± 10%, Vss = 0V, Ta = -40 to 85°C)

| PARAMETER | SYM. | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{LI}$ | Vin=Vss to Vcc | | - | - | 1 | μA |
| Output Leakage Current | $I_{LO}$ | $V_{I/O}$=Vss to Vcc , $\overline{CS}$ = $V_{IH}$ or $\overline{OE}$ = $V_{IH}$ or $\overline{WE}$ = $V_{IL}$ | | - | - | 1 | μA |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = + 2.1mA | | - | - | 0.4 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = - 1.0mA | | 2.4 | - | - | V |
| Operating Power Supply Current | Icc | $\overline{CS}$ = $V_{IL}$, I/O=0mA Cycle = MIN. Duty = 100% | -12 | - | - | 90 | mA |
| | | | -15 | - | - | 75 | mA |
| Standby Power Supply Current | $I_{SB}$ | $\overline{CS}$ = $V_{IH}$, Cycle=min, Duty=100% | | - | - | 0.3 | mA |
| | $I_{SB1}$ | $\overline{CS}$ ≥ $V_{CC}$-0.2V | | - | - | 10 | uA |

## CAPACITANCE

(Vcc = +5V / ± 10%, Ta = 25°C, f = 1 MHz)

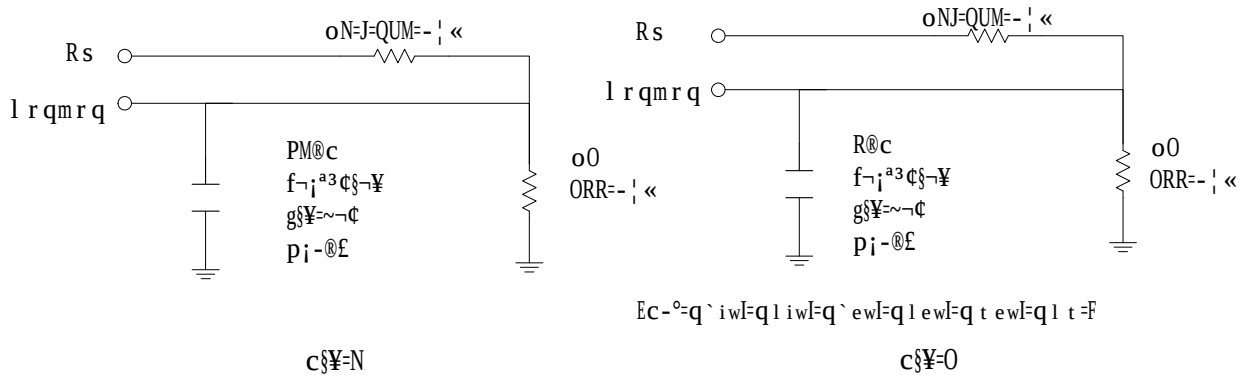
| PARAMETER | SYMBOL | CONDITION | MAX. | UNIT |
|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | $V_{IN}$ = 0V | 6 | pF |
| Input/ Output Capacitance | $C_{I/O}$ | $V_{OUT}$ = 0V | 8 | pF |

**Note:** These parameters are sampled but not 100% tested.

## AC TEST CONDITIONS

| PARAMETER | CONDITIONS |
|---|---|
| Input Pulse Levels | 0V to 3V |
| Input Rise and Fall Times | 3 ns |
| Input and Output Timing Reference Level | 1.5V |
| Output Load | See Fig. 1,2 |

## AC TEST LOADS AND WAVEFORM




c§¥=N c§¥=0

## AC CHARACTERISTICS

($V_{CC}$= +5V / ± 10%, Vss = 0V, Ta = -40 to 85°C)

### (1) READ CYCLE

| PARAMETER | SYM. | -12ns | | -15ns | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | |
| Read Cycle Time | tRC | 12 | àµ | 15 | àµ | ns |
| Address Access Time | tAA | àµ | 12 | àµ | 15 | ns |
| Chip Select Access Time | tACS | àµ | 12 | àµ | 15 | ns |
| Output Enable to Output Valid | tAOE | àµ | 7 | àµ | 7 | ns |
| Chip Selection to Output in Low Z | tCLZ* | 3 | àµ | 3 | àµ | ns |
| Output Enable to Output in Low Z | tOLZ* | 0 | àµ | 0 | àµ | ns |
| Chip Deselection to Output in High Z | tCHZ* | 0 | 6 | 0 | 7 | ns |
| Output Disable to Output in High Z | tOHZ* | 0 | 6 | 0 | 7 | ns |
| Output Hold from Address Change | tOH | 3 | àµ | 3 | àµ | ns |

* These parameters is measured with 30pF test load.

### (2) WRITE CYCLE

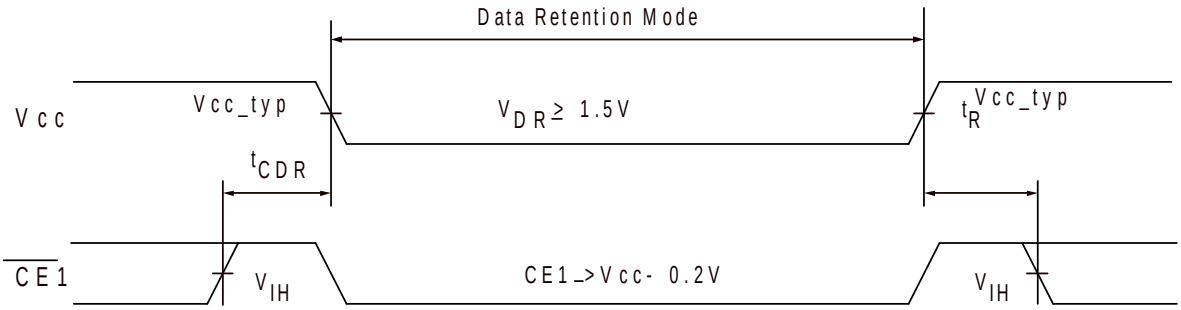
| PARAMETER | SYM. | -12ns | | -15ns | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | |
| Write Cycle Time | tWC | 12 | àµ | 15 | àµ | ns |
| Chip Selection to End of Write | tCW | 10 | àµ | 11 | àµ | ns |
| Address Valid to End of Write | tAW | 10 | àµ | 11 | àµ | ns |
| Address Setup Time | tAS | 0 | àµ | 0 | àµ | ns |
| Write Pulse Width | tWP | 10 | àµ | 11 | àµ | ns |
| Write Recovery Time | tWR | 0 | àµ | 0 | àµ | ns |
| Data Valid to End of Write | tDW | 8 | àµ | 8 | àµ | ns |
| Data Hold from End of Write | tDH | 0 | àµ | 0 | àµ | ns |
| Write to Output in High Z | tWHZ* | àµ | 6 | àµ | 6 | ns |
| Output Active from End of Write | tOW | 0 | àµ | 0 | àµ | ns |

* These parameters is measured with 30pF test load.

## DATA RETENTION CHARACTERISTICS

| Item | Symbol | Test Condition | Min | Typ | max | unit |
|---|---|---|---|---|---|---|
| Vcc for data retention | $V_{DR}$ | $\overline{CS} \geq V_{cc}$-0.2V | 1.5 | - | - | V |
| Data retention current | $I_{DR}$ | $V_{cc}$=3.0, $\overline{CS} \geq V_{cc}$-0.2V | - | | 10 | uA |
| Data retention set-up time | $t_{CDR}$ | See data retention waveform | 0 | - | - | ms |
| Recovery time | $t_R$ | | 5 | - | - | |

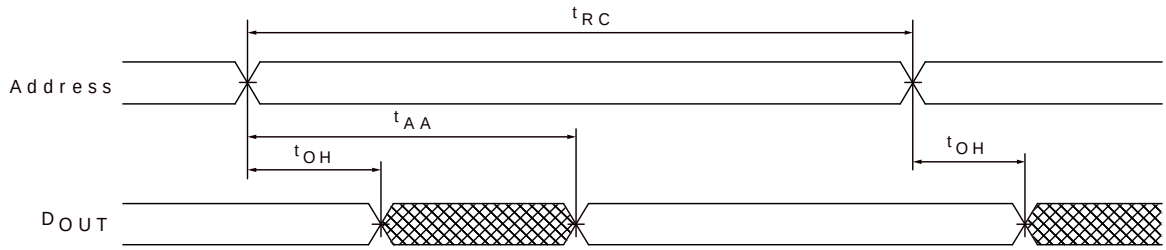
## DATA RETENTION WAVE FORM



## TIMING WAVEFORMS

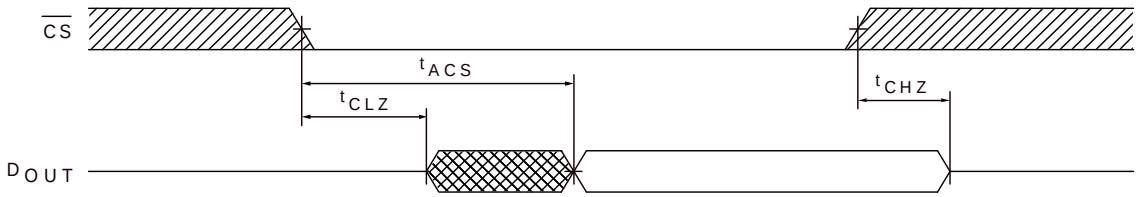
### READ CYCLE 1

(Address Controlled)



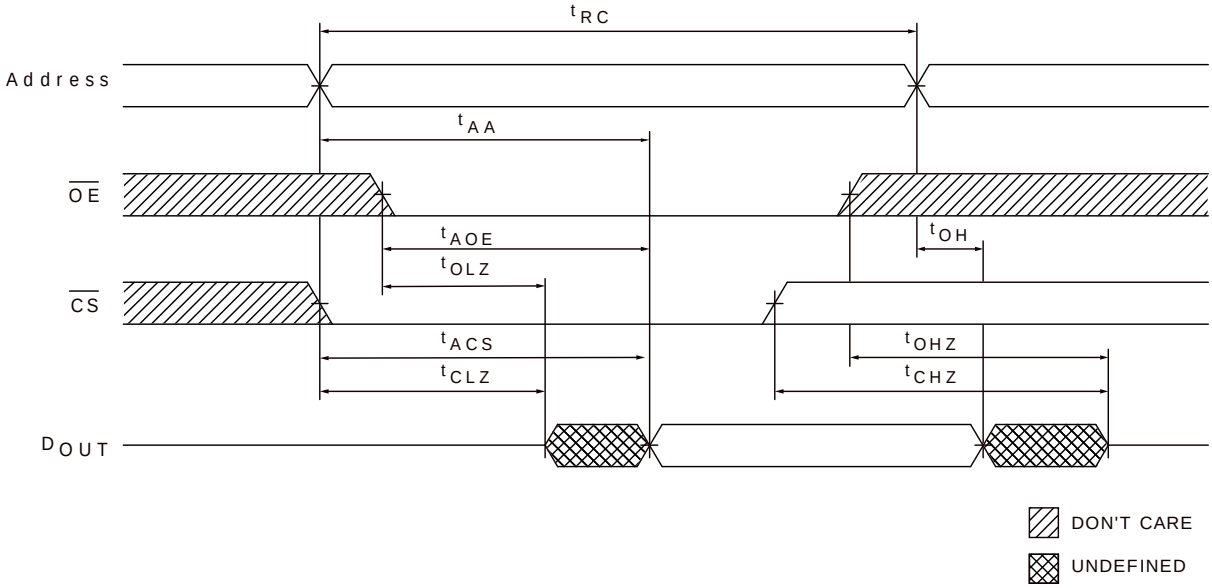

### READ CYCLE 2

(Chip Select Controlled)

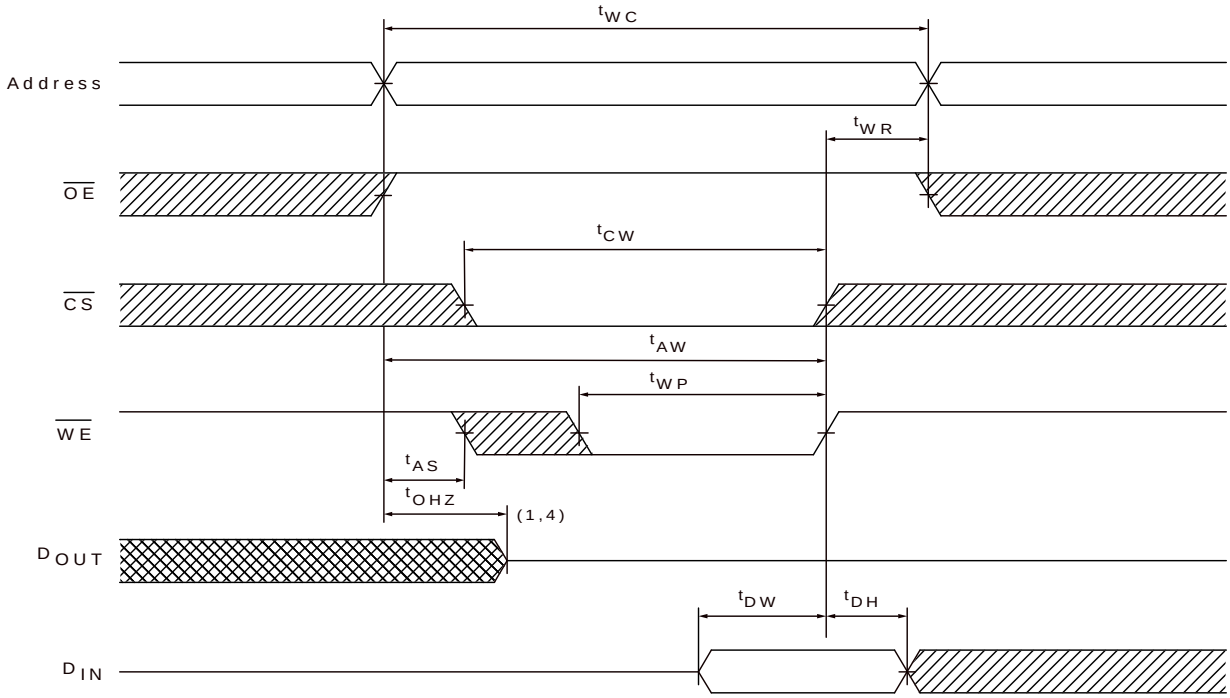



### READ CYCLE 3

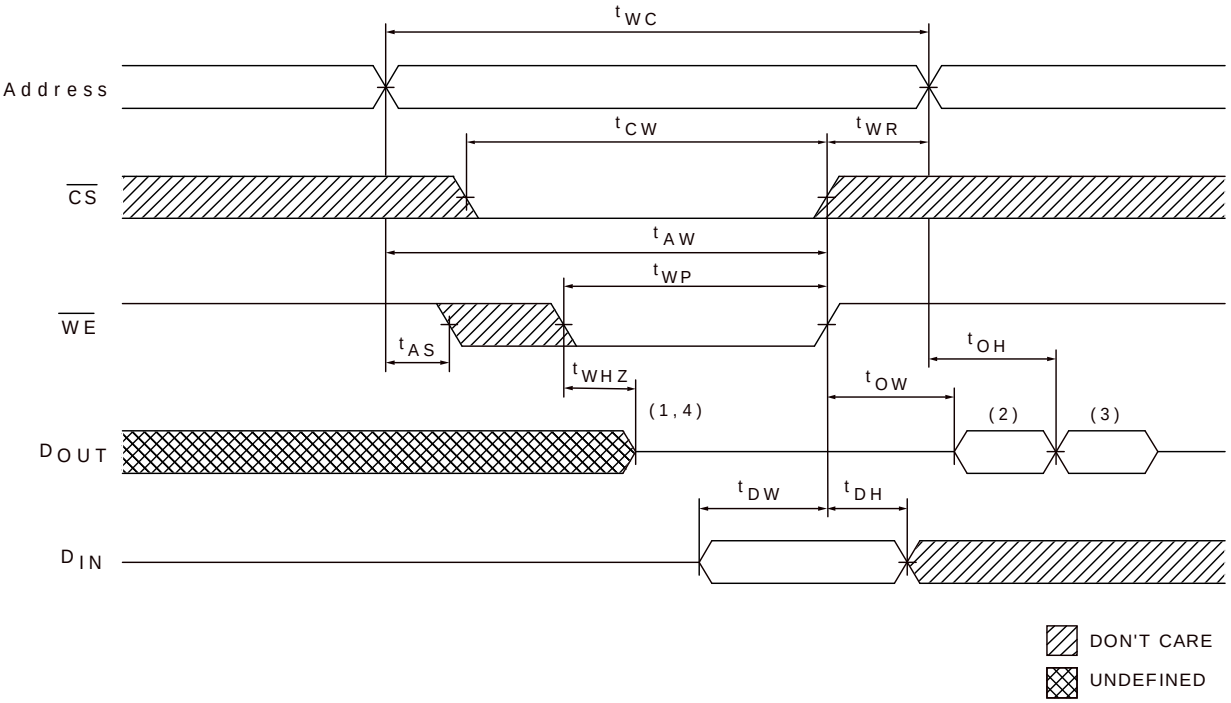
(Output Enable Controlled)



## WRITE CYCLE 1 ($\overline{OE}$ CLOCK)




## WRITE CYCLE 2 ($\overline{OE}$ = $V_{IL}$ Fixed)

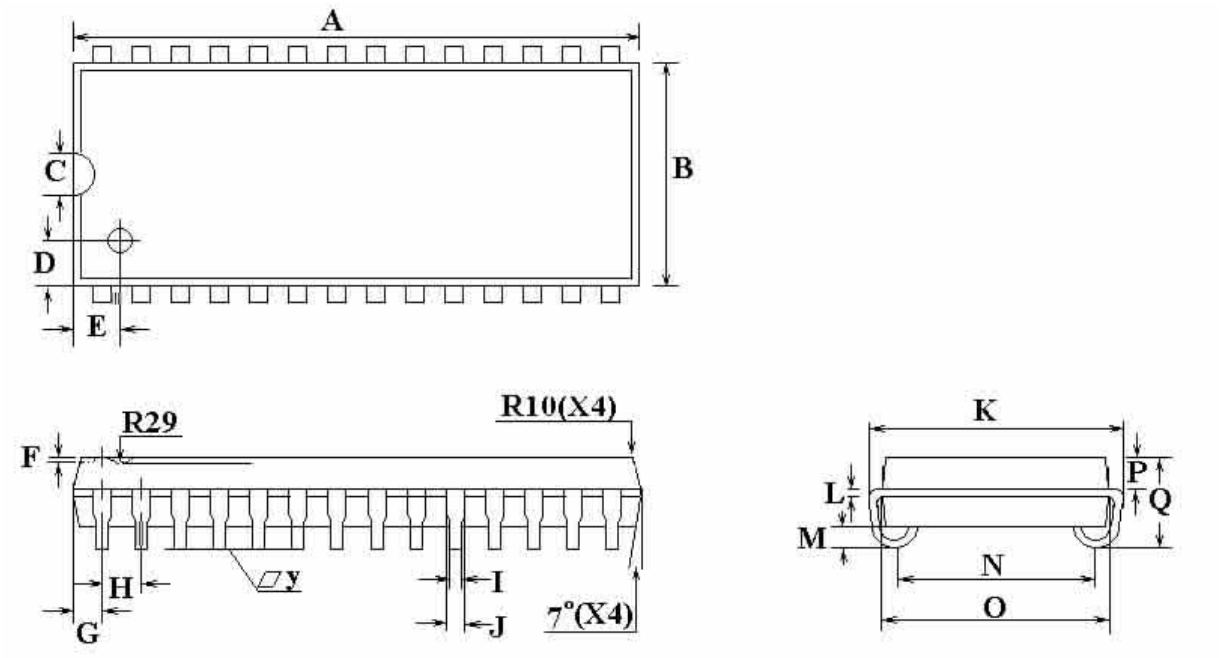


Notes: 1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.

2. The data output from $D_{OUT}$ are the same as the data written to $D_{IN}$ during the write cycle.
3. $D_{OUT}$ provides the read data for the next address.
4. Transition is measured ± 500 mV from steady state with $C_L$ = 5pF. This parameter is guaranteed but not 100% tested.
5. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of $t_{WP}$ or ($t_{WHZ}$ + $t_{DW}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required $t_{DW}$. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified $t_{WP}$.

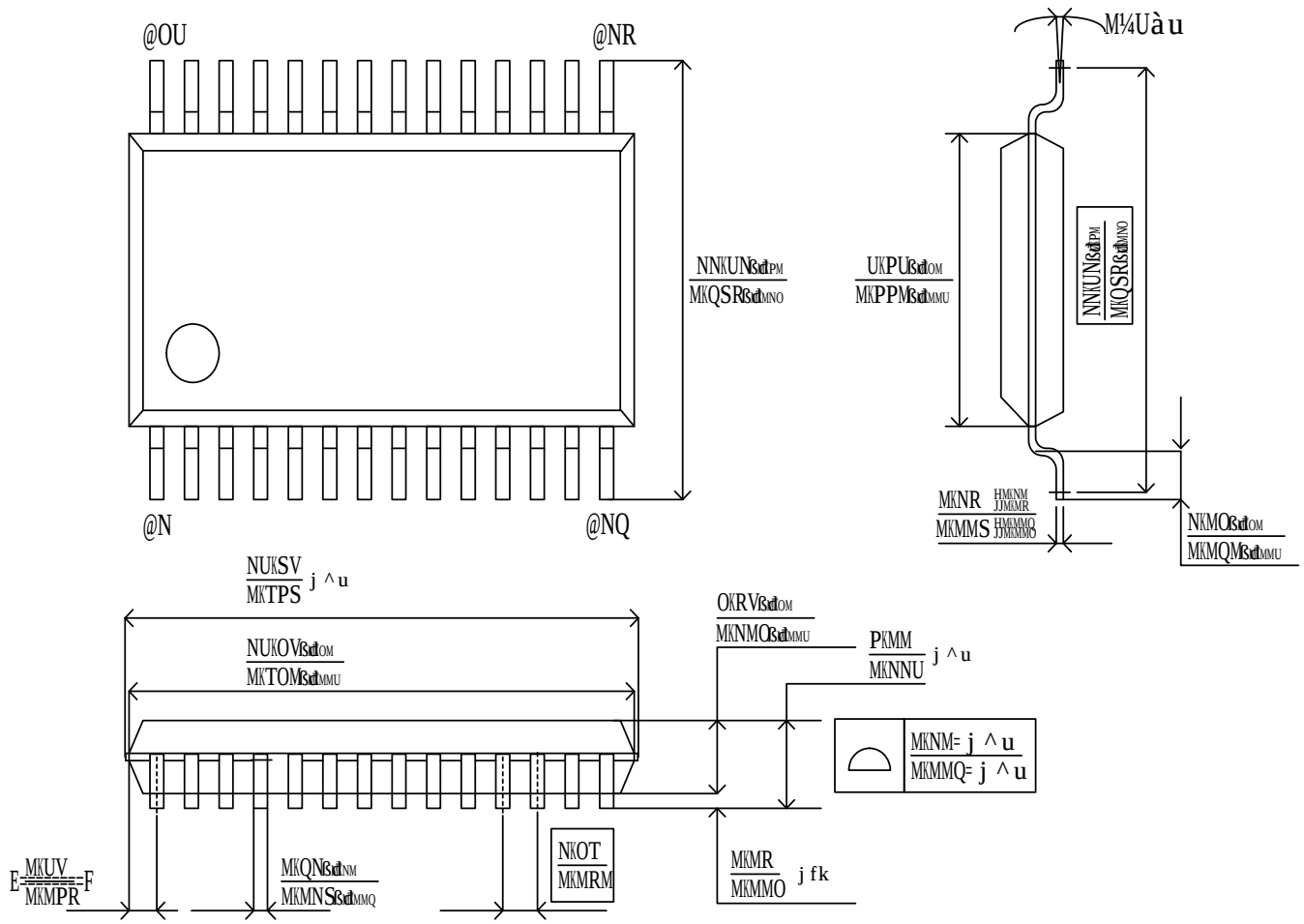
## PACKAGE DIMENSIONS

## 28-LEAD SOJ SRAM (300 mil)

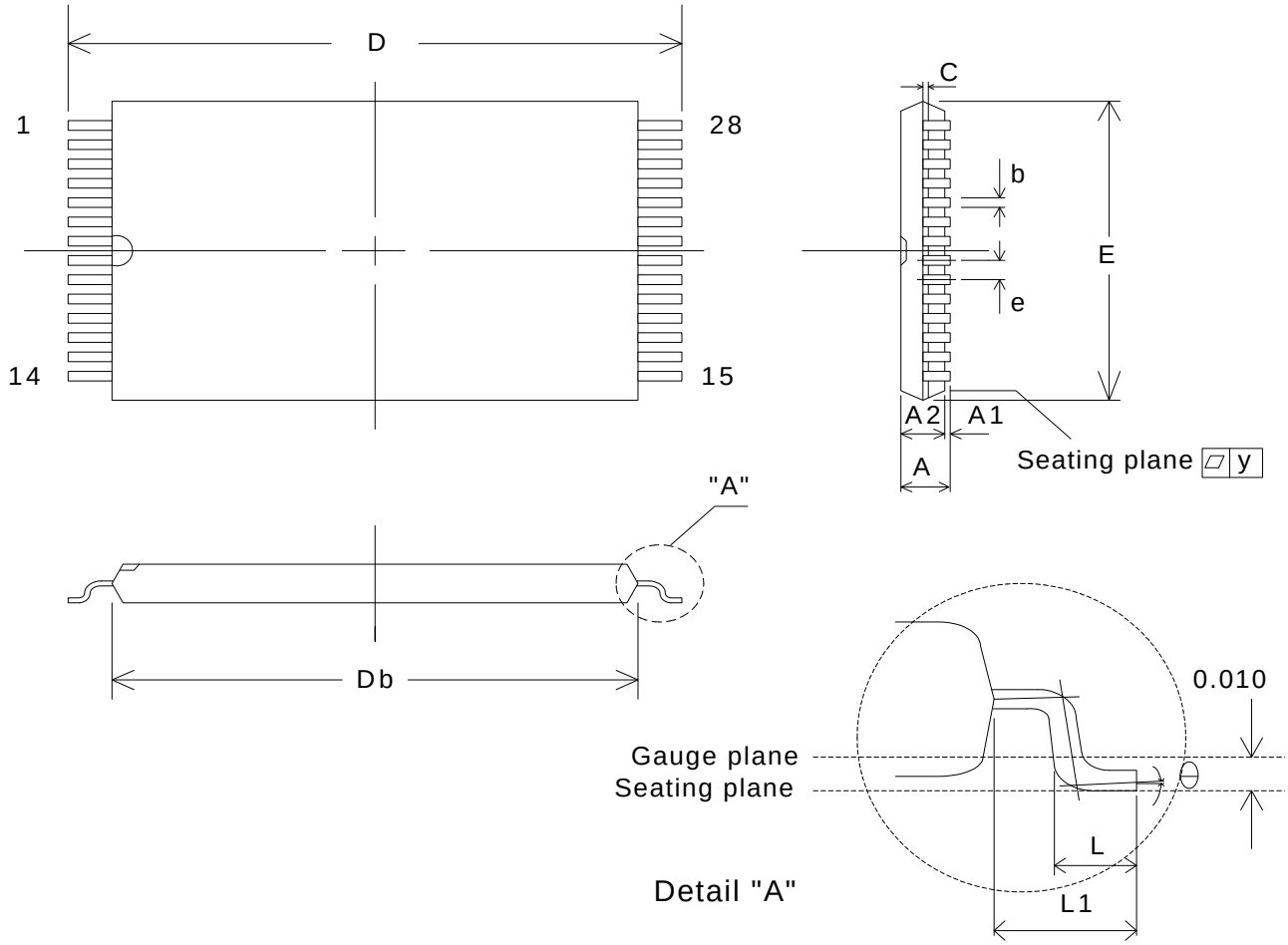



| SYMBOL | DIMENSIONS IN INCHES | DIMENSIONS IN MM |
|---|---|---|
| A | 0.710±0.002 | 18.03±0.05 |
| B | 0.336±0.003 | 8.53±0.08 |
| C | 0.060±0.002 | 1.52±0.05 |
| D | 0.050±0.001 | 1.27±0.03 |
| E | 0.063±0.001 | 1.63±0.03 |
| F | 0.015±0.002 | 0.38±0.05 |
| G | 0.030±0.002 | 0.76±0.05 |
| H | 0.050±0.002 | 1.27±0.05 |
| I | 0.018±0.002 | 0.46±0.05 |
| J | 0.028±0.002 | 0.71±0.05 |
| K | 0.337±0.002 | 8.56±0.05 |
| L | 0.010±0.001 | 0.25±0.03 |
| M | 0.026±0.002 | 0.66±0.05 |
| N | 0.268±0.003 | 6.81±0.08 |
| O | 0.300±0.002 | 7.62±0.05 |
| P | 0.053±0.001 | 1.35±0.03 |
| Q | 0.140±0.004 | 3.56±0.10 |
| y | 0.004(MAX) | 0.10(MAX) |

## PACKAGE DIMENSIONS
## 28-LEAD SOP



## PACKAGE DIMENSIONS
## 28-LEAD TSOP-I FORWARD AND REVERSE (8X13.4mm)




| SYMBOL | DIMENSIONS IN INCHES | DIMENSIONS IN MM |
|---|---|---|
| A | 0.047(max.) | 1.20(max.) |
| A1 | 0.004ßđ0.002 | 0.10ßđ0.05 |
| A2 | 0.039ßđ0.002 | 1.00ßđ0.05 |
| b | 0.008(typ.) | 0.20(typ.) |
| c | 0.006(typ.) | 0.15(typ.) |
| Db | 0.465ßđ0.004 | 11.80ßđ0.10 |
| E | 0.315ßđ0.004 | 8.00ßđ0.10 |
| e | 0.022(typ.) | 0.55(typ.) |
| D | 0.528ßđ0.008 | 13.40ßđ0.20 |
| L | 0.020ßđ0.004 | 0.50ßđ0.10 |
| L1 | 0.0315ßđ0.004 | 0.80ßđ0.10 |
| y | 0.004(max.) | 0.10(max.) |
| áh | 0àu~5àu | 0àu~5àu |