Supertex inc.

TN0104
Low Threshold

N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
				TO-92	TO-243AA*
40V	1.8Ω	1.6V	2.0A	TN0104N3	—
40V	2.0Ω	1.6V	2.0A	—	TN0104N8

* Same as SOT-89. Product supplied on 2000 piece carrier tape reels.

Product marking for TO-243AA:

TN1L❋

Where ❋ = 2-week alpha date code

Features

- ❏ Low threshold —1.6V max.
- ❏ High input impedance
- ❏ Low input capacitance
- ❏ Fast switching speeds
- ❏ Low on resistance
- ❏ Free from secondary breakdown
- ❏ Low input and output leakage
- ❏ Complementary N- and P-channel devices

Applications

- ❏ Logic level interfaces – ideal for TTL and CMOS
- ❏ Solid state relays
- ❏ Battery operated systems
- ❏ Photo voltaic drives
- ❏ Analog switches
- ❏ General purpose line drivers
- ❏ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

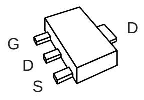
* For and TO-92, distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

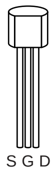
These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-243AA
(SOT-89)



TO-92

Note: See Package Outline section for dimensions.

01/06/03

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-92	450mA	2.40A	1.0W	125	170	450mA	2.40A
TO-243AA	630mA	2.90A	1.6W†	15	78†	630mA	2.90A

* I_D (continuous) is limited by max rated T_j.
† $T_A = 25°C$. Mounted on FR5 Board, 25mm x 25mm x 1.57mm. Signficant P_D increase possible on ceramic substrate.

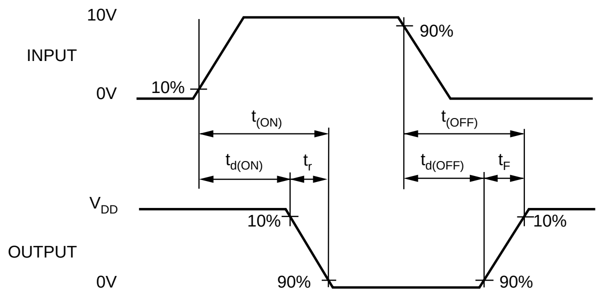
Electrical Characteristics (@ 25°C unless otherwise specified)

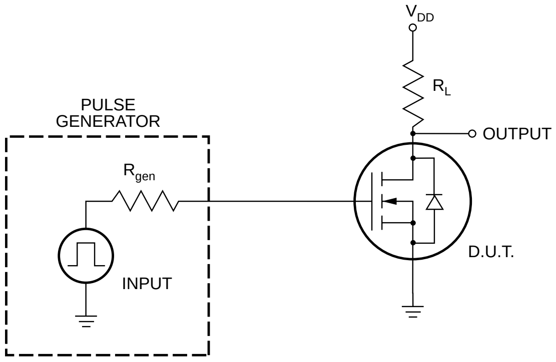
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage		40			V	$V_{GS}= 0V$, $I_D = 1.0mA$
$V_{GS(th)}$	Gate Threshold Voltage		0.6		1.6	V	$V_{GS} = V_{DS}$, $I_D = 500\mu A$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.8	-5.0	mV/°C	$V_{GS} = V_{DS}$, $I_D = 1.0mA$
I_{GSS}	Gate Body Leakage			0.1	100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current				1	µA	$V_{GS} = 0V$, V_{DS} = Max Rating
					100	µA	$V_{GS} = 0V$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current			0.35		A	$V_{GS} = 3V$, $V_{DS} = 20V$
			0.5	1.1			$V_{GS} = 5V$, $V_{DS} = 20V$
			2.0	2.6			$V_{GS} = 10V$, $V_{DS} = 20V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance	All Packages		5.0		Ω	$V_{GS} = 3V$, $I_D = 50mA$
				2.3	2.5		$V_{GS} = 5V$, $I_D = 250mA$
		TO-92		1.5	1.8		$V_{GS} = 10V$, $I_D = 1A$
		TO-243AA			2.0		$V_{GS} = 10V$, $I_D = 1A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.7	1.0	%/°C	$V_{GS} = 10V$, $I_D = 1A$,
G_{FS}	Forward Transconductance		0.34	0.45		℧	$V_{DS} = 20V$, $I_D = 0.5A$
C_{ISS}	Input Capacitance				70	pF	$V_{GS} = 0V$, $V_{DS} = 20V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance				50		
C_{RSS}	Reverse Transfer Capacitance				15		
$t_{d(ON)}$	Turn-ON Delay Time			3.0	5.0	ns	$V_{DD} = 20V$, $I_D = 1A$ $R_{GEN} = 25\Omega$
t_r	Rise Time			7.0	8.0		
$t_{d(OFF)}$	Turn-OFF Delay Time			6.0	9.0		
t_f	Fall Time			5.0	8.0		
V_{SD}	Diode Forward Voltage Drop	TO-92		1.2	1.8	V	$V_{GS} = 0V$, $I_{SD} = 1.0A$
		TO-243AA			2.0		$V_{GS} = 0V$, $I_{SD} = 0.5A$
t_{rr}	Reverse Recovery Time			300		ns	$V_{GS} = 0V$, $I_{SD} = 1A$

Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

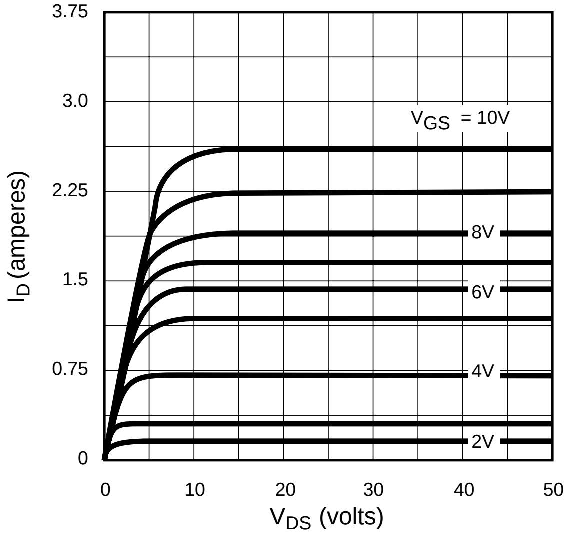
Switching Waveforms and Test Circuit



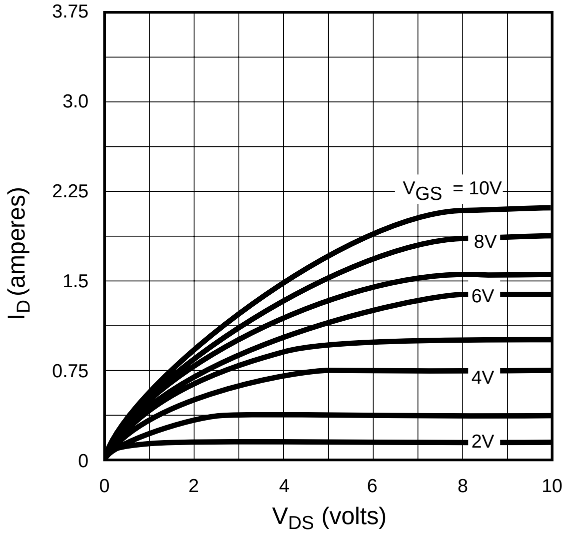


Typical Performance Curves

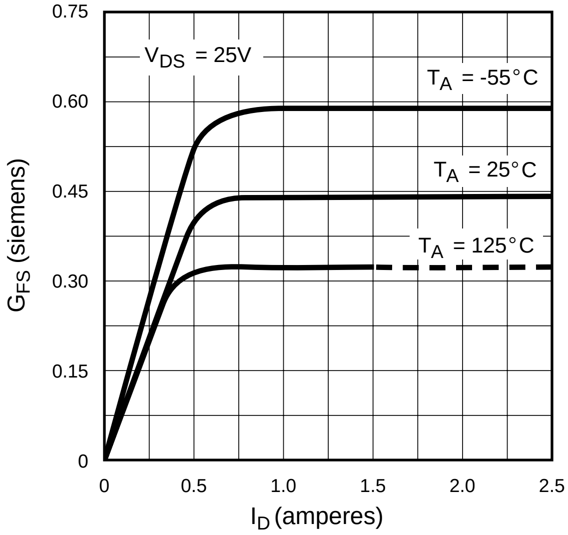
Output Characteristics



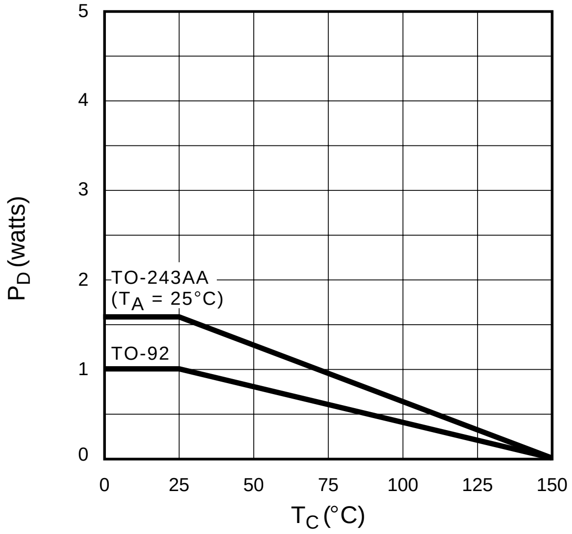
Saturation Characteristics



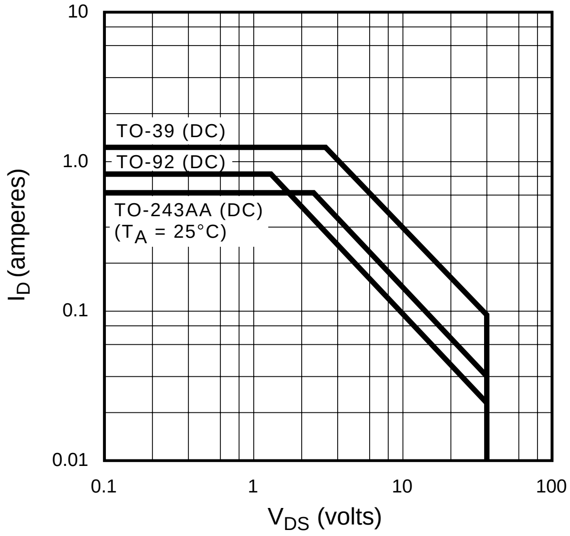
Transconductance vs. Drain Current



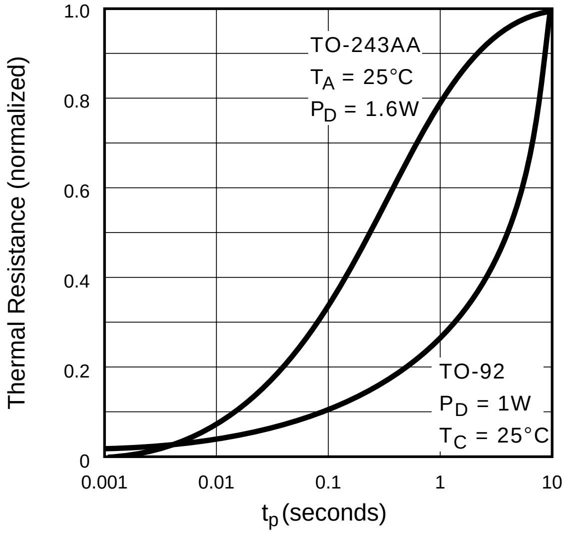
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

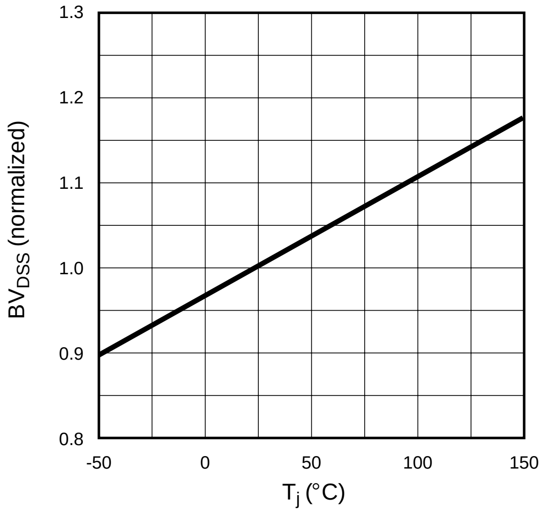


Thermal Response Characteristics

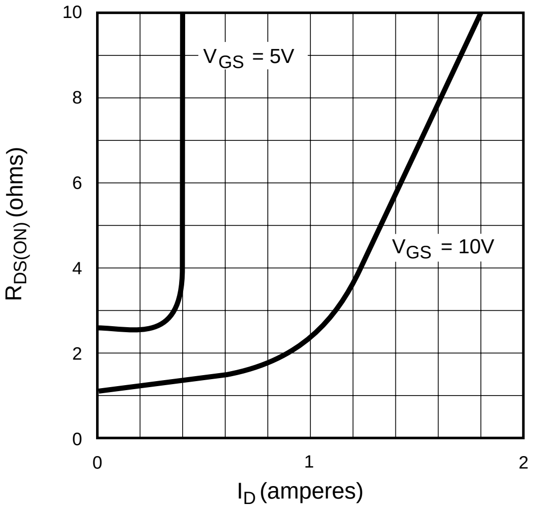


Typical Performance Curves

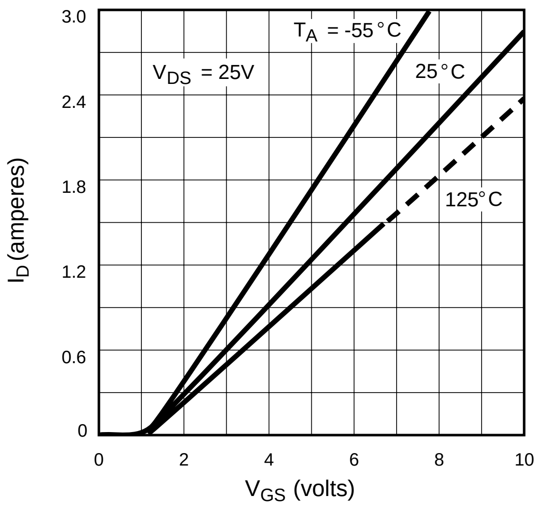
BV$_{DSS}$ Variation with Temperature



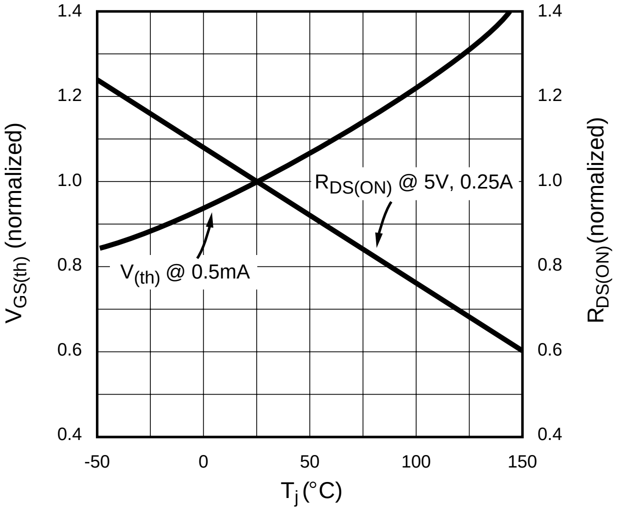
On-Resistance vs. Drain Current



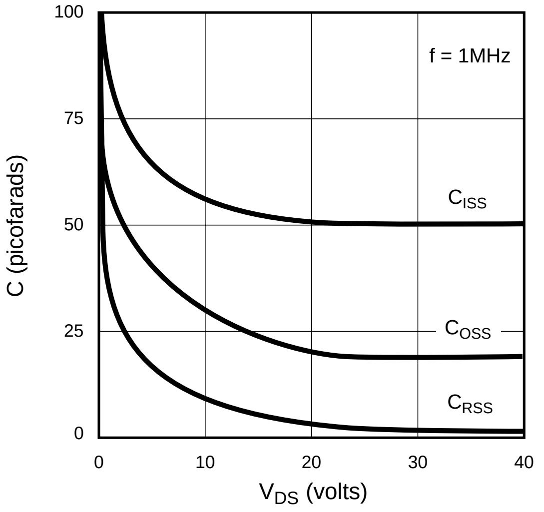
Transfer Characteristics



V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics