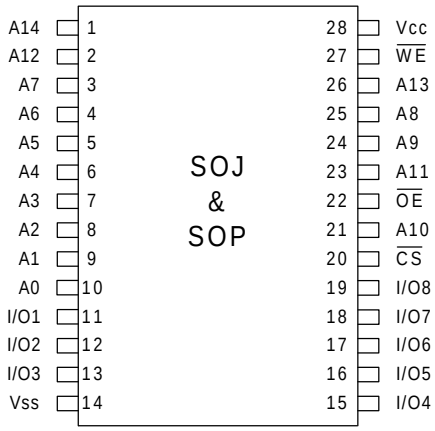
SRAM

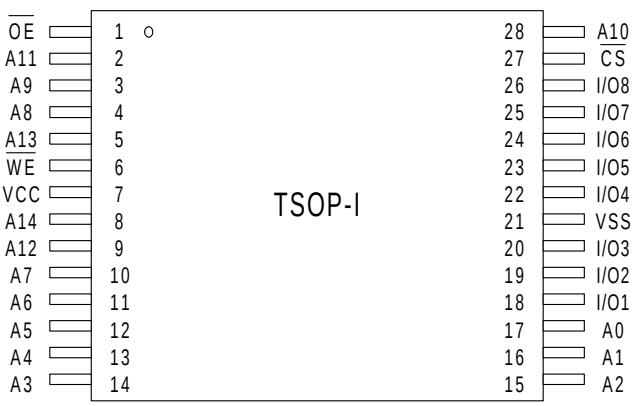
32K X 8 LOW POWER CMOS STATIC RAM

FEATURES

- Access time: 35ns/70ns
- Low power consumption : Active 200 mW(typ.)
- Low operating current : 50mA
- Single + 5 power supply
- Fully static operation – No clock or refreshing required
- All inputs and outputs directly TTL compatible
- Common I/O capability
- Available packages : 28-pin 300 mil SOJ, 28-pin SOP, TSOP-I (forward type).
- Output enable ($\overline{OE}$) available for very fast access
- Mix-mode Outputs

PIN CONFIGURATION

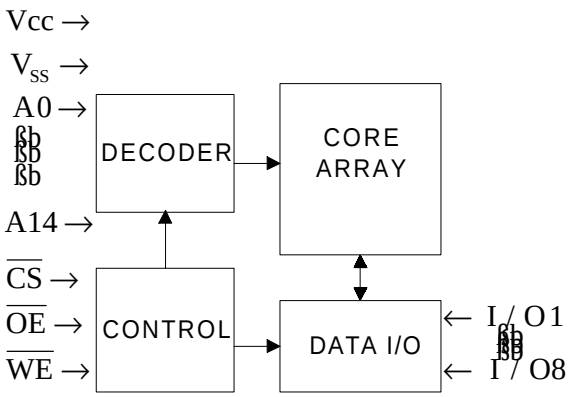




GENERAL DESCRIPTION

The T15M256A is a high speed, low power CMOS static RAM organized as 32,768 x 8 bits that operates on a single 5-volt power supply. This device is packaged in standard 28-pin 300 mil SOJ ,28-pin SOP, TSOP-I forward.

BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A14	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
$\overline{CS}$	Chip Select Inputs
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power Supply
Vss	Ground

PART NUMBER EXAMPLES

	PACKAGE	SPEED
T15M256A-35J	SOJ	35ns
T15M256A-70P	TSOP-I	70ns
T15M256A-70D	SOP	70ns

DC CHARACTERISTICS ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply Voltage to Vss Potential	-0.5 to + 6	V
Inputs to Vss Potential	-0.5 to Vcc +0.5	V
Power Dissipation	0.5	W
Storage Temperature	-60 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYM	MIN	TYP	MAX	UNIT
Supply Voltage	Vcc	Typ-5%	5	Typ+5%	V
Input Voltage, low	V_{IL}	-0.3	-	0.8	V
Input Voltage, high	V_{IH}	2.2	-	Vcc+0.3	V
Ambient Temperature	T_A	0	-	70	°C

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O1- I/O8	Vcc
H	X	X	Not Selected	High-Z	$I_{SB,}I_{SB1}$
L	H	H	Output Disable	High-Z	Icc
L	L	H	Read	Data Out	Icc
L	X	L	Write	Data In	Icc

OPERATING CHARACTERISTICS

(Vcc = 5V± 5%, Vss = 0V, Ta = 0 to 70°C)

PARAMETER	SYM.	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input Leakage Current	I_{LI}	Vin=Vss to Vcc		-10	-	+10	µA
Output Leakage Current	I_{LO}	$V_{I/O}$=Vss to Vcc, $\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}		-10	-	+10	µA
Output Low Voltage	V_{OL}	I_{OL} = + 8.0mA		-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = - 4.0mA		2.4	-	-	V
Operating Power Supply Current	Icc	$\overline{CS}$ = V_{IL}, I/O=0mA Cycle = MIN. Duty = 100%	-35	-	-	50	mA
			-70	-	-	50	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, Cycle=MIN, Duty=100%		-	-	10	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC}-0.2V		-	-	2	mA

Note: Typical characteristics are at Vcc = 5V, Ta = 25°C

CAPACITANCE

(Vcc = 5V, Ta = 25°C, f = 1 MHz)

PARAMETER	SYMBOL	CONDITION	MAX.	UNIT
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF
Input/ Output Capacitance	$C_{I/O}$	V_{OUT}= 0V	8	pF

Note: These parameters are sampled but not 100% tested.

AC TEST CONDITIONS

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3 ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L =30pF,I_{OH}/I_{OL} = -4mA/8mA

AC TEST LOADS AND WAVEFORM

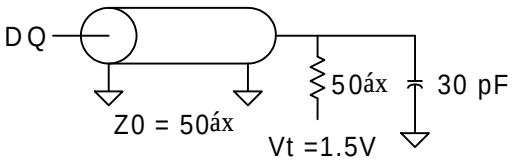


Fig.1

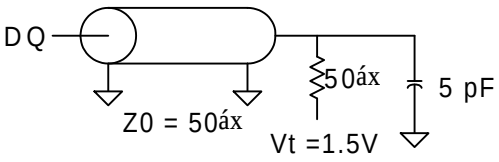


Fig.3

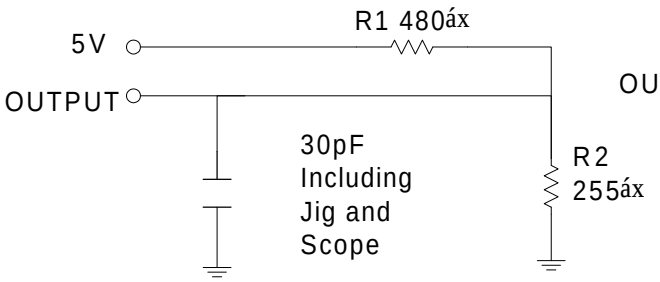


Fig.2

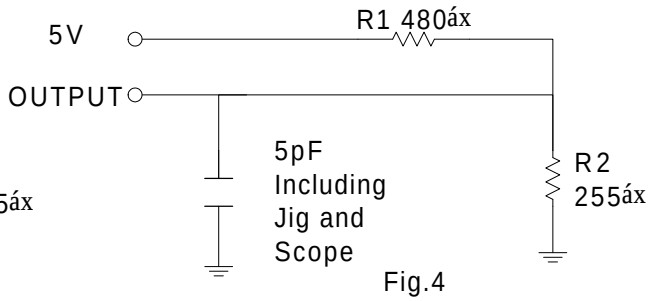


Fig.4

(For TCLZ, TOLZ, TCHZ, TOHZ, TWHZ, TOW)

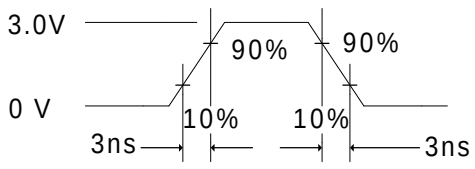


Fig.5

AC CHARACTERISTICS

(V_{CC}=5V ± 5%, Vss = 0V, Ta = 0 to 70°C)

(1) READ CYCLE

PARAMETER	SYM.	T15M256A-35		T15M256A-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	T_{RC}	35	àµ	70	àµ	ns
Address Access Time	T_{AA}	àµ	35	àµ	70	ns
Chip Select Access Time	TACS	àµ	35	àµ	70	ns
Output Enable to Output Valid	T_{AOE}	àµ	25	àµ	35	ns
Chip Selection to Output in Low Z	T_{CLZ}*	3	àµ	3	àµ	ns
Output Enable to Output in Low Z	T_{OLZ}*	0	àµ	0	àµ	ns
Chip Deselection to Output in High Z	T_{CHZ}*	àµ	25	àµ	35	ns
Output Disable to Output in High Z	T_{OHZ}*	àµ	25	àµ	35	ns
Output Hold from Address Change	T_{OH}	3	àµ	3	àµ	ns

* These parameters are sampled but not 100% tested.

(2)WRITE CYCLE

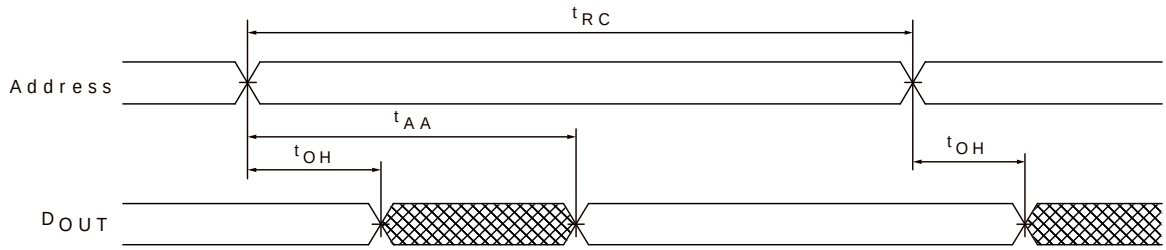
PARAMETER	SYM.	T15M256A-35		T15M256A-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	T_{WC}	35	àµ	70	àµ	ns
Chip Selection to End of Write	T_{CW}	30	àµ	60	àµ	ns
Address Valid to End of Write	T_{AW}	30	àµ	60	àµ	ns
Address Setup Time	T_{AS}	0	àµ	0	àµ	ns
Write Pulse Width	T_{WP}	25	àµ	50	àµ	ns
Write Recovery Time	T_{WR}	0	àµ	0	àµ	ns
Data Valid to End of Write	T_{DW}	20	àµ	30	àµ	ns
Data Hold from End of Write	T_{DH}	0	àµ	0	àµ	ns
Write to Output in High Z	T_{WHZ}*	àµ	10	àµ	25	ns
Output Disable to Output in High Z	T_{OHZ}*	àµ	10	àµ	25	ns
Output Active from End of Write	T_{OW}	0	àµ	0	àµ	ns

* These parameters are sampled but not 100% tested.

TIMING WAVEFORMS

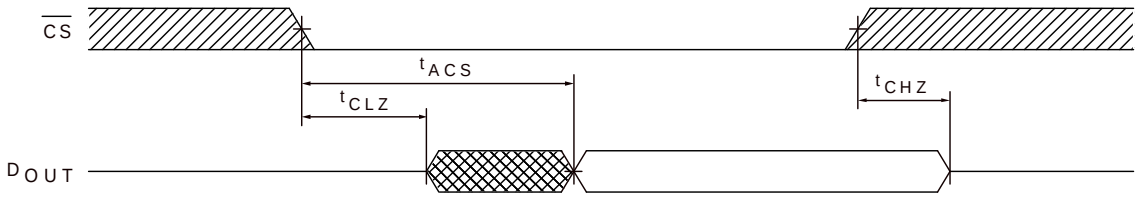
READ CYCLE 1

(Address Controlled)



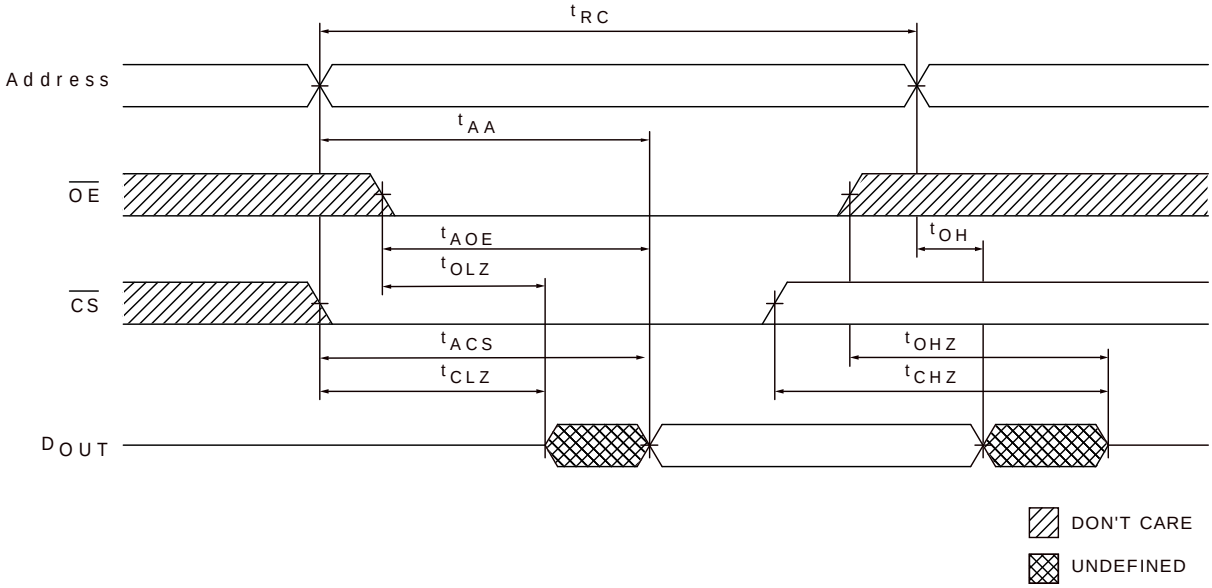
READ CYCLE 2

(Chip Select Controlled)

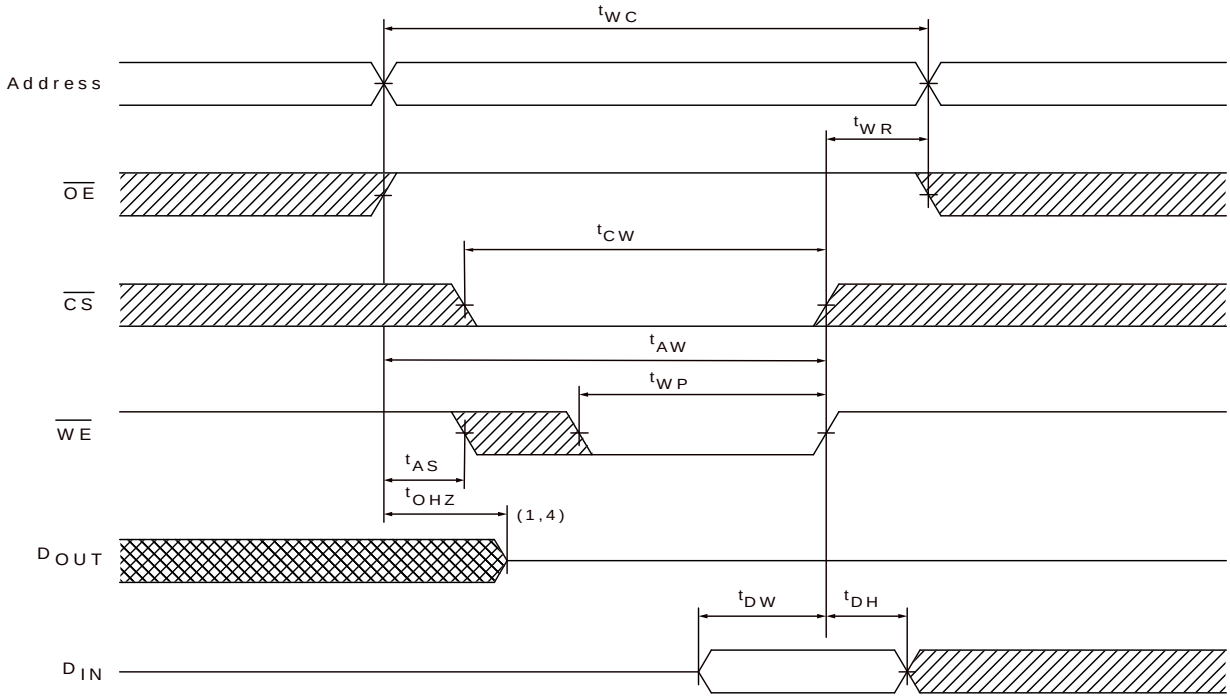


READ CYCLE 3

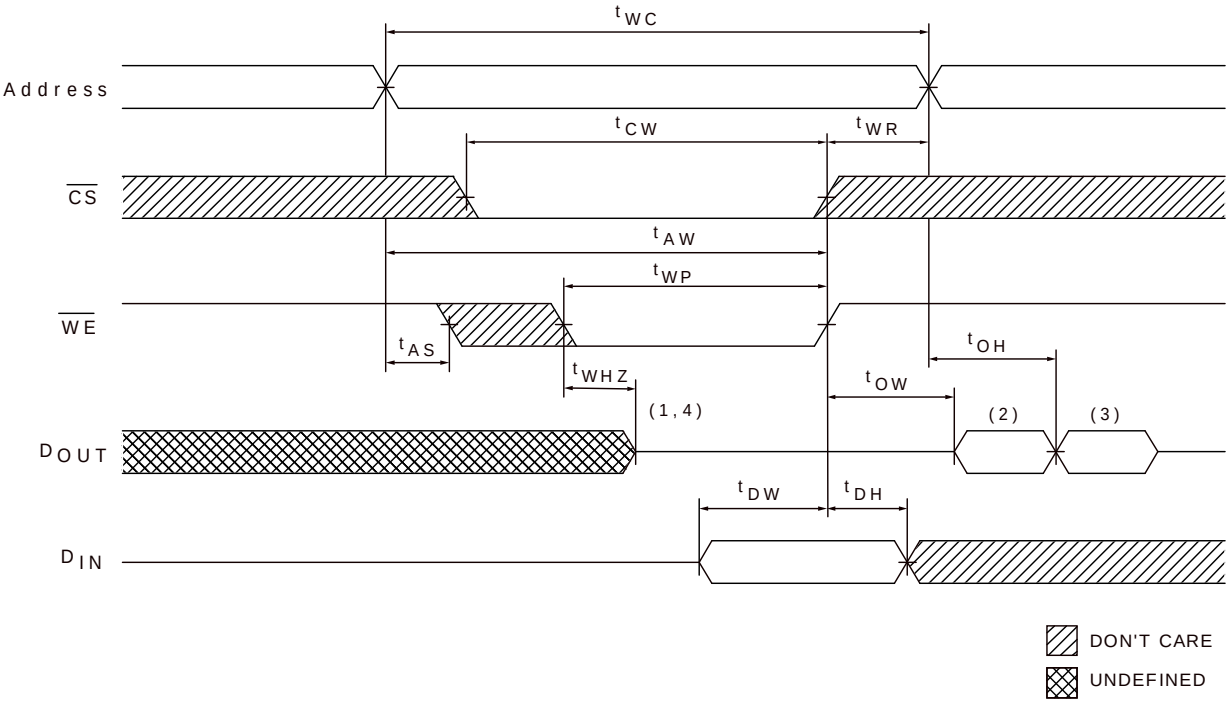
(Output Enable Controlled)



WRITE CYCLE 1 ($\overline{OE}$ CLOCK)



WRITE CYCLE 2 ($\overline{OE}$ = V_{IL} Fixed)

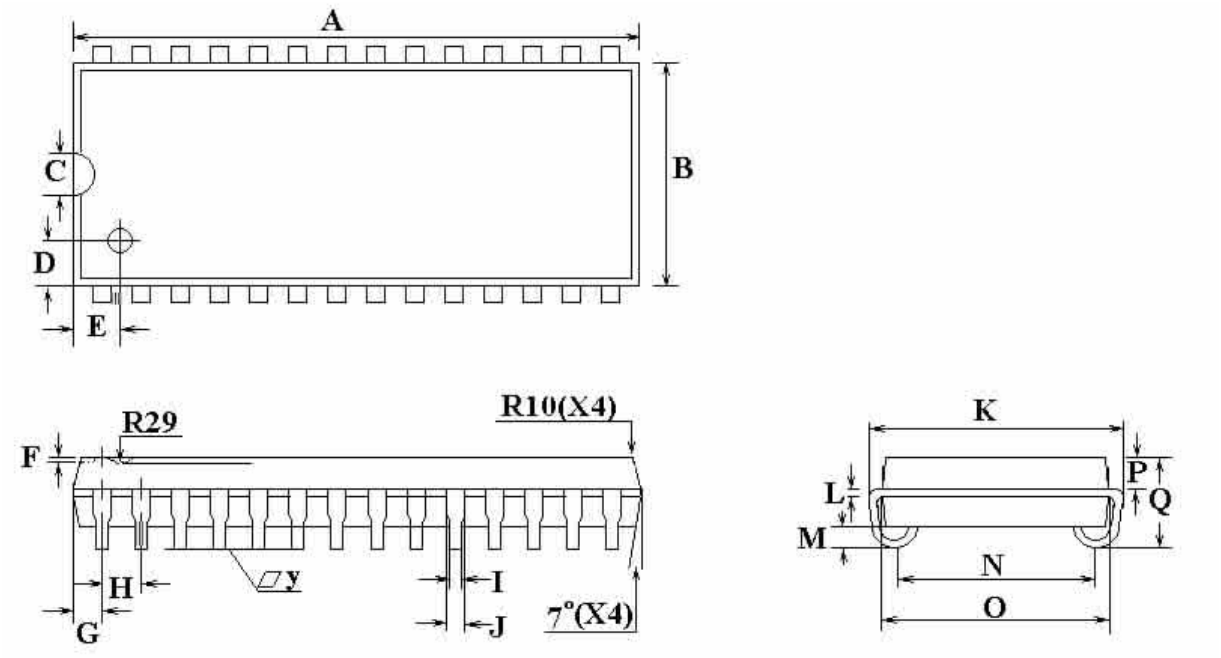


Notes: 1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.

2. The data output from D_{OUT} are the same as the data written to D_{IN} during the write cycle.
3. D_{OUT} provides the read data for the next address.
4. Transition is measured ± 500 mV from steady state with C_L = 5pF. This parameter is guaranteed but not 100% tested.
5. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

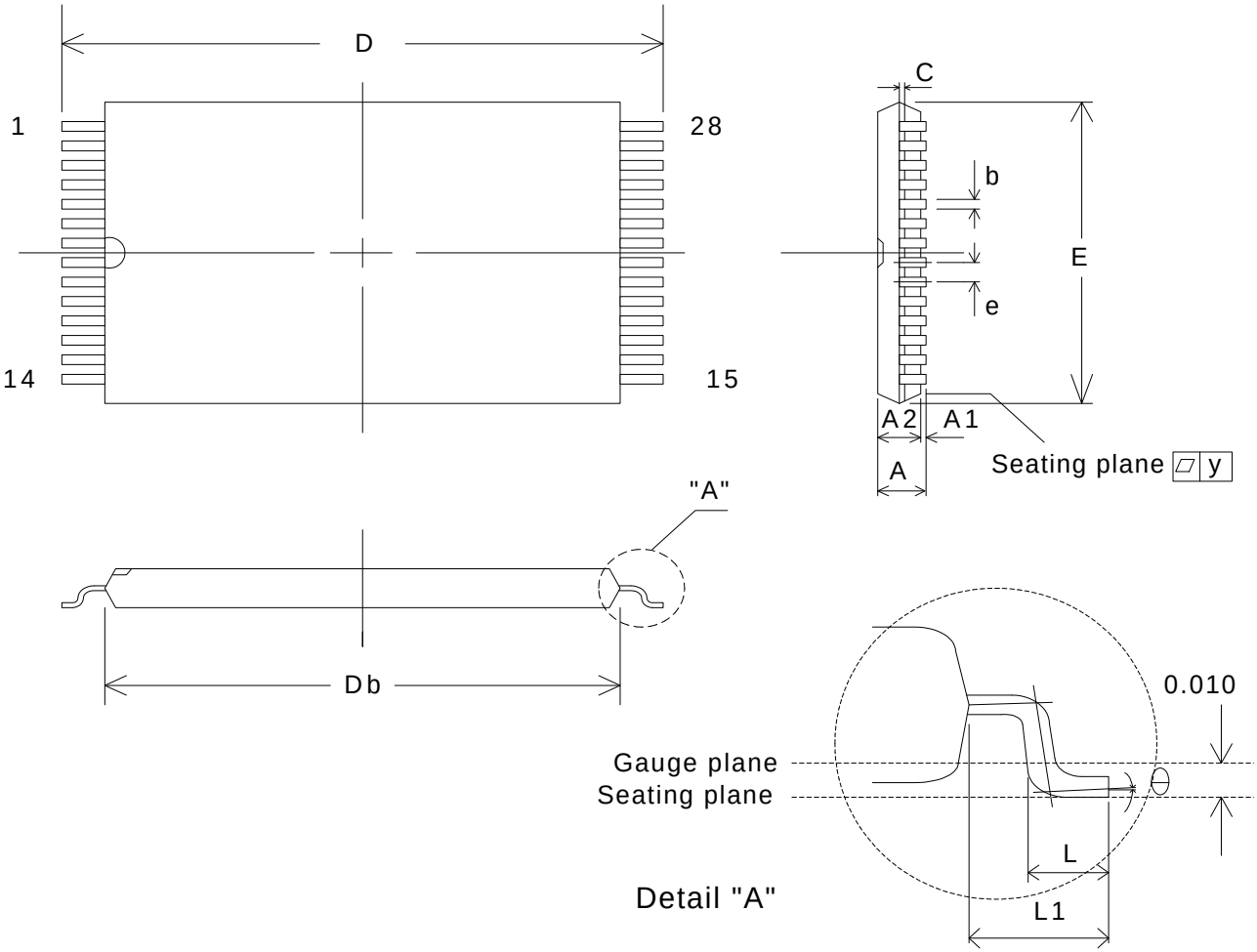
PACKAGE DIMENSIONS

28-LEAD SOJ SRAM (300 mil)



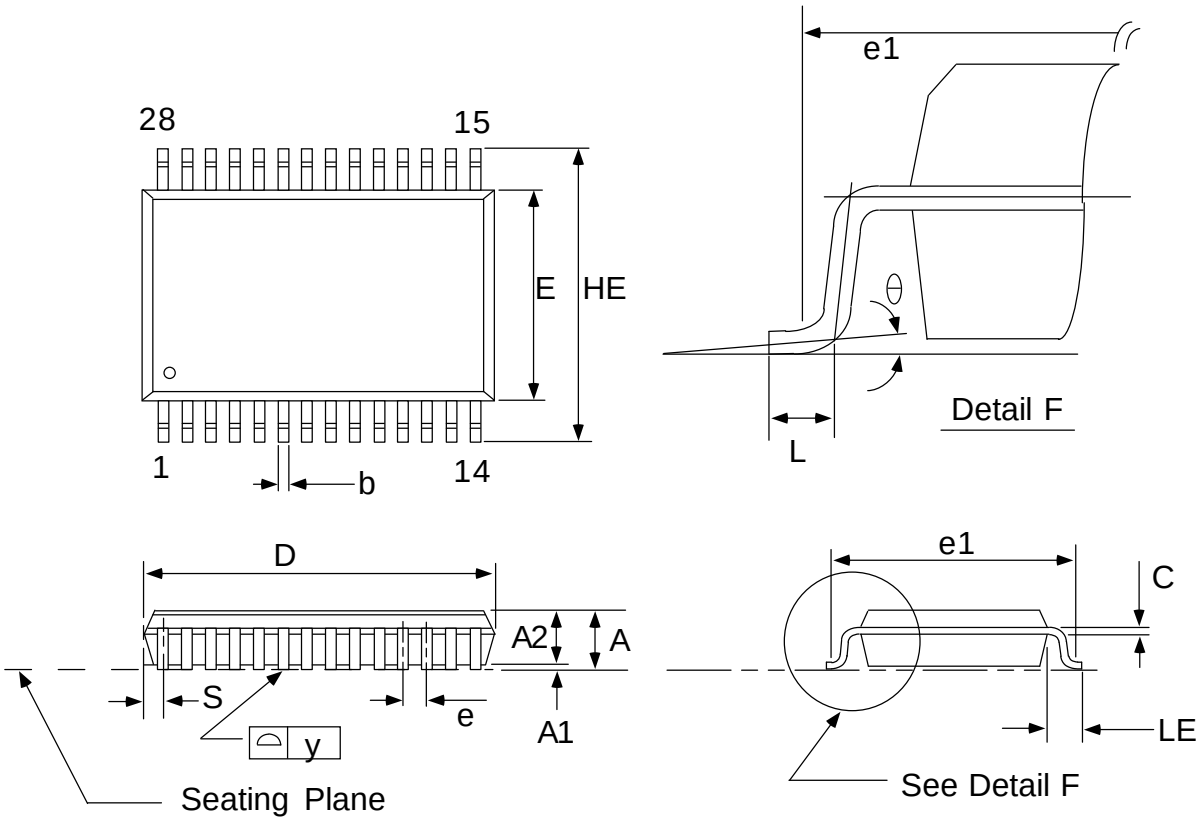
SYMBOL	DIMENSIONS IN INCHES	DIMENSIONS IN MM
A	0.710±0.002	18.03±0.05
B	0.336±0.003	8.53±0.08
C	0.060±0.002	1.52±0.05
D	0.050±0.001	1.27±0.03
E	0.063±0.001	1.63±0.03
F	0.015±0.002	0.38±0.05
G	0.030±0.002	0.76±0.05
H	0.050±0.002	1.27±0.05
I	0.018±0.002	0.46±0.05
J	0.028±0.002	0.71±0.05
K	0.337±0.002	8.56±0.05
L	0.010±0.001	0.25±0.03
M	0.026±0.002	0.66±0.05
N	0.268±0.003	6.81±0.08
O	0.300±0.002	7.62±0.05
P	0.053±0.001	1.35±0.03
Q	0.140±0.004	3.56±0.10
y	0.004(MAX)	0.10(MAX)

PACKAGE DIMENSIONS
28-LEAD TSOP-I SRAM (8X13.4mm)



SYMBOL	DIMENSIONS IN INCHES	DIMENSIONS IN MM
A	0.047(max.)	1.20(max.)
A1	0.004ßđ0.002	0.10ßđ0.05
A2	0.039ßđ0.002	1.00ßđ0.05
b	0.008(typ.)	0.20(typ.)
c	0.006(typ.)	0.15(typ.)
Db	0.465ßđ0.004	11.80ßđ0.10
E	0.315ßđ0.004	8.00ßđ0.10
e	0.022(typ.)	0.55(typ.)
D	0.528ßđ0.008	13.40ßđ0.20
L	0.020ßđ0.004	0.50ßđ0.10
L1	0.0315ßđ0.004	0.80ßđ0.10
y	0.004(max.)	0.10(max.)
áh	0àu~5àu	0àu~5àu

PACKAGE DIMENSIONS
28-LEAD SOP



Symbol	Dimension in inches			Dimension in mm		
	min.	typ.	max	min.	typ.	max.
A	-	-	0.098	-	-	2.5
A1	0.01	-	-	0.25	-	-
A2	0.083	0.085	0.087	2.13	2.15	2.17
b	0.014	0.016	0.018	0.39	0.4	0.41
C	0.004	0.006	0.008	0.1	0.15	0.2
D	-	0.713	0.733	-	18.1	18.6
E	0.322	0.331	0.338	8.2	8.4	8.6
e	0.044	0.050	0.056	1.12	1.27	1.42
HE	0.453	0.465	0.476	11.5	11.8	12.1
L	0.026	0.033	0.041	0.65	0.85	1.05
LE	0.047	0.059	0.071	1.2	1.5	1.8
S	-	39	-	-	1.0	-
y	-	-	0.005	-	-	0.12
á¡	0àu	-	10àu	0àu	-	10àu

Notes :
1. Dimensions D max. & S include mold flash or tie bar burrs.
2. Dimension b does not include dambar protrusion / intrusion.
3. Dimensions D & E include mold mismatch and determined at the mold parting line.
4. controlling dimension : inches
5. general appearance spec should be based on final visual inspection spec.