TMC2376

PC-to-TV Video Standards Converter

Features

- Programmable to VESA and Industry Standard timing modes.
- Frame rate Conversion
- Programmable 2D scaling
- Frame-store memory controller
- Accepts 640x480 , 800x600, 1024x768 VGA, Mac
- Multiple output standards: NTSC, NTSC-EIA, PAL-B/G/H/I, SCART, Y/C, CVBS, RGB, YUV formats
- Pan and Zoom
- 3-Line Flicker filter
- I^2C compatible port controls
- Synclock
- 8-bit A/D converters
- 24-bit RGB input port
- 9-bit output D/A converters

Applications

- PC video inputs for TVs or interlaced monitors
- TV out for PCs, VGA or graphics cards
- Internet appliances, net browsers
- Video Kiosks

See use restrictions on backpage.

Description

A range of VGA formats/refresh rates can be converted to NTSC and PAL standards compliant with SMPTE-170M and CCIR-624 standards. Within the TMC2376 are capture and encoder engines separated by the frame buffer memory controller. Required external components are minimal: 16M SDRAM memory, clocks and passive parts.

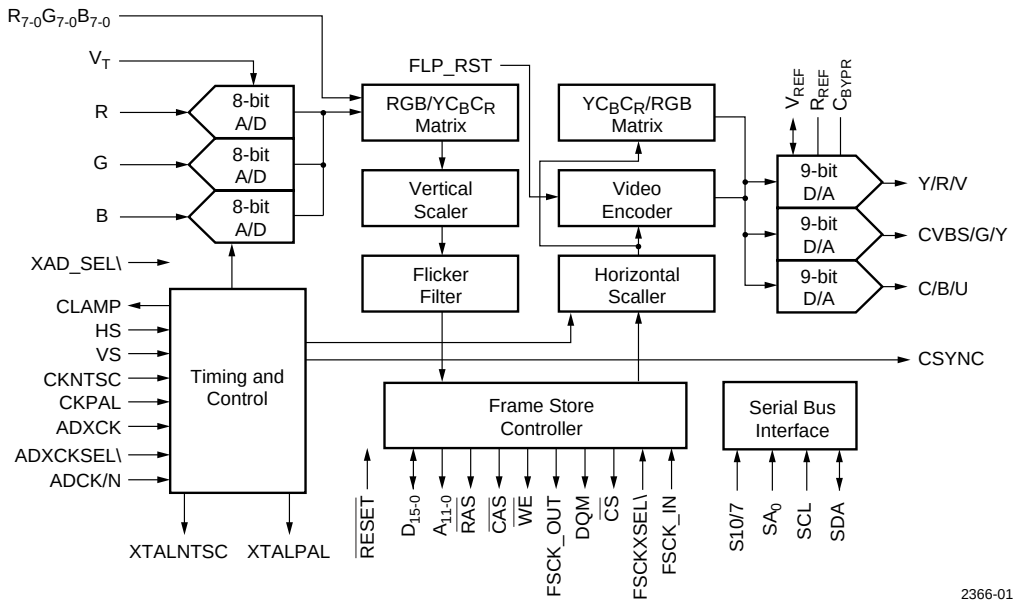
RGB video inputs are converted to the YUV422 format. Vertical scaling and flicker filtering are implemented at the VGA frame rate ahead of the frame store interface.

Frame rate conversion is implemented with by a Frame Store Controller that interfaces with an external SDRAM frame store memory.

YUV422 data is recovered from the memory at the outgoing frame rate. Data is scaled prior to the digital video encoder which generates Y/C and CVBS outputs. For RGB outputs, the encoder may be bypassed via a YUV to RGB transcoder for SCART compatible video.

Setup is via an I^2C compatible serial port. Power is derived from +3.3V and +5V supplies. Package is a 128-lead Metric Quad Flat Pack (MQFP).

Architectural Block Diagram



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Rev. 0.9.4

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Architectural Overview

Overall design structure is outlined in this section. Details of how to use and setup the TMC2376 are included in the Functional Description section.

RGB video inputs are asynchronously converted to either NTSC/PAL, YUV or RGB video formats. Architecturally, the TMC2376 is divided into five major sections:

- Video Capture Engine
- Clock Processor
- Frame Store Controller
- Video Encoder Engine
- Serial Bus Interface

Besides power and a few external passive components, the TMC2376 requires only a single 16M external SDRAM and external clocks to implement a high quality video standards converter.

Analog RGB inputs with separate horizontal and composite sync signals are accepted. Analog video must be AC coupled to allow clamping during the horizontal sync period. Digital inputs must be 24-bit RGB clocked by external clock, ADXCK.

A wide range of resolution formats can be accepted, including VESA and industry standards such as 640x480, 800x600 and 1024x768. Incoming RGB signals are converted to either the NTSC or PAL TV Standards. Output video format can be selected to be either composite, Y/C, RGB or YUV.

Incoming frame rate can range from 56 to 95 Hz. The Video Capture engine runs asynchronously relative to the Video Encoder Engine. An external frame store memory separates the two engines with write and read access controlled by the TMC2376.

Transformation operations include overscan, underscan, pan and zoom. Scaling operations are separated by the frame store with vertical down-sampling incorporated into the Capture Engine and horizontal up-sampling incorporated into the Encoder Engine.

Video Capture Engine

AC coupled RGB video inputs are clamped to ground. Triple 8-bit A/D converters digitize the analog RGB inputs at rates of up to 50 Ms/s. Internal A/D sample clock, ADCK is derived from a phase locked loop referenced to the leading edge of horizontal sync. Either positive or negative sync polarity is accepted.

The selected input (A/D converter outputs or TMC2376 digital RGB) is transcoded by the color matrix into the 16-bit YC_BC_R422 format. Next, the Vertical Scaler reduces the number of incoming video lines by the selected scaling factor. Finally, the 3-line Flicker Filter averages lines to eliminate flicker between horizontal lines or along horizontal boundaries.

Frame Store Memory Controller

Inserted between the capture and the encoder engines, the frame store has two functions: one is to act as a reservoir of pixels to match the incoming frame rate the outgoing field rate; the other is to support vertical scaling by allowing lines to be written into the frame store intermittently, but read out at a constant rate.

Frame store clock, FS_CK is derived from the CKNTSC clock by a second phase locked loop that is referenced to the 4 fsc subcarrier clock.

Video Encoder Engine

Pixels are retrieved from the external frame store memory asynchronously relative to the incoming frames. Outgoing video timing is set to the selected TV standard, either NTSC or PAL.

Incoming data sampling is normally set to fill complete lines in the Frame Store Memory. Horizontal scaling is applied to pixels exiting the Frame Store. Pixels may be routed through either a digital video encoder or an YC_BC_R-to-RGB transformation matrix. Either output is connected to a triple 9-bit D/A converter to generate the video output which can be in either CVBS, Y/C, RGB or YUV format.

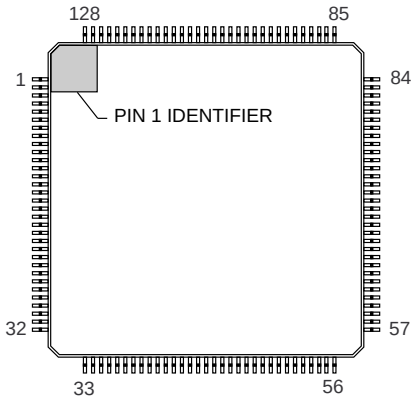
Encoder Engine timing is derived from one of two 4x subcarrier sources: 14.31818 MHz CKNTSC for NTSC; 17.734475 MHz CKPAL for PAL.

Serial Control Port

TMC2376 setup is programmed by fourteen 10-bit registers that are accessible via the I^2C compatible serial port. Status and Revision ID can also be read from the registers.

Pin Assignments

128-Lead MQFP Package (TMC2376KC)



Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	CKNTSC	33	VDD5X	65	ADCK/N	97	D12
2	XTALNTSC	34	N/C	66	ADXCKSEL	98	D13
3	CKPAL	35	N/C	67	ADXCK	99	D14
4	XTALPAL	36	FLP_RST	68	VDDPA	100	D15
5	VSS5X	37	RESET	69	VSSPA	101	VSS5
6	VSSDA	38	R0	70	G3	102	B7
7	VREF	39	R1	71	G2	103	B6
8	RREF	40	R2	72	G1	104	B5
9	VDDDA	41	R3	73	G0	105	B4
10	CBPYR	42	VDDAD	74	VSS5	106	VDD3
11	CVBS/G/Y	43	VSSAD	75	DQM	107	A0
12	VDDDA	44	VSSAD	76	WE	108	A1
13	VSSDA	45	R	77	CS	109	A2
14	Y/R/V	46	VDDAD	78	RAS	110	A3
15	VDDDA	47	VDDAD	79	CAS	111	A4
16	C/B/U	48	G	80	VDD5	112	A5
17	VDDDA	49	VSSAD	81	D0	113	A6
18	VDD5	50	VTOUT	82	D1	114	A7
19	VDD5	51	VTIN	83	D2	115	A8
20	CSYNC	52	VSSAD	84	D3	116	A9
21	VSS5	53	B	85	D4	117	A10
22	VSS5	54	VDDAD	86	D5	118	A11
23	XA/D_SEL	55	CLAMP	87	D6	119	VDD5
24	G4	56	R4	88	D7	120	B3
25	G5	57	R5	89	VSS3	121	B2
26	G6	58	R6	90	VDD3	122	B1
27	G7	59	R7	91	D8	123	B0
28	VSS5X	60	VDD5X	92	D9	124	VSSPF
29	SCL	61	VSS5X	93	D10	125	FSCKXSEL
30	SDA	62	VS	94	D11	126	FSCK_OUT
31	SA10/7	63	HS	95	VDD3	127	FSCK_IN
32	SA0	64	VSS5X	96	VSS3	128	VDDPF

Preliminary Information

Pin Descriptions

Pin Name	Pin Number 128-pin MQFP	Type/Value	Pin Function Description
Clocks			
CKNTSC	1	TTL compatible input	**Reference Clock Input, NTSC.** Input from 14.31818 MHz external oscillator; or one pin of a crystal connected between CKNTSC and XTALNTSC. NTSC subcarrier frequency is derived from this 4x clock. CKNTSC must be connected (see *Table 4. 4x Clock Connections*)
XTALNTSC	2	TTL output	**NTSC Crystal Return.** If a crystal is used, connect one pin to CKNTSC, the other to XTALNTSC.
CKPAL	3	TTL compatible input	**Reference Clock, PAL.** Input from 17.734475 MHz external oscillator; or one pin of a crystal connected between CKPAL and XTALPAL. PAL subcarrier frequency is derived from this 4x clock.
XTALPAL	4	TTL output	**PAL Crystal Return.** If a crystal is used, connect one pin to CKPAL, the other to XTALPAL.
HS	63	TTL input	**VGA Horizontal Sync Input.** Active HIGH or active LOW polarity is sensed.
VS	62	TTL input	**VGA Vertical Sync Input.** Active HIGH or active LOW polarity is sensed.
Global Controls			
$\overline{\text{FLP\_RST}}$	36	TTL input	**Field, Line and Pixel Reset.** Resets video encoder engine to the start location on the outgoing frame. Used for genlock.
$\overline{\text{RESET}}$	37	TTL input	**Reset.** Resets internal state machines and initializes default register values.
A/D Converter Interface			
R, G, B	45, 48, 53	700/1000 mV pp	**Analog red, blue and green inputs.** AC coupled RGB video input signals. Nominal voltage range is 0.7 Volt peak-to-peak. Inputs are clamped to ground when HS_IN is active.
V_T	51	750/1050 mV	**A/D Converter Top Reference Voltage Input.** Input to voltage follower that supplies current to A/D converter reference resistors. Range is 0.5 - 2.0 volts.
V_{TOUT}	50	750/1050 mV	**A/D Converter Top Reference Voltage Output.** Voltage follower connection to top of A/D converter reference resistors.
ADXCK	67	TTL compatible input	**A/D converter clock.** Analog-to-digital converter external clock input if ADXCKSEL = H.
ADXCKSEL\	66	TTL input	**ADXCK select.** Selects the ADCK source: ADXCKSEL\ = L: external clock applied to the ADXCK pin. ADXCKSEL\ = H: internal phase-locked loop.
ADCK/N	65	TTL output	**ADCK divided by N.** ADCK divided by N for connection to external phase-locked loop controller.
CLAMP	55	TTL output	**Clamp out.** Clamp output signal. CLAMPO = H, when the internal clamp is active during the horizontal sync period, HS_IN.

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Pin Descriptions (continued)

Pin Name	Pin Number 128-pin MQFP	Type/Value	Pin Function Description
Digital RGB Inputs			
R_{7-0}	59, 58, 57, 56, 41, 40, 39, 38	TTL input	**Digital red input.** 8-bit red input data.
G_{7-0}	27, 26, 25, 24, 70, 71, 72, 73	TTL input	**Digital green input.** 8-bit green input data.
B_{7-0}	102, 103, 104, 105, 120, 121, 122, 123	TTL input	**Digital blue input.** 8-bit blue input data.
XAD_SEL\	23	TTL input	**Digital/analog RGB in select**. LOW selects external digital $R_{7-0}G_{7-0}B_{7-0}$ inputs; HIGH selects internal A/D converters with $R_{7-0}G_{7-0}B_{7-0}$ set to active outputs, states undefined.
Video Outputs			
Y/R/V	14	Analog Video	**Video output.** As programmed by Command Register $DACFMT_{1-0}$ bits: 00 Luminance component Y of S-video 01 Red component of RGB 1X V component of YUV
CVBS/G/Y	11	Analog video	**Video output.** As programmed by Command Register $DACFMT_{1-0}$ bits: 00 Composite video. 01 Green component of RGB. 1X Y component of YUV.
C/B/U	16	Analog Video	**Video output.** As programmed by Command Register $DACFMT_{1-0}$ bits: 00 Chrominance component of S-video. 01 Blue component of RGB. 1X U component of YUV.
CSYNC	20	TTL output	**Composite sync output.** Digital composite sync for YUV and RGB/ SCART video outputs.
Voltage Reference			
V_{REF}	7	+1.235 V	**Voltage reference input/output.** If unconnected, except for a 0.1µF capacitor to ground for noise decoupling, the internal 1.235 Volt band-gap reference will be supplied to the three D/A Converters . An external 1.235 volt reference connected to the V_{REF} pin, will override the internal voltage reference.
R_{REF}	8	392/768Ω	**Reference resistor.** Connected between R_{REF} and ground, this resistor sets the current range of the D/A converters.. Use 392Ω for a 37.5Ω load and 768Ω for a 75Ω load.
C_{BYPR}	10	0.1 µF	**Bypass Capacitor.** A 0.1µF capacitor must be connected between C_{BYPR} and V_{DDDA} to reduce noise at the D/A outputs.

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Pin Descriptions (continued)

Pin Name	Pin Number 128-pin MQFP	Type/Value	Pin Function Description
Frame Buffer Port			
D_{15-0}	100-97, 94-91, 88-81	TTL input/ output	**Data port, frame store memory.** 16-bit data bus for 16M SDRAM.
A_{11-0}	118-107	TTL output	**Address port, frame store memory.** 12-bit address bus for 16M SDRAM.
$\overline{RAS}$	78	TTL output	**Row address strobe.** $\overline{RAS}$ output for 16M SDRAM frame store memory.
$\overline{CAS}$	79	TTL output	**Column address strobe.** $\overline{CAS}$ output for 16M SDRAM frame store memory.
$\overline{WE}$	76	TTL output	**Write enable.** $\overline{WE}$ output for 16M SDRAM frame store memory.
DQM	75	TTL output	**Data Qualify.** Qualify data for 16M SDRAM frame store read/write operations. State is set by the memory access mode: DQM = L, enables memory outputs for read operations and exposes memory inputs for write operations. DQM = H, disables memory outputs and masks memory inputs
$\overline{CS}$	77	TTL output	**SDRAM chip select.** $\overline{CS}$ output for 16M SDRAM frame store memory.
FSCK_IN	127	TTL compatible input	**Frame store clock input.** Clock input to be routed to FSCK_OUT selected if FSCK_SEL = L.
FSCKXSEL\	125	TTL input	**Frame store clock select.** Selects either internal or external clock for 16M SDRAM frame store memory. If FSCKXSEL\ = H, the internal clock synthesized from CKNTSC is selected. With FSCKXSEL\ = L, the FSCK_IN input is selected.
FSCK_OUT	126	TTL output	**Frame store clock output**. FSCK_OUT for 16M SDRAM frame store memory.
Serial Port			
SA10/7	31	TTL input	**Serial address length select.** Selects the length of the serial address: SA10/7 = L: 10-bits SA10/7 = H: 7-bits
SA_0	32	TTL input	**Serial data address bit 0.** . Selects the serial bus address SA_0 = L: 0x6A, Ox276 SA_0 = H: 0x4A, Ox224
SDA	30	TTL input	**Serial data.** Data line of the serial port.
SCL	29	TTL input	**Serial clock.** Clock line of the serial port.
Power and Ground			
V_{DDAD}	42, 46, 47, 54	+5.0 V	**A/D converter Power.**
V_{DDPA}	68	+5.0 V	**ADCK Phase-locked loop Power**. Filtered +5 volt power for ADCK phase locked loop.
V_{DD3}	90, 95, 106	+3.3 V	**Digital Power.** 3.3 volt power for memory interface.

Pin Descriptions (continued)

Pin Name	Pin Number 128-pin MQFP	Type/Value	Pin Function Description
V_{DDPF}	128	+5.0 V	**FSCK Phase-locked loop Power.** Filtered +5 volt power for FSCK phase locked loop.
V_{DD5}	18, 19, 33, 60, 80, 119	+5.0 V	**Digital Power.** 5 volt power for digital sections of chip excluding the 3.3 volt memory interface.
V_{DDDA}	9, 12, 15, 17	+5.0 V	D/A Converter Power.
V_{SSAD}	43, 44, 49, 52	0 V	A/D Converter Ground.
V_{SSPA}	69	0 V	ADCK phase-locked loop ground.
V_{SS3}	89, 96	0 V	**Digital ground.** +3.3 volt power return.
V_{SSPF}	124	0 V	FSCK phase-locked loop ground.
V_{SS5}	5, 21, 22, 28, 61, 64, 74, 101	0 V	**Digital ground.** +5 volt power return.
V_{SSDA}	6, 13	0 V	D/A Converter Ground.

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Control Register Definitions

Control Register Functions

Control register functions are summarized in Table 1. Capture Engine parameter registers have no prefix; Command and Status registers are prefixed by 1; Encoder parameter registers are prefixed by 2.

Each internal register is 10-bits wide. To access a register two 8-bit data words must be transferred. In the case of a write, writing the second byte loads the internal 10-bit register. Most registers have type read/write. Read only registers access the internal status of the TMC2376. Write-only registers initiate the transfer of data.

For typical settings, see Video Formats/Register Settings.

Table 1. Control Register Map

Reg.	Bit #	Name	Type
Input horizontal offset			
0	7-0	IHO_{7-0}	R/W
1	1-0	IHO_{9-8}	R/W
Input vertical offset			
2	7-0	IVO_{7-0}	R/W
3	1-0	IVO_{9-8}	R/W
Input horizontal active width			
4	7-0	$IHAW_{7-0}$	R/W
5	1-0	$IHAW_{9-8}$	R/W
Input lines stored			
6	7-0	ILS_{7-0}	R/W
7	1-0	ILS_{9-8}	R/W

Reg.	Bit #	Name	Type
Input horizontal samples (per line)			
8	7-0	IHS_{7-0}	R/W
9	1-0	IHS_{9-8}	R/W
Input horizontal count			
A	7-0	IHC_{7-0}	R
B	1-0	IHC_{9-8}	R
Input vertical count (lines)			
C	7-0	IVC_{7-0}	R
D	1-0	IVC_{9-8}	R
Vertical scaling coefficient			
E	5-0	VSC_{5-0}	RW
F	-	-	W

Table 1. Control Register Map (continued)

Reg.	Bit #	Name	Type
Command register			
10	7-0	CR_{7-0}	R/W
11	1-0	CR_{9-8}	R/W
Status port			
12	3-0	S_{3-0}	R
13	—	—	—
Command register extended			
14	7-0	CRE_{7-0}	R/W
15	1-0	CDE_{9-8}	R/W
Not used			
16 - 1F			

Output horizontal offset			
20	7-0	OHO_{7-0}	R/W
21	—	—	R/W
Output vertical offset			
22	7-0	OVO_{7-0}	R/W
23	1-0	—	R/W
Horizontal scaling coeficient			
24	5-0	HSC_{7-0}	R/W
25	—	—	R/W
Not used			
26–3F	—	—	—

Status of internal registers following reset at power-up, is shown in Table 2. Note that all unused bits are set to zero and all unused register bits are set 0 for readback.

Table 2. Control Register Power-on Reset States

	Name	Function	Value hex (dec)
01,00	IHO_{9-0}	Input horizontal offset	80 (128)
03,02	IVO_{9-0}	Input vertical offset	80 (128)
05,04	$IHAW_{9-0}$	Input horizontal active width	200 (512)
07,06	ILS_{9-0}	Input lines stored	DC (220)
09,08	IHS_{9-0}	Input horizontal samples	2FE (766)
B,A	IHC_{8-0}	Input horizontal count	112 (274)[1]
D,C	IVC_{9-0}	Input vertical count	2FE (766)[1]
F,E	VSC_{5-0}	Vertical scaling coefficient	000
11,10	CR_{9-0}	Command register	001
12	S_{7-0}	Status register	00[2]
13	—	Not used	00
15,14	CRE_{9-0}	Command register extended	004
16-1F	—	Not used	00
21,20	OHO_{7-0}	Output horizontal offset	0C0 (192)
23,22	IVO_{7-0}	Output vertical offset	020 (32)
25,24	HSC_{5-0}	Horizontal scaling coefficient	000
26-2F	-	Not used	00

Notes:
1. May vary.
2. 01 if PLL is locked.

Control Registers Definitions

In the following definitions, range is defined as:

{min value:[max value]}.

Input Horizontal Offset Register Low (0)

7	6	5	4	3	2	1	0
IHO_7	IHO_6	IHO_5	IHO_4	IHO_3	IHO_2	IHO_1	IHO_0

Input Horizontal Offset Register High (1)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	IHO_9	IHO_8

Reg	Bit#	Bit Name	Description
1, 0	1-0, 7-0	IHO_{9-0}	**Input horizontal offset bits [9-0].** Horizontal displacement of the image in pixels from the leading edge of horizontal sync. Programming a value greater than IHS is illegal, preventing any pixels from being written into the Frame Store.

Range: {0 : [(Input Horizontal Samples(0x8,0x9) + 1) - Input Horizontal Active Width(0x4,0x5)]}.

Due to pipeline delays within the TMC2376, a bias of 42 must be added to the delay from the leading edge of sync to the start of active video expressed in A/D clock sampling ticks. For example, with a 40 MHz sampling clock and a 56.29 kHz line rate, there are 711 samples per line. Typical blanking period is 20% from the leading edge of horizontal sync to the start of active video, leading to a delay of 142 pixels. Adding 42 pixels, the correct OHO value is 184.

Input Vertical Offset Low (2)

7	6	5	4	3	2	1	0
IVO_7	IVO_6	IVO_5	IVO_4	IVO_3	IVO_2	IVO_1	IVO_0

Input Vertical Offset High (3)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	IVO_9	IVO_8

Reg	Bit#	Bit Name	Description
3, 2	1-0, 7-0	IVO_{9-0}	**Input vertical offset bits [9:0].** Vertical displacement of the image in lines from the leading edge of vertical sync plus a one line bias.

Range: {0 : [Input Vertical Count (0xC,0xD) – Input Lines Stored (0x6,0x7)]}.
Constraining the upper limit of the range prevents IVO from forcing the last line of an image with height ILS beyond the range of IVC.

Note:

1. Input Vertical Count (0xC,0xD) must be read to obtain the register value.

Input Horizontal Active Width Low (4)

7	6	5	4	3	2	1	0
$IHAW_7$	$IHAW_6$	$IHAW_5$	$IHAW_4$	$IHAW_3$	$IHAW_2$	$IHAW_1$	$IHAW_0$

Input Horizontal Active Width High (5)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	$IHAW_9$	$IHAW_8$

Reg	Bit#	Bit Name	Description
5, 4	1-0, 7-0	$IHAW_{9-0}$	**Input horizontal active width [9:0].** Number of incoming pixels to be stored in the Frame Store Memory following extraction from the incoming active video area.

Range: {0 : [{((Input Horizontal Samples (0x8,0x9) + 1) - Incoming Video Horizontal Blank):[720]}]}.

Note:

1. IHAW optimizes the number of stored pixels. Line store capacity limits the maximum value of IHAW to 720 active pixels per video line.

Input Lines Stored Low (6)

7	6	5	4	3	2	1	0
ILS_7	ILS_6	ILS_5	ILS_4	ILS_3	ILS_2	ILS_1	ILS_0

Input Lines Stored High (7)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	ILS_9	ILS_8

Reg	Bit#	Bit Name	Description
7, 6	1-0, 7-0	ILS_{9-0}	**Input lines stored bits [9:0].** Number of incoming lines per field to be stored in the Frame Store Memory following extraction from the incoming active video area.

Range: {0 : [{(Input Vertical Count (0xC,0xD) - Incoming Video Vertical Blank) * (1 - (Input Line Drop Coefficient (0xE,0xF)/64))/2:[PAL or NTSC Active lines per field]}]}.

Note:

1. Input number of lines accepted = ILS * 2 * [64 / (64 - VSC)].
2. VSC is the vertical scaling coefficient. The term in [ ] brackets is the reciprocal of the vertical scaling factor. A factor of two is included to account for interlace.

Input Horizontal Samples Low (8)

7	6	5	4	3	2	1	0
IHS_7	IHS_6	IHS_5	IHS_4	IHS_3	IHS_2	IHS_1	IHS_0

Input Horizontal Samples High (9)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	IHS_9	IHS_8

Reg	Bit#	Name	Description
9, 8	1-0, 7-0	IHS_{9-0}	**Input horizontal line samples bits [9:0].** Terminal count of the number of clocks per horizontal line between incoming horizontal sync pulses. Internal ADCK phase-locked loop is programmed with this value.

Range: {Min ADCK PLL Frequency * Input Horizontal Count (0xA,0xB) *(NTSC $4f_{SC}$ Period - (PAL_NTSC (0x10,0x11:Bit 1) * (NTSC $4f_{SC}$ Period - PAL $4f_{SC}$ Period))):[{Max ADCK PLL Frequency * Input Horizontal Count (0xA,0xB) * (NTSC $4f_{SC}$ Period - (PAL_NTSC (0x10,0x11:Bit 1) * (NTSC $4f_{SC}$ Period - PAL $4f_{SC}$ Period))):[1022]]}].

Note:

1. ADCK PLL frequency = $4f_{SC} * IHS / IHC$. Accounting for the maximum and minimum PLL VCO frequencies establishes the limits on the range of IHS. In the range equation, the PAL_NTSC bit controls addition of the difference between NTSC and PAL $4f_{SC}$ clock periods.

Input Horizontal Count Low (A)

7	6	5	4	3	2	1	0
IHC_7	IHC_6	IHC_5	IHC_4	IHC_3	IHC_2	IHC_1	IHC_0

Input Horizontal Count High (B)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	IHC_8

Reg	Bit#	Bit Name	Description
B, A	0, 7-0	IHC_{8-0}	**Input horizontal count bits [8:0] (read only).** Number of $4f_{SC}$ clock pulses per horizontal line. $4f_{SC}$ is the selected 4X subcarrier clock (17.734 MHz for PAL or 14.318 MHz for NTSC). IHC can be read to determine the incoming horizontal line frequency for auto selection of the incoming video format.

Range: {0:[511]}.

Input Vertical Count Low (C)

7	6	5	4	3	2	1	0
IVC_7	IVC_6	IVC_5	IVC_4	IVC_3	IVC_2	IVC_1	IVC_0

Input Vertical Count High (D)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	IVC_9	IVC_8

Reg	Bit#	Bit Name	Description
D, C	1-0, 7-0	IVC_{9-0}	**Input vertical line count bits [9:0] (read only).** Terminal count of the number of incoming lines per frame. IVC is used to determine the incoming vertical refresh frequency for auto selection of the incoming video format.

Range: {0:[1022]}.

Vertical Scaling Coefficient (E)

7	6	5	4	3	2	1	0
0	0	VSC_5	VSC_4	VSC_3	VSC_2	VSC_1	VSC_0

Vertical Scaling Coefficient (F)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Reg	Bit#	Bit Name	Description
E	5-0	VSC_{5-0}	**Vertical scaling coefficient bits [5:0], m.** The number of lines that must be removed modulo 64 to down-sample the incoming frame to the number of active lines in the outgoing TV frame. Vertical scaling factor = (1 - m/64).
F	-	-	**Load .** Writing to register F activates register E data.

Range: {0:[{(1 - (2 * Input Lines Stored(Offset 0x6,0x7) /(Input Vertical Count(Offset 0xC,0xD) - Input Vertical Blank))) * 64:[32]}]}.

In the above range, the vertical scaling coefficient, n is limited by the constraint that the scaling factor cannot reduce the number of input lines below the number of lines programmed to be stored. For example, 500 input lines cannot be scaled by 1/2 if the number of stored lines programmed is 300. However, if the number of stored lines, ILS is lowered to 200, then 200 of the 250 lines will be stored although the last 50 will be discarded.

Example: 480 line VGA image mapped to 400 line image.

VSC = (1-(400/480))*64 = 10.6667

Use 11 for the Coefficient value.

Command Register Low (10)

7	6	5	4	3	2	1	0
CBPF	LUMNTCH	UVALT	FRZ	RGBGAIN	ZOOM	PAL/NTSC	RESET

Command Register High(11)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	$DACFMT_1$	$DACFMT_0$

Reg	Bit#	Bit Name	Description
11	1-0	$DACFMT_{1-0}$	**DAC Output Format.** Selects between: 0 0 Y/C and CVBS 0 1 RGB 1 0 YUV 1 1 YUV
10	7	CBPF	0: Bypass chroma bandpass filter 1: Insert chroma bandpass filter
10	6	LUMNTCH	0: Bypass luminance notch filter 1: Insert luminance notch filter
10	5	UVALT	0: Cosite U and V samples 1: Alternate U and V samples
10	4	FRZ	0: Continuous update 1: Freeze frame
10	3	RGBGAIN	0: 1X input gain 1: 1.43 input gain
10	2	ZOOM	0: Zoom off 1: Zoom on
10	1	PAL/NTSC	0: select NTSC video output timing 1: select PAL video output timing
10	0	RESET	0: reset video pipeline (control registers are not affected) 1: run

Status Register (12)

7	6	5	4	3	2	1	0
$REVID_3$	$REVID_2$	$REVID_1$	$REVID_0$	STRTERR	0	0	PLL_LOCK

Reg	Bit#	Bit Name	Description
12	7-4	REVID	**Chip revision identification.** Starts at 0
12	3	STRTERR	**Output Video Start Position.** Flag indicates if active video has been programmed to overlay output horizontal sync. 0: Start position within limits 1: Start position error
12	2-1	-	Not used
12	0	PLL_LOCK	**SCLK PLL status.** 0: unlocked 1: locked

Unused Register (13)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Note:

1. Register 13 is the unused mate of register 12. 00 hex will be read back from register 13.

Command Register Extended Low (14)

7	6	5	4	3	2	1	0
FAZE	—	YCOFF	COMPOFF	ADCOFF	BIPGEN	OCS	FLIKON

Command Register Extended High (15)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Reg	Bit#	Bit Name	Description
14	7	FAZE	**Sample phase.** Sets the phase of the RGB A/D converter sampling clock. H = normal. L = inverted
14	6	-	Reserved
14	5	YCOFF	Luma and chroma video D/A converter power. 0 = Power on 1 = Power off
14	4	COMPOFF	Composite video D/A Converter Power. 0 = Power on 1 = Power off
14	3	ADCOFF	Analog-to-digital Converter Power. 0 = Power on 1 = Power off
14	2	BIPGEN	Built In Test Pattern Generator. 0: Select video input 1: Select test pattern
14	1	OCS	**Output Chroma Scale.** Sets the gain of the chrominance channel for optional de-saturation of colors. 0: 1X (normal) 1: 0.75X (de-saturate)
14	0	FLICKON	**Flicker Filter On.** Disables flicker filter to enhance vertical definition. Or enables three line vertical filtering to reduce line-to-line flicker on interlaced images. 0: bypass vertical filter. 1: three line vertical filtering.

Reg	Bit#	Bit Name	Description
15	1	-	**Reserved.**
15	0	-	**Reserved.**

Output Horizontal Offset Low (20)

7	6	5	4	3	2	1	0
OHO_7	OHO_6	OHO_5	OHO_4	OHO_3	OHO_2	OHO_1	OHO_0

Output Horizontal Offset High (21)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Reg	Bit#	Bit Name	Description
20	7-0	OHO_{7-0}	**Output horizontal offset [7:0].** Horizontal displacement of the outgoing active video area image in pixels from the leading edge of outgoing horizontal sync.
21	-	-	**Load.** Writing to register 21 activates register 20 data.

Range: { HBlank for NTSC or PAL in pixels:[255]}.

Output Vertical Offset Low (22)

7	6	5	4	3	2	1	0
OVO_7	OVO_6	OVO_5	OVO_4	OVO_3	OVO_2	OVO_1	OVO_0

Output Vertical Offset High (23)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Reg	Bit#	Bit Name	Description
22	7-0	OVO_{7-0}	**Output vertical offset [7:0].** Vertical displacement of the outgoing active video area in lines from the beginning of the equalization pulses: line 1/263 for NTSC; line 311/623 for PAL.
23	—	—	**Load.** Writing to register 23 activates register 22 data.

Range: {VBlank for NTSC or PAL in lines:[255]}.

Horizontal scaling Coefficient (24)

7	6	5	4	3	2	1	0
—	—	HSC_5	HSC_4	HSC_3	HSC_2	HSC_1	HSC_0

Horizontal scaling Coefficient (25)

7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—

Reg	Bit#	Bit Name	Description
24	5-0	HSC_{5-0}	**Horizontal scaling coefficient, n [5:0].** The number of pixels that must be added modulo 64 to up-sample the outgoing field from the frame store. Horizontal scaling factor = (1 + n/64).
25	-	-	**Load .** Writing to register 25 activates register 24 data.

Range: {0:[63]}.

Example: HSC = 1F hex; n = 31; Scaling factor = (1 + 31/64) = 1.48.

Functional Description

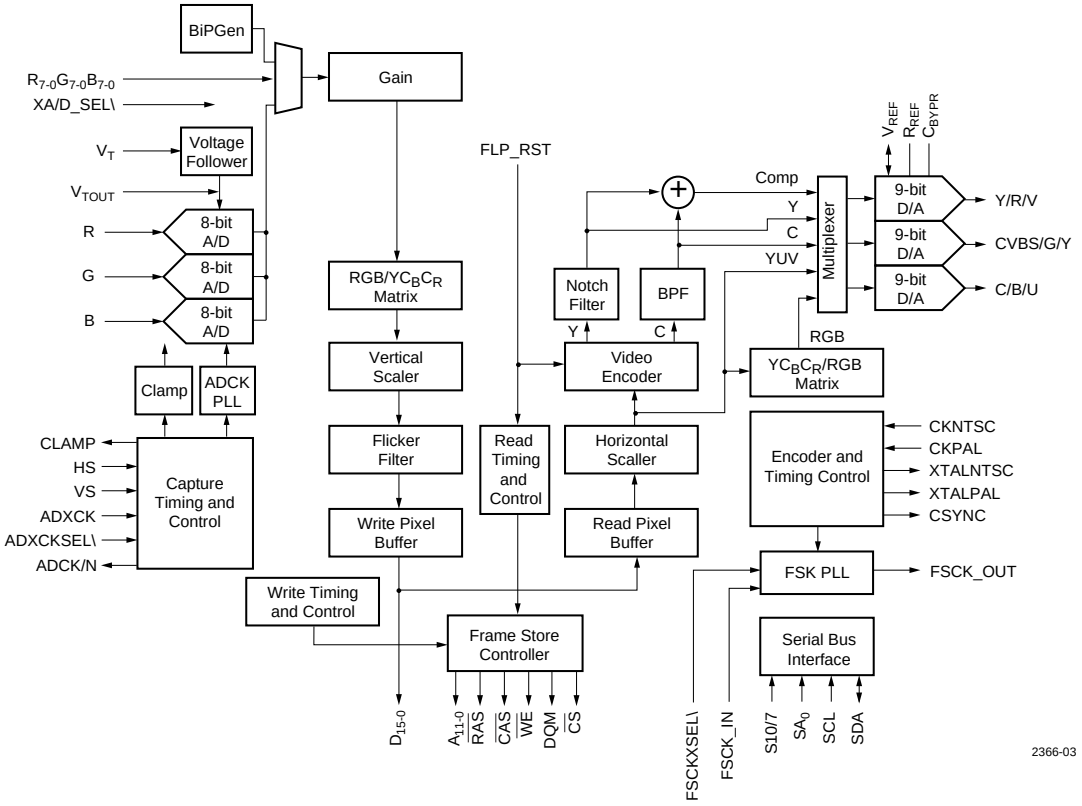


Figure 1. Functional Block Diagram

Details of how to connect and setup the TMC2376 are included in this section. Overall design principles are in the Architectural Overview section. Operation of the TMC2376 is divided into four sections:

- Capture Engine
- Frame Store Controller
- Encoder Engine
- Serial Control Port

Capture Engine

A/D Converters, Bit Pattern Generator, RGB/YUV Matrix, Vertical Scaler and Flicker Filter comprise the Capture Engine.

Timing and Control

Timing of the Capture Engine is derived from the Input Control Block which contains a series of counters and decoders synchronized to the A/D sample clock, ADCK. ADCK is derived from a phase locked loop referenced to the leading edge of horizontal sync.

Sync polarity is auto-detected by sensing the leading edge of horizontal sync HS and vertical sync, VS. This edge is the reference for the phase-locked loop tracking the horizontal pixel count and the vertical line counter.

Registers that interface with the Capture Timing and Control block are:

- IHS
- IHC (read only)
- IVC (read only)

Capture Control also coordinates hand off of data to the Frame Store Controller.

Input horizontal samples, IHS is the 10-bit terminal count of the number of pixels per horizontal line between sync pulses. IHS is the value programmed into the ADCK phase-locked-loop. If, for example there are to be 800 samples per incoming line, then IHS must be programmed to be 799.

Input horizontal count, IHC is the number of $4f_{SC}$ clock pulses (14.31818 MHz for NTSC; 17.734 MHz for PAL) that occur between horizontal sync pulses. This count is stored in the IHC register that can be read via the serial bus for automatic detection of the format of incoming video.

Input vertical count, IVC is the 10-bit terminal count of the number of lines that occur between the vertical sync pulses. This count is stored in the IVC register that can be read via the serial bus for automatic detection of the format of incoming video.

Clamps

Incoming RGB video signals must be AC coupled to the A/D converters. Preceding each A/D converter is an FET clamp switch which establishes the black reference level of each video signal by shorting the A/D converter input to ground when the clamp signal is active. Clamp timing is derived

internally from the HS input. A digital output, CLAMP which is HIGH when the clamp is active, may be used to drive clamp circuits preceding external A/D converters when the $R_{7-0}G_{7-0}B_{7-0}$ inputs are used.

Analog-to-Digital Converters

Setting the XA/D_SEL\ pin = H, selects the internal A/D converters with inputs RGB while the $R_{7-0}G_{7-0}B_{7-0}$ digital inputs become active outputs with undefined states. Bottom reference voltage of the A/D converters is ground. Top reference voltage, V_T is a high impedance input that is applied via voltage followers to the reference ladder network of each A/D converter. V_T must be de-coupled with a 0.1µF capacitor to ground.

A stable voltage source greater than the input peak amplitude must be connected to V_T. Nominal level of V_T is 0.75 volts, slightly above the nominal to allow a margin between incoming video levels and the conversion range. V_T can be derived from the internal reference voltage, V_{REF} by splitting the resistor connected to $_{RREF}$ as described in the Application Notes section.

To avoid aliasing effects, incoming RGB video signals should be filtered by a low pass filter prior to the AC coupling capacitor. Filter cutout frequency should be set at half the highest expected sampling rate of the A/D converter clock, ADCK. A simple two element RC filter is adequate.

Phase of ADCK is set by the Command Register FAZE bit. By flipping the phase of the sampling clock by 180°, the sampling points can be positioned closer to the center of incoming pixels. Figure 2 shows optimum sampling of VGA pixels on the rising edge of the ADCLK signal, when synchronous sampling is chosen.

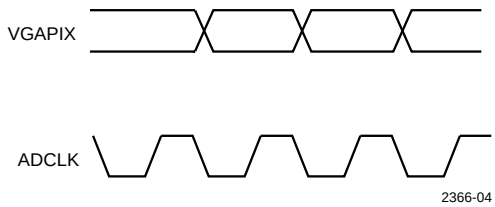


Figure 2. FAZE Sets ADCK Sampling Edge on Incoming Pixels

A/D converter power can be disconnected by setting the Command Register ADCOFF bit.

24-bit Digital RGB Port

Extra pins are included on the TMC2376KB package to incorporate a 24-bit TTL compatible RGB input port. Either analog or digital inputs can be selected by the level on the XA/DSEL\ pin. With the 24-bit RGB port enabled, incoming pixels may be derived directly from an external digital RGB source or from external analog RGB via triple 8-bit A/D converters

Internal Bit Pattern Generator

BiPGen is the internal Bit Pattern Generator which outputs a test pattern consisting of:

1. Color Bars
2. Gradient
3. Impulses

BiPGen is initialized at power up and can be selected by setting the BIPGEN bit in the Control Register, The pattern is set as shown in Figure 3.

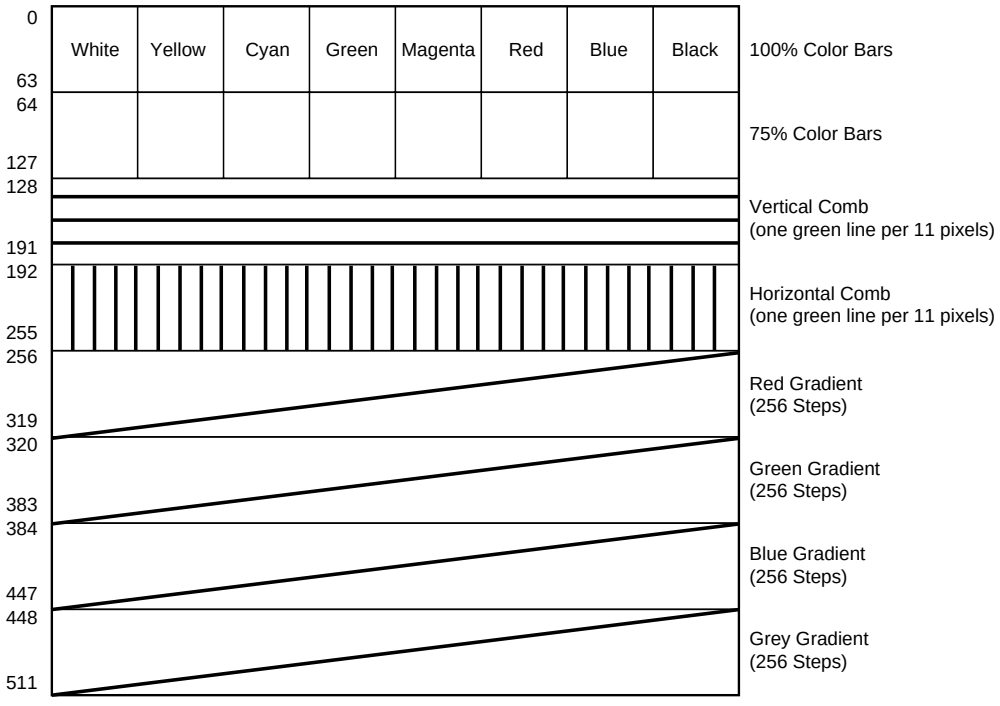


Figure 3. BiPGen Chart

The 512x512 chart is inserted into a 768x768 pixel frame, displaced 128 pixels from the left boundary and 128 pixels from the upper boundary. Color bars are each 64 pixels wide. BIPGEN pixels are clocked at half the rate of internal frame store clock, FSCK.

Digital RGB Multiplexer

The A/D_SEL pin in conjunction with the BIPGEN bit in the Command Register controls a triple 24-bit multiplexer that selects the source of RGB data to be supplied to the digital gain block. 24-bit RGB data can be accepted from:

- TTL compatible RGB input port
- A/D converter outputs
- BiPGen, the internal test pattern generator

RGB Gain

Following each A/D converter is a digital gain stage that allows the A/D converter to accommodate either 700 mV or 1000 mV RGB input video signals. Gain is set by the RGBGAIN bit of the Mode Register. When using RGBGAIN, V_T must be set to 1000 mV. Consequently, there is a slight loss in intensity quantization when the peak input level is 700 mV.

RGB/YUV Matrix

Pixels are converted from the 24-bit RGB format to the 24-bit YUV format by an RGB/YUV matrix. UV data is filtered and decimated prior to realignment with Y data form a 16-bit YUV422 data stream.

Command Register bit, UVALT determines the siting of UV samples relative to Y samples (see Figure 4). In the normal mode, each U and V sample pair corresponds to an even Y sample. In the alternating mode, U is sampled on even Y values and V is sampled on odd Y values. UVALT also impacts UV reconstruction in the Video Encoder Engine.

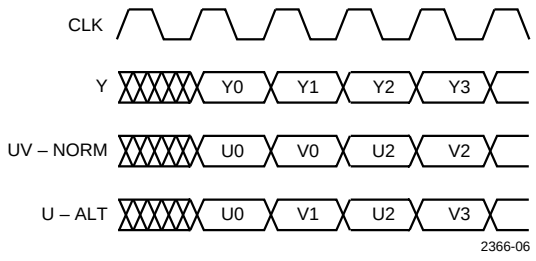


Figure 4. Siting of YUV samples determined by UVALT.

Vertical Scaler

16-bit YUV422 data from the Transcoder is passed to the Vertical Scaler which operates on columns of pixels. Vertical scale factor is set by programming the VSC registers (register numbers E and F). VSC is the Vertical Scale Coefficient, n which determines the vertical scaling factor:

VSF = (1 - n/64)

n is the reduction (caused by the scaling filter), modulo 64, in the number incoming vertical lines. With a range: $0 \le n \le 32$; $\_ \le VSF \le 1$.

Line stores used within the scaler are 768 pixels long.

Flicker Filter

Twitter artifacts occurring between odd and even video fields, can be eliminated by enabling the Flicker Filter. Filtering band-limits the spatial frequencies of columns of pixels to remove high frequency components of high/low luminance boundaries which cause flicker on an interlaced TV image.

Output of the filter is the weighted average of three consecutive lines incoming lines. Without the flicker filter, one contrasting VGA line can be encoded into one field of the TV video while adjacent lines are encoded onto the other field. Flicker frequency will be 30 Hz for NTSC and 25 Hz for PAL. With the flicker filter enabled, there is a slight smearing of the vertical definition.

Command Register Extended (0x14) bit 0, FLICKON programs the state of the flicker filter. With FLICKON = 1, 3-line filtering is activated. With FLICKON = 0, vertical filtering is bypassed.

Line stores used within the flicker filter are 768 pixels long.

Frame Store Controller

Pixel data transfer between the TMC2376 and the Frame buffer is coordinated by the Frame Store Controller (FSC). For normal operation, a 16 Mbit SDRAM is connected between to the frame store controller port. Supported SDRAM parts include:

NEC	µPD451616G5-A10
Samsung	KM416S1120A-G/F10
Toshiba	TC59S1616AFT-10A

Note that the Toshiba part with 64 msec. refresh period is more suitable for PAL applications using freeze frame and for 56 Hz incoming vertical refresh. Samsung and NEC parts have 32 msec. refresh.

Data from the Capture Engine is written into the frame store in parallel with extraction of data by the encoder engine is extracted. Read and write buffers at the data port allow data to be transferred in bursts without interruption of the overall flow of pixels. Bandwidth of the FSC bus is 80 MHz, sufficient to support maximum rate write cycles from the Capture Engine simultaneously with full rate Encoder Engine read cycles.

Pixel data format is YUV422. Bit assignments of consecutive 16-bit data words is shown in Figure 5.

15							8	7							0
C_{B7}	C_{B6}	C_{B5}	C_{B4}	C_{B3}	C_{B2}	C_{B1}	C_{B0}	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
C_{R7}	C_{R6}	C_{R5}	C_{R4}	C_{R3}	C_{R2}	C_{R1}	C_{R0}	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0

Figure 5. Frame Store Data Bus Format

SDRAM Interface

Within the Frame Store Controller are pixel buffers and arbitration logic that allow the alternate bursts of read and write cycles. Pixels are transferred between the TMC2376 and the Frame Buffer in 32-pixel length bursts.

Frame store control signals are passed to the SDRAM on the $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ A_{11-0} lines with data on D_{16-0}. Except for initialization $\overline{CS}$ = L. Memory Access timing is based upon a CAS latency of 3 and burst length of 8. In the burst mode, the SDRAM auto-increments its internal address pointer.

There are only three types of memory access:

- SDRAM Mode register setup.
- Burst write. (fourth CAS incorporates an auto-precharge cycle)
- Burst read. (fourth CAS incorporates an auto-precharge cycle)

SDRAM mode register setup is initiated by either power-up or by $\overline{RESET}$. Within the SDRAM, there are three fields which are setup, as shown in Figure 6.

OP_{4-0}					LT_2	LT_1	LT_0	WT	BL_2	BL_1	BL_0
0	0	0	0	0	0	1	1	0	0	1	1

Figure 6. SDRAM Mode register setup

BL_{2-0} = 3, sets the burst length to 8; WT = 0, establishes sequential addressing of the burst data. LT_{2-0} = 3, sets the CAS\ latency to 3. Option bits, OP_{4-0} = 0, to select the Mode Register Set operation. Timing of the mode register write operation is shown in Figure 7. When the $\overline{CS}$ = $\overline{RAS}$ = $\overline{CAS}$ = $\overline{WE}$ = L, the data on address bits A_{11-0} is stored in the SDRAM mode register.

A 32-pixel write cycle consists of four 8-pixel burst writes to the SDRAM. At the beginning of the write cycle shown in Figure 8, the data bus is tri-stated with $\overline{RAS}$ = $\overline{CAS}$ = $\overline{WE}$ = H. To start a 32-pixel burst write cycle, a row address, ar(m) is loaded by bringing $\overline{RAS}$ = L. Three clock cycles later, the column address ac(m) is loaded and the first pixel d(n) written by bringing $\overline{CAS}$ = $\overline{WE}$ = L.

After pixel d(n+7) has been written, $\overline{CAS}$ = $\overline{WE}$ = L to initiate the next 8-pixel burst. After 32 pixels have been written to the DRAM, the $\overline{RAS}$ and $\overline{CAS}$ cycles terminate and the data bus D[15:0] is tri-stated.

During the 32-pixel burst, outgoing write addresses increment every clock cycle. Because $\overline{RAS}$ = $\overline{CAS}$ = H, the address is ignored by the SDRAM.

Figure 10 shows a complete 32 pixel write cycle starting with $\overline{RAS}$ = L. Next follow four $\overline{CAS}$ = L strobes while 32 pixels are stored in memory. Finally, an auto pre-charge command is issued by address bit A10 = H for the last $\overline{CAS}$ strobe.

A typical read cycle, as shown in Figure 9, is similar to the write cycle. The difference is that during a read cycle, $\overline{WE}$ = H when $\overline{CAS}$ = L. A 32-pixel read cycle will normally be preceded by a write cycle and occasionally be preceded by a read cycle.

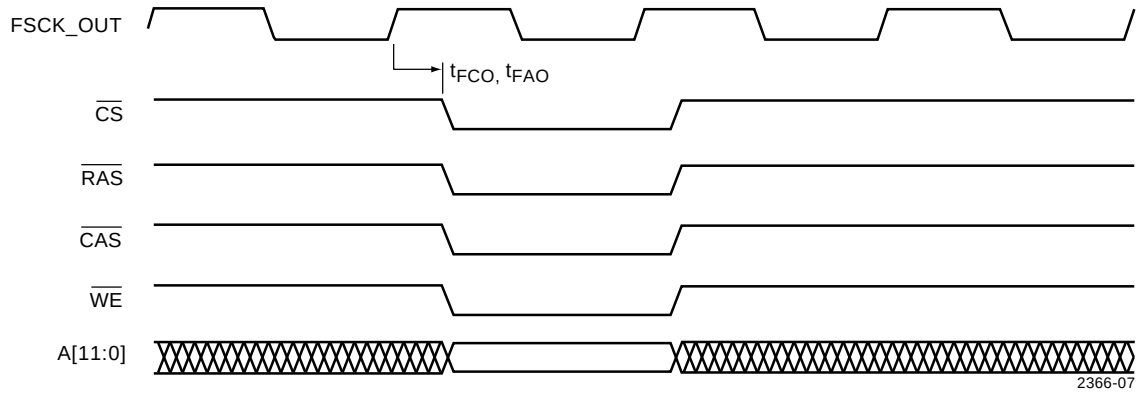


Figure 7. Frame Store Mode Register Write Timing

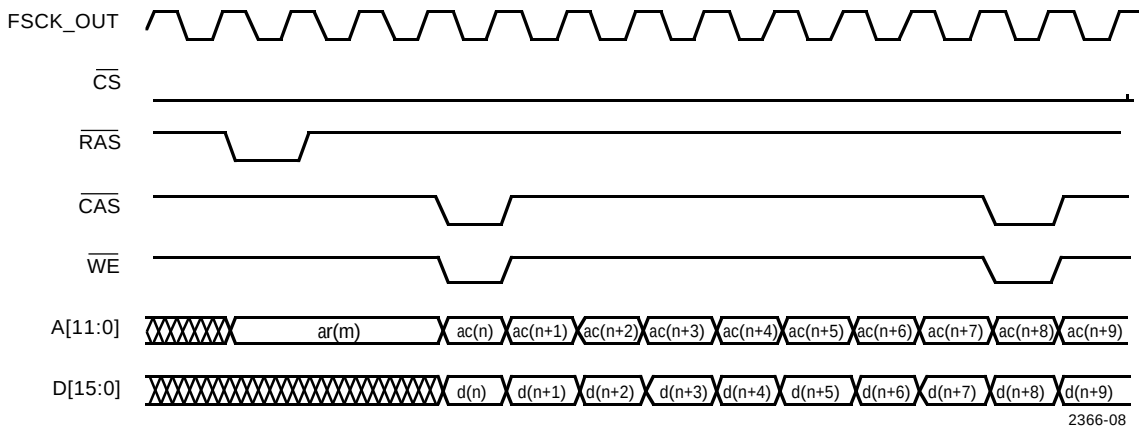


Figure 8. Frame Store Data Write Timing

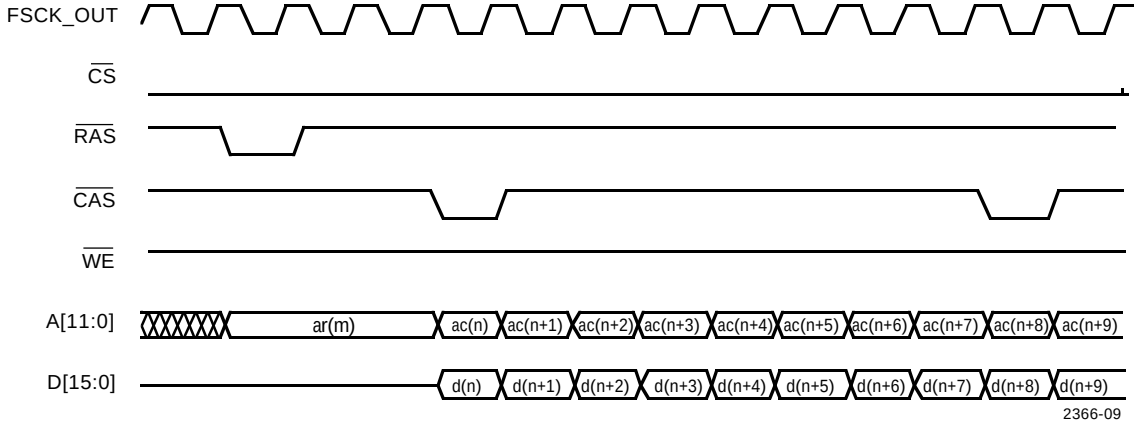


Figure 9. Frame Store Data Read Timing

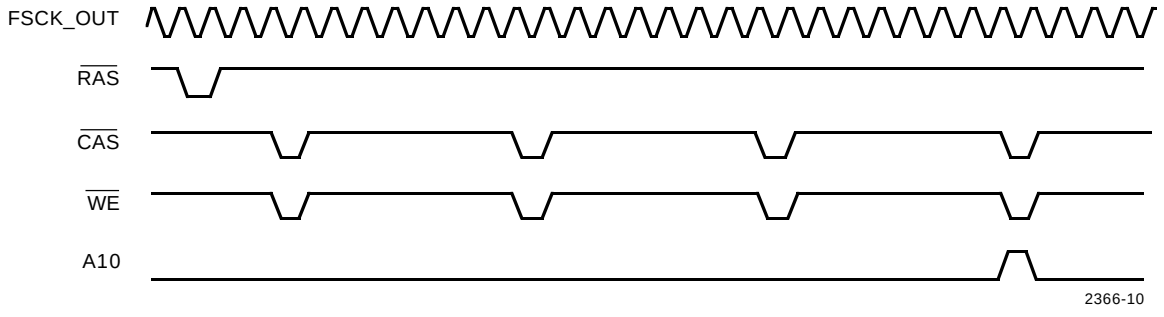


Figure 10. Frame Store Write Cycle with Auto Precharge

Preliminary Information

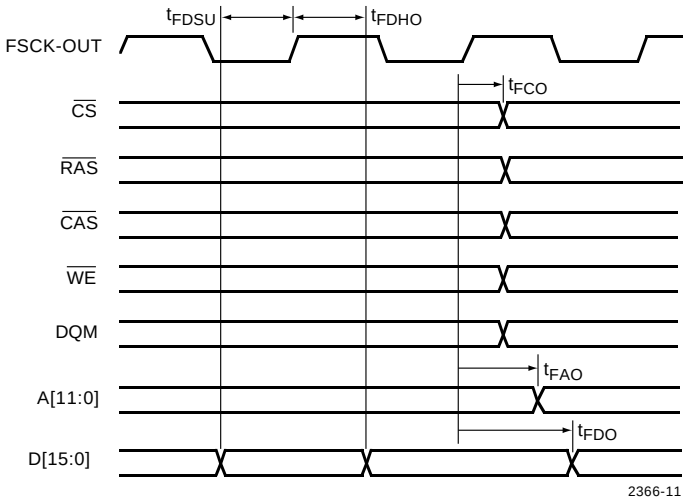


Figure 11. Timing Parameter Definition, SDRAM Interface

Phase Locked Loop

All SDRAM access is synchronized to the selected $4f_{SC}$ clock derived from the CKNTSC clock input. The $4f_{SC}$ clock is divided by two, then depending upon the outgoing video standard selection, either NTSC or PAL, multiplied x9 or x11 by the Frame Store Controller Phase Locked Loop to create the 80 MHz SDRAM clock, FSCK

FSCKXSEL\ selects either internal clock, FSCK or external input FSCK_IN which should have a frequency of 80 MHz to accomodate high resolution images (1024x768) refreshed at high rates (75 Hz) converted to the PAL format (17.73 MHz $4f_{SC}$ clock).

Input Offset and Size Control

Besides synchronizing all SDRAM access activities, the frame store controller also coordinates several offset and size functions. These values are programmed into internal registers that control the setup of the Frame Store Controller.

Input horizontal offset, IHO is a ten bit value that sets the horizontal displacement of the captured active video relative to the horizontal sync as show in Figure 12.

Input vertical offset, IVO is a ten bit value that sets the vertical displacement of the captured active video relative to the vertical sync as show in Figure 12.

Input horizontal active width, IHAW is the 10-bit terminal count of the number of horizontal pixels to be inserted into frame store memory. (see Figure 12)

Input lines sampled, ILS is the 10-bit terminal count of the number of lines to be inserted into frame store memory following vertical scaling. (see Figure 12)

Output Offset and Size Control

Synchronization and timing of outgoing video pixel data is predetermined by the selection of the video format. However, the location of the active video area must be selected by programming the offset registers. Leading edges of outgoing horizontal and vertical sync define the dimensions of the outgoing frame as shown in Figure 13. Offsets OVO and OHO define the position of the active video area within the outgoing frame.

Output horizontal offset, IHO is the 8-bit terminal count of the horizontal displacement of the outgoing active video in pixels relative to the leading edge of horizontal sync. (see Figure 13)

Output vertical offset, IVO is the 8-bit terminal count of the vertical displacement of the outgoing active video in pixels relative to the beginning of vertical sync equalization pulses. (see Figure 13)

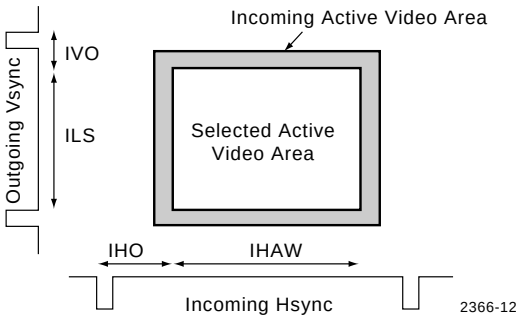


Figure 12. Input Offset and Size Definitions

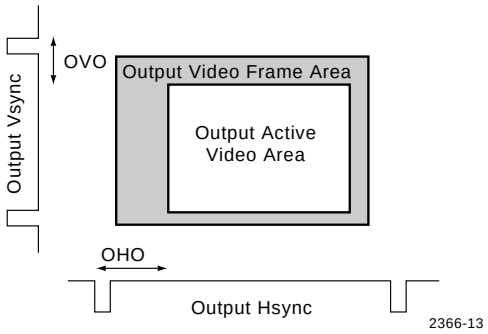


Figure 13. Output Horizontal and Vertical Offset Definitions

Freeze Frame

Writing to the Frame Store can be interrupted by setting the FRZ bit of the Mode Register. Capture will continue until the end of the current frame.

Zoom

When zoom is activated by setting the ZOOM bit to 1 in the Command Register, pixels are 2X replicated in the vertical and the horizontal directions. Pixels are replicated vertically by the Capture Engine which duplicates the loading of each line into the Frame Store. If, for example, only 120 separate lines are accepted, then 240 lines are written to each field contained the Frame Store Memory. When the zoomed frame segment is retrieved, the number of horizontal pixels is doubled by duplicating each pixel twice as the pixels are read from the Frame Store Memory.

Offset may be applied to a zoomed image through the IHO and IVO registers as shown in Figure 14

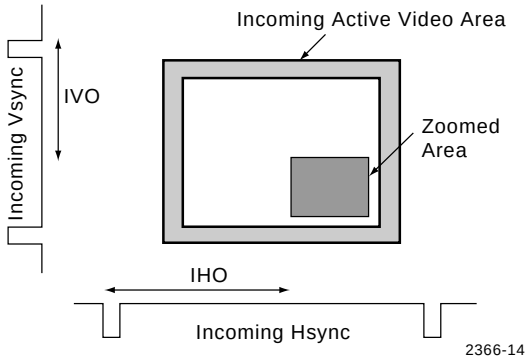


Figure 14. Zoomed image showing offsets

Encoder Engine

All blocks following the frame store controller through to the D/A converters are included in the encoder engine which produces CVBS, Y/C, RGB and YUV formats with PAL or NTSC timing.

Outgoing TV Formats

Table 3, Table 4 and Table 5 show the Horizontal and Vertical Timing for the NTSC and PAL TV formats.

Horizontal timing parameters: front porch, back porch and active video pixel counts are set by OHO, IHAW and HSC. Input horizontal active width (IHAW) combined with the horizontal scaling coefficient (HSC) sets the width of the active video in pixels. OHO sets the offset of the active video from the leading edge of sync, corresponding to the front porch. With the active video and the front porch pixel counts defined, the pixel count of the back porch follows.

Vertical timing parameters: vertical front porch, back porch and active video pixel counts are set by the OVO and ILS register values. Input lines stored, the ILS register value sets the number of incoming lines stored per field, defining the number of lines within the vertical active video output. Output vertical offset, OVO establishes the displacement of the active lines from the vertical sync, defining the front porch and in conjunction with ILS and the selected output format, the back porch.

Table 3. NTSC and PAL Frequencies

Television Standard	Field Rate (Hz)	Lines Per Frame	Line Rate (kHz)	Pixel Rate (MHz)	f_{sc} (MHz)
NTSC	59.94	525	15.734	14.31818	3.579
PAL	50.00	625	15.625	17.734475	4.433

Table 4. NTSC and PAL $4f_{SC}$ Clock Counts

Television Standard	Front Porch	Horizontal Sync	Breezeway	Burst	Color Back Porch	Active Video	Line
NTSC	18	67	5	43	10	767	910
PAL	22	84	6	54	12	957	1135

Table 5. NTSC and PAL Vertical Timing

Television Standard	Field Rate (Hz)	Lines Per Frame	Line Rate (kHz)	Front Porch (lines)	Vertical Sync (lines)	Back Porch (lines)	Active Video (lines/field)
NTSC	59.94	525	15.734	3-3.5	3	14-14.5	242.5
PAL	50.00	625	15.625	2.5	2.5	21	286.5

Timing and Control

Timing of the Encoder Engine is Synchronized by the Encoder Timing and Control Block. Frame store clock, FS_CK is derived from the CKNTSC clock by the FSCK phase locked loop.

Either of two 4x subcarrier clocks can be selected to synchronize the Encoder Engine. Frequencies are:

- CKNTSC: 14.31818 MHz for NTSC.
- CKPAL: 17.734475 MHz for PAL.

A clock signal must always be applied to the 4x NTSC clock input, CKNTSC. Depending upon the outgoing TV standard requirements, one of three possible clock combinations can be selected as depicted in Table 6.

Table 6. 4x Clock Connections

TV Standard	CKNTSC	CKPAL
NTSC and PAL	✓	✓
NTSC only	✓	N/A
PAL only	Connect to CKPAL	✓

Horizontal Scaler

Pixels extracted from the external frame store memory are passed to the Horizontal Scaler by the Frame Store Controller.

Horizontal scale factor is set by programming the HSC registers (register no.'s 0x24 and 0x25). HSC is the Horizontal scaling coefficient, m that determines the horizontal scaling factor:

$HSF = (1 + m/64)$

With a range: $0 \le m \le 63$; $1 \le HSF \le 1 + 63/64$

Digital Video Encoder

For CVBS and Y/C outputs, pixels from the Horizontal Scaler are routed to the Video Encoder. NTSC (SMPTE 170M) and PAL (CCIR 624) standards are preprogrammed into the Video Encoder to preset horizontal and vertical timing, subcarrier frequency, and chrominance phase.

Setting the Command Register $DACFMT_{1-0}$ bits to 00 selects CVBS and Y/C outputs. Mode register bit 1 PAL/NTSC selects either PAL or NTSC timing.

Mode Register bit, CBPF inserts a 18% (0.64 MHz for NTSC; 0.8 MHz for PAL) f_{SC} bandpass filter centered at f_{SC} following the chroma modulator.

Mode Register bit, LUMNTCH insert a luminance notch filter in the Y channel prior to the CVBS summer and the Y output.

Mode Register Extended bit, OCS set the gain of the U and V channels prior to the chroma modulator.

YUV/RGB Matrix

For RGB outputs, pixels from the Horizontal Scaler are routed to the YUV/RGB matrix. Matrix coefficients are programmed by setting the $DACFMT_{1-0}$ bits in the Mode register. For a YUV output, the $DACFMT_{1-0}$ bits can be set to bypass the YUV/RGB matrix.

Digital-to-Analog Converters

Three 9-bit D/A converters accept data from either the video encoder or the YUV-to-RGB transcoder. Each output is a current source connected to the analog V_{DDDA} supply. Current is injected into external resistor to develop the output voltage. Typically the DC load is 37.5Ω formed from two 75Ω resistors and a low pass filter. A 75Ω load may be selected to minimize power dissipation.

Peak output current of the D/A converters is established by V_{REF} and an external resistor connected between R_{REF} and ground. Peak current is six times the current through the reference resistor.

An internal 1.235 volt reference is buffered from V_{REF} by a resistor, to enable V_{REF} to be overridden by an external voltage. Output current may be calibrated by resistor selection or by setting a potentiometer attached to R_{REF}.

For 1.3 volt video, with a 37.5Ω load, the correct value of R_{REF} is 392Ω. With a 75Ω load, the correct value of R_{REF} is 768Ω. See applications circuits.

To minimize DAC noise, a bypass capacitor must be connected from C_{BYPR} to an adjacent V_{DDDA} pin.

Power may be conserved by disabling the power supplied to unused D/A converters. Mode Register bit CVBSOFF controls CVBS D/A converter power. Mode Register bit YCOFF controls Y/C D/A converter.

Serial Control Port (R-Bus)

All TMC2376 register access is via a 2-wire serial control interface. Either 7 or 10-bit addressing may be used with two addresses available for each type of addressing scheme. (see Table 7)

Two signals comprise the bus: clock (SCL) and bi-directional data (SDA). The TMC2376 acts as a slave for receiving and transmitting data over the serial interface.

Data received or transmitted on the SDA line must be stable for the duration of the positive-going SCL pulse. Data on SDA may change only when SCL = L. An SDA transition while SCL = H is interpreted as a start or stop signal.

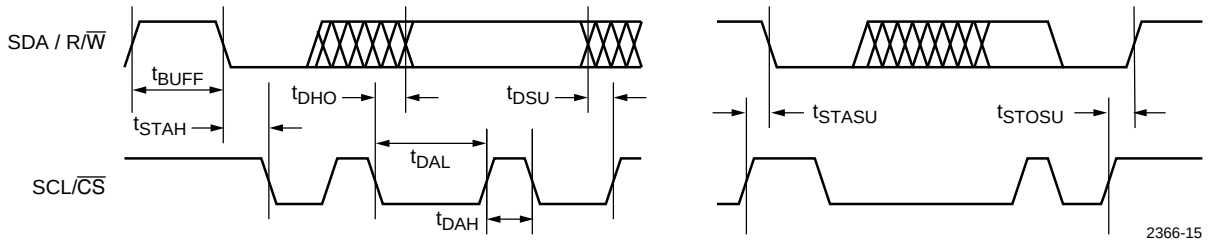


Figure 15. Serial Port Read/Write Timing

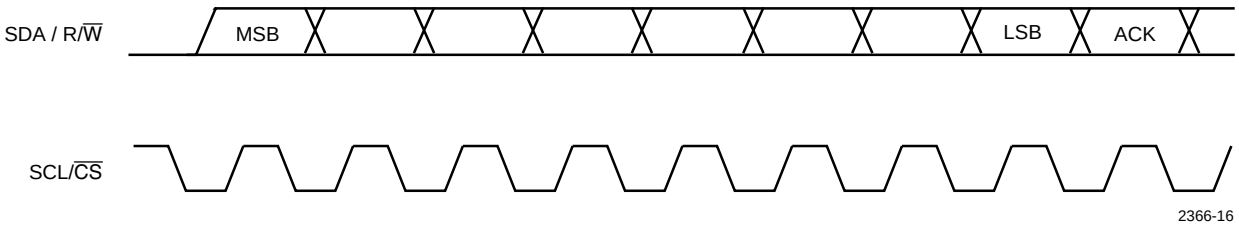


Figure 16. Serial Interface – Typical Byte Transfer

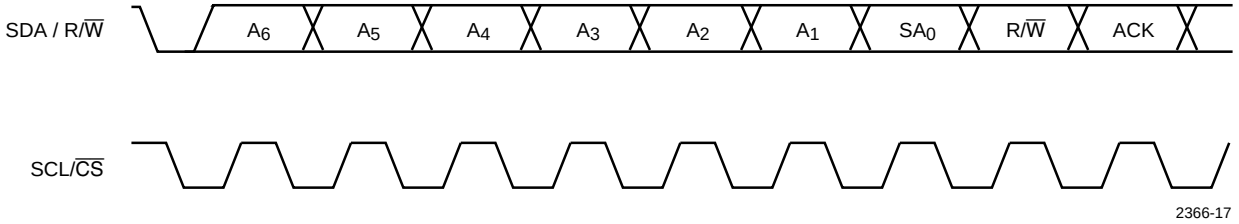


Figure 17. 7-bit Slave Address with Read/Write\ Bit

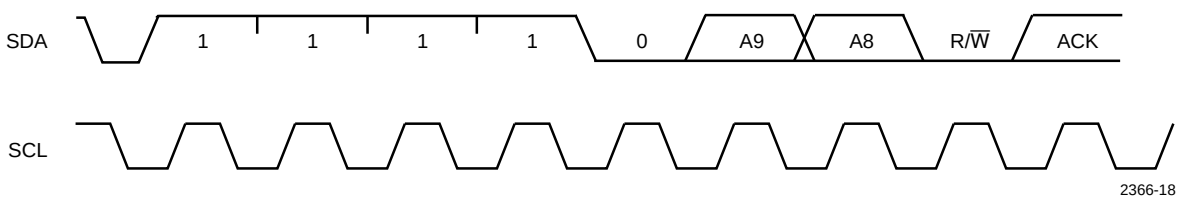


Figure 18. 10-bit address transfer, upper two bits

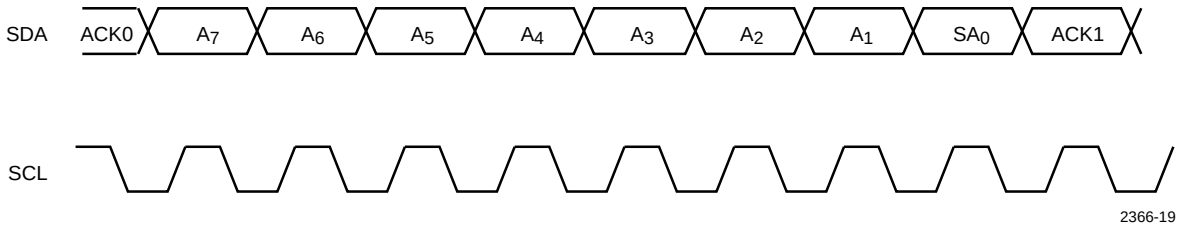


Figure 19. 10-bit address transfer, lower eight bits

There are five steps within a serial bus cycle:

1. Start signal
2. Slave address byte
3. Pointer register address byte
4. Data byte to read or write
5. Stop signal

When the serial interface is inactive (SCL = H and SDA = H) communications are initiated by sending a start signal. The start signal (Figure 15, left waveform) is a HIGH-to-LOW transition on SDA while SCL is HIGH. This signal alerts all slaved devices that a data transfer sequence is imminent.

For 7-bit addressing, the first eight bits of data transferred after a start signal comprise a seven bit slave address and a single R/W bit (Read = H, Write = L). As shown in *Figure 16*, the R/W bit indicates the direction of data transfer, read from or write to the slave device. If the transmitted slave address matches the address of the TMC2376 (set by the state of the SA_0 and $SA_{10/7}$ input pins in Table 7.), the TMC2376 acknowledges by bringing SDA LOW on the 9th SCL pulse (see Figure 17). If the addresses do not match, the TMC2376 does not acknowledge.

With 10-bit addressing (see Figure 19 and Figure 19), data is still transferred in 8-bit chunks. The upper two bits of the ten bit address are transferred as the lower two bits of the first byte along with the reserved sequence 11110 in the upper five bits and the R/W bit. The lower eight bits are transferred in the second byte without a R/W bit. Subsequent data reads or writes follow the 7-bit transfer sequences.

For each byte of data read or written, the MSB is the first bit of the sequence.

Table 7. Serial Port Addresses

$SA_{10/7}$	SA_0	Address (Hex)
1	1	4A
1	0	6A
0	1	224
0	0	276

Data Transfer via Serial Interface

If a slave device, such as the TMC2376 does not acknowledge the master device during a write sequence, SDA remains HIGH so the master can generate a stop signal. If the master device does not acknowledge (ACK = L) the TMC2376 during a read sequence, the TMC2376 interprets this as “end of data.” SDA remains HIGH so the master can generate a stop signal.

To write data to a specific TMC2376 control register, first the slave address must be established by sending the slave address byte. Next, the 8-bit pointer must be loaded with the address of the target control register which is the base address for subsequent write operations. Finally, the data bytes are written, two bytes for each 10-bit register. After each control register data transfer, the pointer address auto-increments. If the number of bytes transferred exceeds the number of pointer addresses, the pointer will not be incremented, instead remaining at the final register value of 25 hex while an acknowledge singal, ACK is sent.

Data is read from the control registers of the TMC2376 in a similar manner, except that two data transfer operations are required:

1. Write the slave address byte with bit R/W = L.
2. Write the pointer byte.
3. Write the slave address byte with bit R/W = H.
4. Read the control register indexed by the pointer.

Preceding each slave write, there must be a start cycle. Following the pointer byte there should be a stop cycle. Sequential registers may be accessed by repeated read cycles since pointer auto-increments after each byte transfer. After the last read, there must be a stop cycle comprising a LOW-to-HIGH transition of SDA while SCL is HIGH. (see *Figure 15*, right waveform)

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read, write) between the slave and master without releasing the serial interface lines.

Serial Interface Read/Write Examples

Examples below show how serial bus cycles can be linked together for multiple register read and write access cycles. For sequential register accesses, each ACK handshake initiates further SCL clock cycles from the master to transfer the next data byte.

Write to one 10-bit control register (two consecutive 8-bit writes)

- Start signal
- Slave Address byte (R/$\overline{W}$ bit = LOW)
- Pointer Address byte
- Lower data byte to register
- Upper data byte to register (pointer address +1)
- Stop signal

Read from one 10-bit control register (two consecutive 8-bit reads) control register

- Start signal
- Slave Address byte (R/$\overline{W}$ bit = LOW)
- Pointer Address byte
- Stop signal
- Start signal
- Slave Address byte (R/W bit = HIGH)
- Lower data byte from pointer address
- Upper byte from (pointer address + 1)
- No acknowledge (terminates data transfer by TMC2376)

Equivalent Circuits

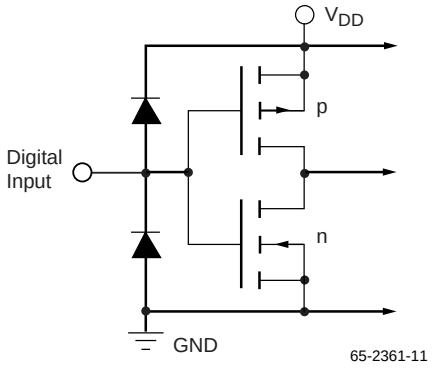


Figure 20. Equivalent Digital Input Circuit

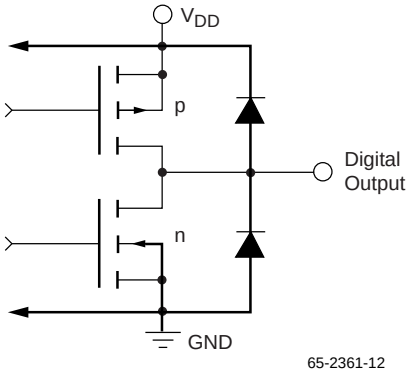


Figure 21. Equivalent Digital Output Circuit

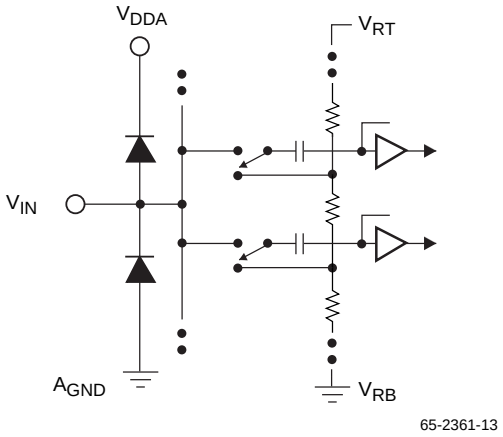


Figure 22. Equivalent A/D Input Circuit

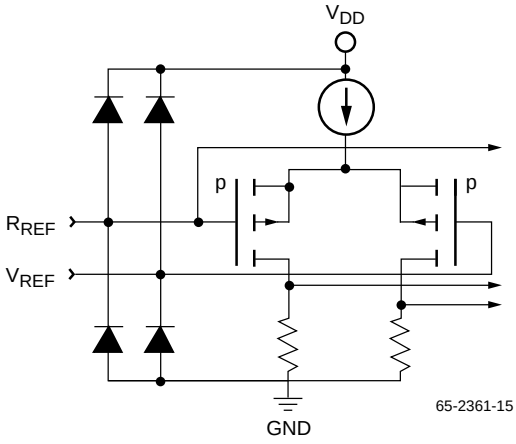


Figure 23. Equivalent D/A Reference Input Circuit

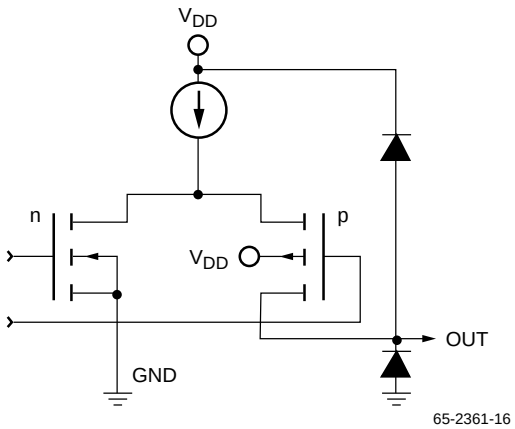


Figure 24. Equivalent D/A Output Circuit

Preliminary Information

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Unit
Power Supply Voltages				
V_{DD3} (Measured to V_{SS3})	-0.5	3.3	4.6	V
V_{DD5} (Measured to V_{SS5})	-0.5		7.0	V
V_{DDAD} (Measured to V_{SSAD})	-0.5		7.0	V
V_{DDPA} and V_{DDPF} (Measured to V_{SSPA} and V_{SSPF})	-0.5		0.5	V
V_{DDDA} (Measured to V_{SSDA})	-0.5		7.0	V
V_{SSAD}, V_{SSPA}, V_{SS3}, V_{SSPA}, V_{SS5}, V_{SSDA} (delta)	-0.5		0.5	V
Digital Inputs				
3.3 V logic applied voltage (Measured to V_{SS3})[2]	-0.5		V_{DD3} + 0.5	V
5 V logic applied voltage (Measured to V_{SS5})[2]	-0.5		V_{DD5} + 0.5	V
Forced current [3, 4]	-10.0		10.0	mA
Analog Inputs				
Applied Voltage (Measured to V_{SSAD})[2]	-0.5		V_{DDA} + 0.5	V
Forced current [3, 4]	-10.0		10.0	mA
Digital Outputs				
3.3 V logic applied voltage (Measured to V_{SS3})[2]	-0.5		V_{DD3} + 0.5	V
5 V logic applied voltage (Measured to V_{SS5})[2]	-0.5		V_{DD5} + 0.5	V
Forced current [3, 4]	-6.0		6.0	mA
Short circuit duration (single output in HIGH state to ground)			1	sec.
Temperature				
Junction			150	°C
Lead Soldering (10 seconds)			300	°C
Vapor Phase Soldering (1 minute)			220	°C
Storage	-65		150	°C
Electrostatic Discharge[5]			±150	V

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.
5. EIAJ test method.

Operating Conditions

Parameter		Min	Nom	Max	Units
V_{DD3}	Digital Power Supply Voltage	3.15	3.3	3.45	V
V_{DD5}	Digital Power Supply Voltage	4.75	5.0	5.25	V
V_{DDAD}, V_{DDDA}	A/D and D/A Supply Voltage	4.75	5.0	5.25	V
V_{DDPA}, V_{DDPF}	PLLs Supply Voltage	4.75	5.0	5.25	V
A_{GND}	Analog Ground (Measured to D_{GND})	-0.1	0	0.1	V
V_{RT}	Reference Voltage, Top	0.5	0.75	2.0	V
V_{IN}	Analog Input Range	0		VRT	V
V_{REF}	External Reference Voltage		1.235		V
I_{REF}	D/A Converter Reference Current ($I_{REF} = V_{REF}/R_{REF}$, flowing out of the R_{REF} pin)		3.15		mA
R_{REF}	Reference Resistor, V_{REF} = Nom		392		Ω
R_L	DAC Total Output Load Resistance		37.5		Ω
T_A	Ambient Temperature, Still Air	0		70	°C
f_{CKIN_N}	NTSC reference Clock Frequency		14.31818		MHz
f_{CKIN_P}	PAL reference Clock Frequency		17.734475		MHz

Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
Power Supply Currents						
I_{DD3}	3.3 volt current	FSCK_IN = 80 MHz ADXCK = 40 MHz CKNTSC = 20 MHz		7		mA
I_{DDD5}	5 volt digital current			310		mA
I_{DDDA}	5 volt analog current			160		mA
I_{DDT}	5 volt total current			480	600	mA
Digital Inputs and Outputs						
C_I	Input Capacitance			5	10	pF
C_O	Output Capacitance			10		pF
I_{IH}	Input Current, HIGH	V_{DD3} and V_{DD5} = max., V_{IN} = max.			±10	µA
I_{IL}	Input Current, LOW	V_{DD3} and V_{DD5} = max., V_{IN} = 0 V			±200	µA
I_{ILP}	Input Current, LOW with pull-up	V_{DD3} and V_{DD5} = max., V_{IN} = 0 V	-100			µA
V_{IHTTL}	Input Voltage, Logic HIGH (TTL)		2.0			V
V_{ILTTL}	Input Voltage, Logic LOW (TTL)				0.8	V
V_{IHCK}	Input Voltage, Logic HIGH (clocks)	ADXCK, CKNTSC, CKPAL AND FSCK_IN PINS	2.0			V
V_{ILCK}	Input Voltage, Logic LOW (clocks)			1.2		V
I_{OH}	Output Current, Logic HIGH (V_{DD3} and V_{DD5})				-2.0	mA
I_{OL}	Output Current, Logic LOW (V_{DD3} and V_{DD5})				2.0	mA
V_{OH3}	Output Voltage, HIGH (V_{DD3})	I_{OH} = -2mA	2.4			V
V_{OL3}	Output Voltage, LOW (V_{DD3})	I_{OL} = 2mA			0.4	V
V_{OH5}	Output Voltage, HIGH (V_{DD5})	I_{OH} = -2mA	2.4			V
V_{OL5}	Output Voltage, LOW (V_{DD5})	I_{OL} = 2mA			0.4	V
Analog Inputs						
C_{AI}	A/D Input Capacitance	ADCLK = LOW ADCLK = HIGH		4 12		pF pF
R_{IN}	A/D Input Resistance[1]		500	1000		KΩ
I_{CB}	A/D Input Current				±15	µA
V_{RO}	Voltage Reference Output	Internal Reference	1.100	1.235	1.482	V
I_{RO}	VREF Output Current[1]	External V_{REF}	-150		+150	µA
Analog Outputs						
V_{OC}	Video Output Compliance		-0.4		2	V
R_{OUT}	Video Output Resistance[1]			15		KΩ
C_{OUT}	Video Output Capacitance[1]	I_{OUT} = 0 mA Freq. = 1 MHz		15		pF
I_{OS}	Short-Circuit Current[1]		-20		-80	mA

Notes:

1.Typical per design.

Switching Characteristics

Parameter		Conditions	Min	Typ[1]	Max	Unit
Clocks						
f_{XTOL}	Reference Clock Frequency Tolerance			50	50[1]	ppm
t_{PWH}	Reference Clock Pulse Width, HIGH			40		ns
t_{PWL}	Reference Clock Pulse Width, LOW			40		ns
Incoming Syncs						
f_H	HS_IN frequency		25		75	KHz
f_V	VS_IN frequency		50		90	Hz
N_H	Number of lines per frame		400		850	
t_{PWHS}	HS_IN Pulsewidth		1			µs
t_{VS-HS}	VS_IN to HS_IN Delay		0			ns
Video Output						
t_{DOV}	Analog Output Delay ($4f_{SC}$ clock to Video Out)				30	ns
t_R	D/A Output Current Risetime (10% to 90%)				10	ns
t_F	D/A Output Current Falltime (90% to 10%)				10	ns
SKEW	D/A to D/A Skew		-3	0	3	ns
SDRAM Frame Buffer Interface						
t_{FCKL}	FS_CK out pulse width, LOW		5.0			ns
t_{FCKH}	FS_CK out pulse width, HIGH		5.0			ns
t_{FSCO}	FS_CK out to $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ $\overline{DQM}$ out delay		2.0			ns
t_{FDSU}	FS_CK out to data in setup time		3.0			ns
t_{FDHO}	FS_CK out to data in hold time		3.0			ns
t_{FDO}	FS_CK out to data out delay		2.0			ns
t_{FAO}	FS_CK out to address out delay		2.0			ns
Serial Microprocessor Interface						
t_{DAL}	SCL Pulse Width, LOW			1.3		µs
t_{DAH}	SCL Pulse Width, HIGH			0.6		µs
t_{STAH}	SDA Start Hold Time			0.6		µs
t_{STASU}	SCL to SDA Setup Time (Stop)			0.6		µs
t_{STOSU}	SCL to SDA Setup Time (Start)			0.6		µs
t_{BUFF}	SDA Stop Hold Time Setup			1.3		µs
t_{DSU}	SDA to SCL Data Setup Time			300		ns
t_{DHO}	SDA to SCL Data Hold Time			300		ns

Notes:

1. Values shown in Typ column are typical for $V_{DD5} = V_{DDA} = +5V$, $V_{DD3} = +3.3V$ and TA = 25_C.
2. TV subcarrier acceptance band is ± 300 Hz.

Preliminary Information

System Performance Characteristics

Parameter		Conditions	Min	Typ[1]	Max	Unit
A/D Converter Input						
E_{LI}	A/D Integral Linearity Error, Independent	V_{RT} = 0.7V		±1		LSB
E_{LD}	A/D Differential Linearity Error	V_{RT} = 0.7V		±1		LSB
E_{OT}	Offset Voltage, Top	$V_{RT} - V_{IN}$ for most positive code transition		150		mV
E_{OB}	Offset Voltage, Bottom	V_{IN} for most negative code transition		150		mV
D/A Converter Output						
RES	D/A Converter Resolution		9	9	9	Bits

Notes:

1. Values shown in Typ column are typical for $V_{DD5} = V_{DDA}$ = +5V, V_{DD3} = +3.3V and TA = 25∞C.

Applications Information

Design Example–PC

Figure 27 is a reference schematic for the TMC2376. RGB video signals and the vertical and horizontal sync signals are intercepted by tapping connections to the VGA connector. Typically, control of the TMC2376 will be through the serial interface. S-video and CVBS outputs are fed to connector that should be located at the board edge. Power is derived from 5 volt analog, 3.3 digital 5 volt digital supplies. It is recommended that the analog supply be clean of noise.

A 17.73 MHz PAL oscillator is shown with connection to the CKNTSC input to provide the necessary internal clock. For NTSC, this oscillator can be replaced with a 14.318 MHz oscillator. Systems needing both NTSC and PAL should be set up with separate PAL and NTSC oscillators connected to the CKIN_N and CKIN_P pins; or crystals with appropriate capacitors connected between the CKIN_N and CKOUT_N pins and CKIN_P and CKOUT_P pins.

Input impedance of the A/D converters exceeds 500K and will not load VGA RGB lines. Shunt 47 pF capacitors and 274Ω series resistors form a low pass filter with 12 MHz cut-off. Filtering the incoming video has two functions:

- equalizing the intensities of vertical lines
- eliminating sampling noise.

Outgoing video is filtered by low pass Bessel filters with 10 MHz cutoff. An optional low pass filter has two functions:

- removal of steps from the CVBS output
- limiting the bandwidth of outgoing video.

For higher definition of horizontal frequencies, a sinx/x correction filter should be incorporated to compensate for 2 dB sampling loss of the D/A converters. Schottky diode clamps protect the TMC2376 from high voltage transients.

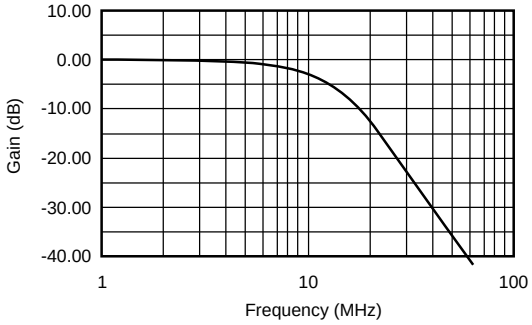


Figure 25. Video Filter Response

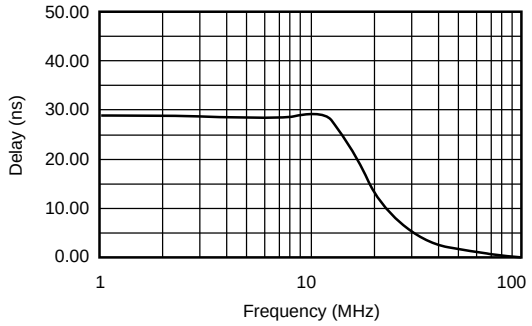


Figure 26. Video Filter Delay

V_{TIN} is derived from the bias voltage across R_{REF} which is established by the internal reference voltage available at V_{REF}. R_{REF} is split into two resistors with series resistance to set the R_{REF} current and ratio to establish the V_{TIN} voltage.

Design Example - TV

By interfacing the TMC2376 circuit shown in Figure 27 with the microcontroller circuit shown in Figure 28 is a TV reference design TV reference design can be created. With this design, many PC VGA or MAC formats can be automatically detected by firmware resident in the 8051 microcontroller to enable the TMC2376 to be programmed with the correct register values for correct scaling and centering.

Only the RGB output is needed to directly drive the CRT via the TV video amplifiers. Separate composite sync is fed to the TV synchronization circuits that drive the horizontal and vertical deflection circuits. The optional 10 MHz low pass filters at the output are not required.

Preliminary Information

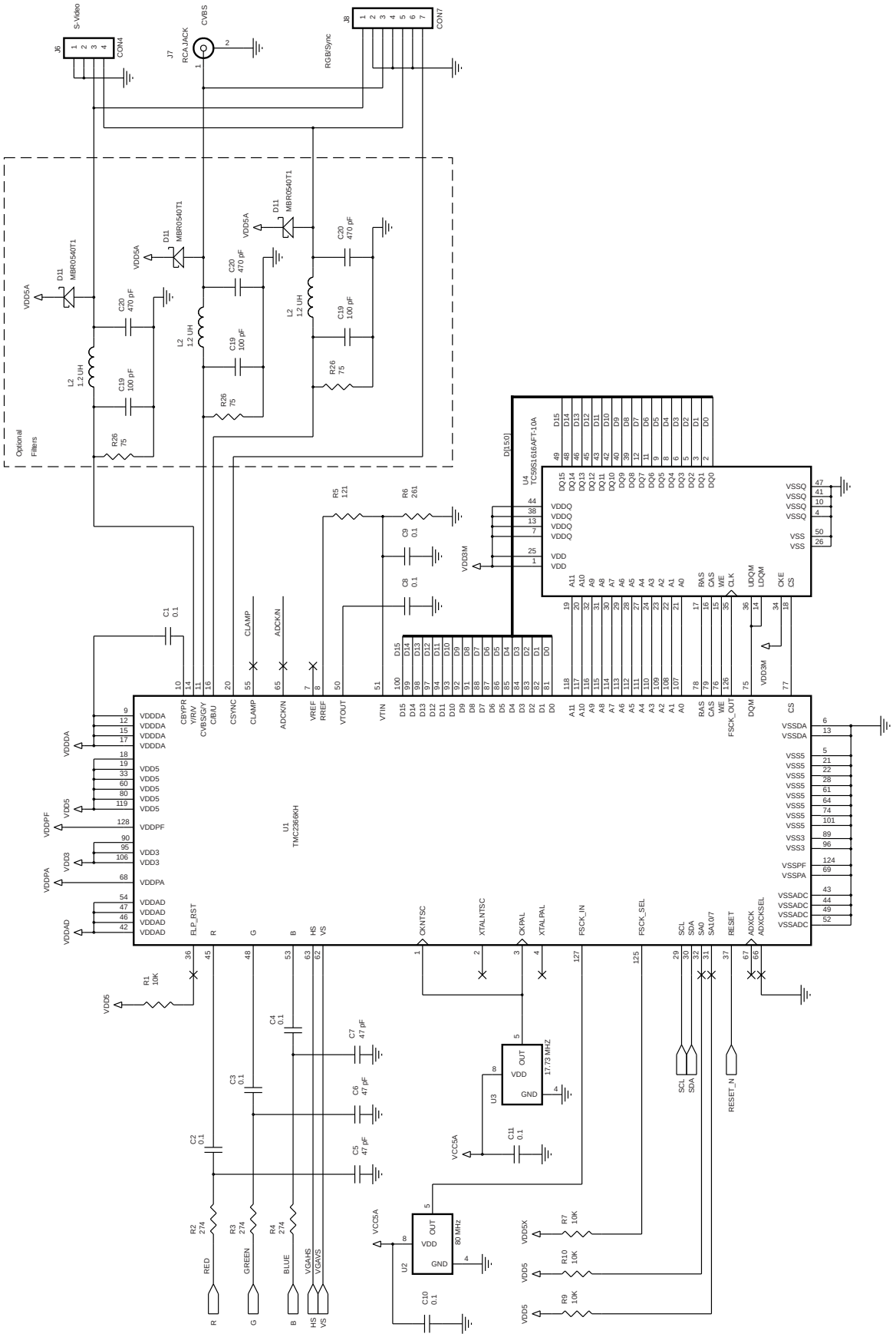


Figure 27. TMC2376 Schematic, Reference Configuration

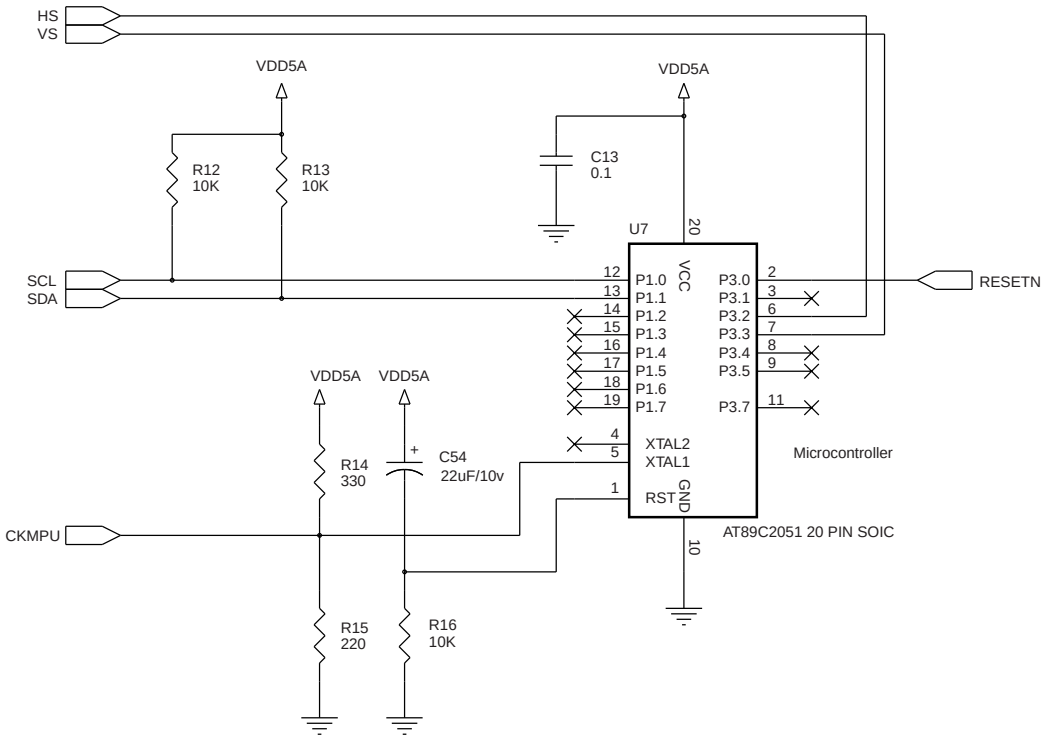


Figure 28. Reference Schematic, Microcontroller

Power and Ground

Within the TMC2376, separate power is routed to functional sections: A/D converters, phase locked loops, D/A converters, digital processors and digital drivers. To minimize power consumption, a 3.3 volt supply is used for the external SDRAM interface and the internal line buffers. All ground pins should be connected to a common ground plane. Power pins should be segregated into analog and digital sections.

Clean analog power should be applied to the V_{DDAD}, V_{DDPA}, V_{DDPF}, and V_{DDDA} pins. A 0.1 µF capacitor should be placed adjacent to each group of pins. The capacitor connected to C_{BYPR} is critical, it must be connected to V_{DDDA} to minimize noise at the D/A converter outputs. Chip capacitors are recommended.

Figure 29 depicts the strategy for distributing power. 5 volt power for the analog and digital sctions is drived from a common source. Filtered analog power is applied to the V_{DDAD}, V_{DDPA}, V_{DDPF}, and V_{DDDA} pins. A 0.1µF capacitor is placed adjacent to each group of pins. The capacitor connected to C_{BYPR} is critical, it must be connected to V_{DDDA} to minimize noise at the D/A converter outputs. Chip capacitors are recommended.

PLL power and ground implementation is critical to minimize clock jitter. Ensure that:

1. There is a solid ground plane in the proximity of the PLL power pins.
2. A 1µF ceramic NP capacitor de-coupling capacitor is installed adjacent to the PLL power and ground pins.
3. A series 100Ω resistor is inserted in each PLL 5 volt supply.
4. 5 VDC power is clean, preferably being supplied from a linear regulator in close proximity.

Digital power may be derived from system digital +5 volts. If necessary insert a ferrite bead in series with the supply trace. A 47 µF capacitor should be placed across the common +5 VDC for V_{DD5}, V_{DDAD} and V_{DDDA} to act as a reservoir for heavy currents drawn by D/A converters and memory. At least one 0.1 µF capacitor should be located adjacent to V_{DD3} and V_{DD5} pins along each side of the TMC2376 to supply transient currents.

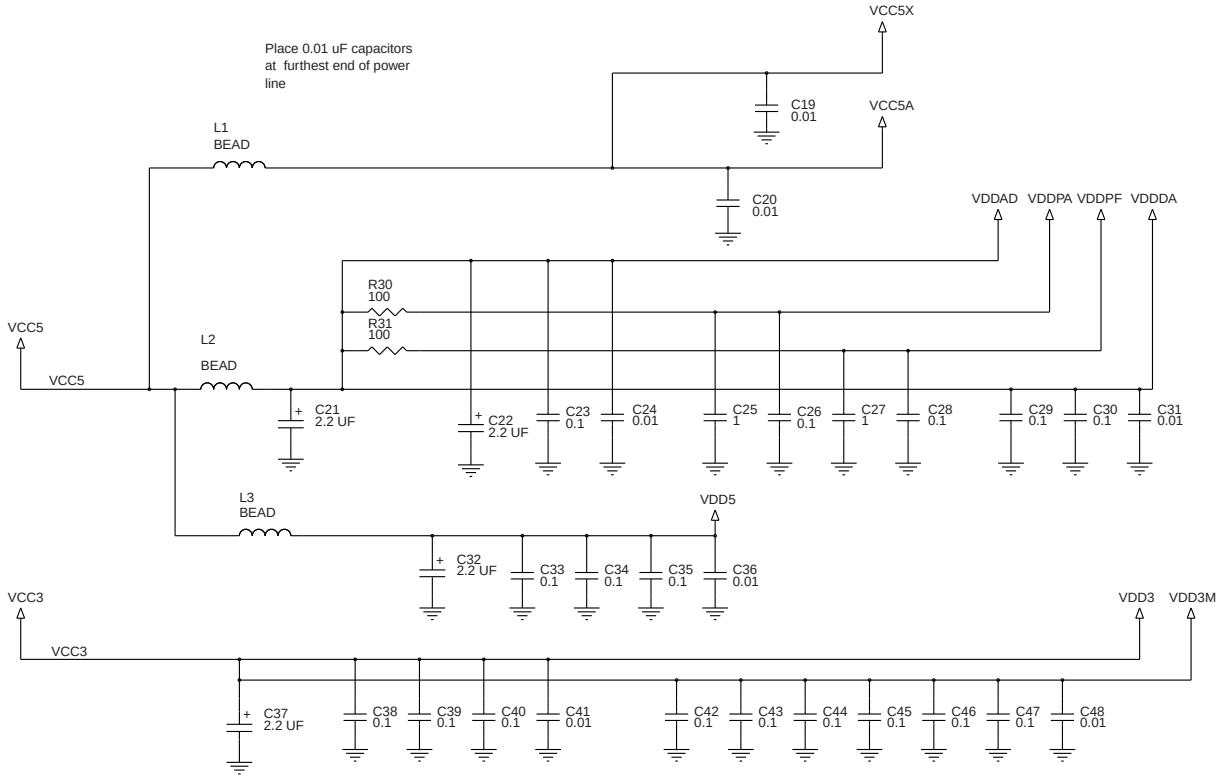


Figure 29. Power Distribution Strategy

Printed Wiring Board Layout

Overall system performance is strongly influenced by the PWB design. Layout and connection principles are embodied in Figure 30. Layout, Connection and Power Distribution Strategy. PWB design tips are:

- Locate the TMC2376 circuit near the board edge, near to video output connectors.
- Route analog traces over the ground plane.
- Position localized components, such as reference resistors close to the TMC2376.
- If a crystal oscillator is used locate the package close to the TMC2376. If a remote clock is used, make the trace connection a transmission line and terminate 330/220 ohm or equivalent to match line impedance.
- Cleanly route RGB video inputs to the TMC2376 treating connection as transmission lines.
- Segregate video traces from digital traces and areas of noise.
- Tightly group the components for each CVBS or S-video video filter. Keep the path between the filters and the CVBS and S-video connectors short.
- Use a contiuous ground plane.
- Separate analog and digital power planes or use individual traces to connect power.

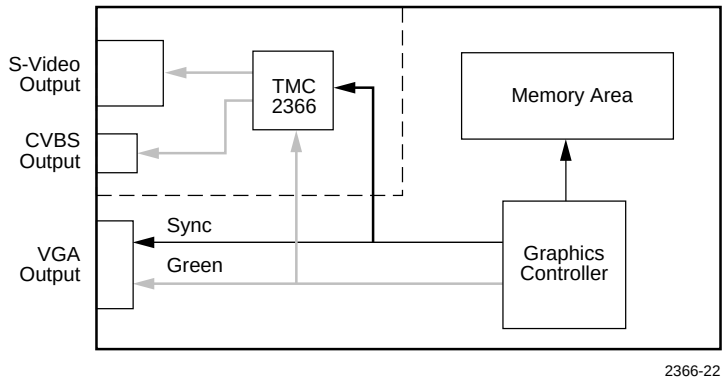


Figure 30. Layout, Connection and Power Distribution Strategy

Video Formats/Register Settings

Incoming VGA Formats

Since the TMC2376 incorporates line rate and frame rate conversion, a wide range of video formats can be accepted. Up to 1024x768 resolution, the TMC2376 can be programmed to be compliant with the VESA Standard, VESA Guideline and Industry Standard timing modes shown in Table 8 which are defined in the VESA Display Monitor Timing Specifications Version 1.0, Revision 0.7. Modes numbers listed in Table 8 correspond to the modes programmed into the PRT.C file of the Fairchild demonstration firmware source code.

Table8. Supported VESA and Industry Standard Timing Formats

Mode No.	Type	VGM File	Active pixels, HxV	Frame rate (Hz)
1	IS	NECPC400	640x400	56
2	VESA	DMT648A	640x350	85
		DMT648B	640x400	85
		DMT7285	720x400	85
3	IS	VGA_m1	720x350	70
		VGA_m2	720x400	70
4	VESA	VS901101	640x480	72
		DMT6475	640x480	75
		DMT6485	640x480	85
5	IS	XGA6475	640x480	75
6	MAC	MAC13LC	640x480	66
7	IS	VGA_m3	640x480	60
8	VESA	VG900602	800x600	60
		DMT8075	800x600	75
		DMT8085	800x600	85
9	VESA	VG900601	800x600	56
10	MAC	MAC_16	832x624	75
11	VESA	VS900603	800x600	72
12	VESA	DMT1085	1024x768	85
13	VESA	XGA1076	1024x768	75
	IS	DMT1075		
14	IS	XGA_m5	1024x768	60
	VESA	VS910801	1024x768	70
15	VESA	VG9001101	1024x768	60

Programming Strategy

To program the internal registers, external firmware must communicate with the TMC2376 via the R-bus. Several control bits must be set in the command registers and nine parameter registers must be programmed with values derived from auto-sense algorithms residing in firmware running on a remote micro-controller or software residing on a host.

First, the command registers must be programmed with the correct bits for D/A format, PAL/NTSC, filter modes, gains, D/A power and A/D power. Next, TMC2376 internal registers must be read to retrieve the count of the number of incoming TV lines and the length of each line measured in $4f_{SC}$ clock cycles. Finally, based upon these register values, the nine TMC2376 parameter registers can be programmed with values extracted from lookup tables which contains register values corresponding to common resolutions such as 640x400, 640x480, 800x600 and 1024x768.

Accessing the 10-bit registers via 8-bit data words over the R-bus is discussed in the Serial Control Port section of this data sheet.

Programming the Command Registers

For most applications, the two ten bit command registers, CR and CRE can be programmed to set the video output format (RGB or CVBS, Y/C), video standard (PAL or NTSC) and the flicker filter ON. Typical command register settings are listed in Table 9.

Table 9. Command Register Setting

2366/76 Pointer	RGB		CVBS		RGB Zoom	
	PAL	NTSC	PAL	NTSC	PAL	NTSC
11,10	0103h	0103h	0002h	0000h	0107h	0105h
15,14	0001h	0001h	0001h	0001h	0001h	0001h

Zoom Mode

To set up the zoom mode, register 11, bit 2 must be set HIGH while the value of IHAW must be half the normal setting. For example, if the incoming video format is VESA DMT7285 and the outgoing video standard is PAL, then IHAW must be reduced from 750 to 375. Table 9 also shows the settings for the zoom mode.

Read Only Registers

Incoming video timing and format can be estimated by interrogating two registers:

IVC, Input Vertical Count. The number of horizontal lines between vertical sync pulses.

Once IVC is read, since the aspect ratio of the video is known to be 4:3, the incoming resolution is known. Usually, this will be 1024x768, 800x600, 640x480 or 640x400. Outside this range, the displayed image should default to the internal test pattern, BiPGen. Note that IVC is a 10-bit register, so 1280x1024 resolution will cause wrap around, leading to an error that must be sensed by checked the line frequency through IHC.

IHC, Input Horizontal Count. The number of $4f_{SC}$ ticks between horizontal sync pulses. From IHC, the incoming line rate can be estimated to enable the incoming sampling rate to be set without overloading the capacities of line memories.

Note that since IHC is a 9-bit register, so long lines will cause wrap around (see PAL VGA_m3), leading to an error that must be corrected. If value in $0 < IHC < 128$, assume that the line count exceeds 512, then add 512 to the IVC value to obtain the 'correct' IVC.

Programming the Parameter Registers

By analyzing data extracted from the IHC and IVC registers, values can be derived to load the nine 10-bit parameter registers: IHO, IVO, IHAW, ILS, IHS, VSC, OHO, OVO and HSC.

Prior to running the analysis, the two command registers CR and CRE must be loaded to set the output video format and output TV standard while defaults can be used for the other bits.

Decision Tree

One straight forward way of implementing the TMC2376 programming firmware or software is solve several equations to obtain values to be loaded into registers. However, because linear solution of the equations is not possible, a more efficient approach is to set up a decision tree to classify incoming video timing by type.

First, lines per frame and line frequency of the incoming video timing must be read from the TMC2376 IVC and IHC registers. Next, these values are passed through the decision tree to classify the timing. Once the type has been determined, corresponding values are downloaded to registers in the PC-to-TV converter.

Based upon the values of IVC, IHC and PAL/NTSC, the process of selecting one of 16 tables ripples through two levels in a decision tree. IVC determines the incoming resolution. There are four resolution categories:

Table 10. Resolution categories

IVC min.	IVC max.	Resolution
420	450	640x400
498	530	640x480
620	670	800x600
799	809	1024x768

After categorizing the resolution, the timing format is estimated based upon the value of IHC. The ranges are as shown in Table 11.

Table 11. Format Subcategories

	Mode No.	Base Format	IVC min.	IVC max.	IHC min.	IHC max.
640x400	1	NECPC400	420	441	-	-
	2	DMT7285	442	446	-	-
	3	VGA_m2	447	450	-	-
640x480	4	DMT6475	495	505	-	-
	5	XGA6475	506	530	400	477
	6	Mac13LC	506	530	420	533
	7	VGA_m3	506	530	-	-
800x600	8	VG900602	620	650	392	487
	9	VG900601	620	650	-	-
	10	MAC_16	650	660	-	-
	11	VS900603	660	670	-	-
1024x768	12	DMT1085	799	809	218	270
	13	XGA1076	799	809	243	303
	14	XGA_m5	799	809	278	340
	15	VG901101	799	809	-	-

Parameter Register Values

Parameter register values are listed for 640x400, 640x480, 800x600 and 1024x768 resolutions in Table 12, Table 13, Table 14, Table 15, Table 16, Table 17, Table 18, and Table 19. Each table shows the IHO, IVO, IHAW, ILS, IHS, VSC, OHO, OVO and HSC parameter register values for either NTSC and PAL. If the values of VSC, OVO and HSC can be changed by an external source such as a TV remote control unit, then limits: VSCmax, OVOmax, OVOmin, HSCmax and HSCmin should be incorporated into the firmware to prevent the output video from becoming unstable. If zoom is to be used, then the VSC value should be set to the value VSCzoom and the value of IHAW halved. If the vertical scaling is to be adjustable, then the value of ILS must track the value of VSC.

Table 12. NTSC Parameter Register Values, 640x400 Resolution

	Pointer	NECPC400	DMT658A	DMT658B	DMT7285	VGA_m2
fV		56.416	85	85	85	70
fH		24.823	37.86	37.861	37.927	31.469
H		440	445	445	446	449
fS		19.48	26.76	29.445	29.5	24.13
IHC	A,B	72	377	377	377	454
IVC	C,D	439	444	444	445	448
IHO	0,1	170			147	142
IVO	2,3	23			35	31
IHAW	4,5	685			607	680
ILS	6,7	197			203	205
I_HS	8,9	856			705	765
VSC	E,F	6			0	0
OHO	20,21	151			156	151
OVO	22,23	50			39	41
HSC	24,25	0			8	0
VSCmax		5			5	4
OVOmax		60			50	50
OVOmin		40			34	34
HSCmin		9			13	8
HSCmax		0			0	0
VSCzoom		6			6	0

Table 13. PAL Parameter Register Values, 640x400 Resolution

	Pointer	NECPC400	DMT658A	DMT658B	DMT7285	VGA_m2
fV		56.416	85	85	85	70
fH		24.823	37.86	37.861	37.927	31.469
H		440	445	445	446	449
fS		19.48	26.76	29.445	29.5	19.4
IHC	A,B	203	466	466	467	562 (50)
IVC	C,D	439	444	444	445	448
IHO	0,1	175			120	70
IVO	2,3	17			35	17
IHAW	4,5	765			750	765
ILS	6,7	212			203	211
I_HS	8,9	950			820	765
VSC	E,F	2			0	0
OHO	20,21	247			240	230
OVO	22,23	64			68	64
HSC	24,25	0			0	0
VSCmax		2			4	2
OVOmax		76			82	76
OVOmin		51			54	51
HSCmax		12			10	16
HSCmin		0			0	0
VSCzoom		6			0	0

Table 14. NTSC Parameter Register Values, 640x480 Resolution

	Pointer	DMT6475	XGA6475	MAC13LC	VGA_m3
fV		75	75	66.7	59.94
fH		37.5	39.375	35	31.469
H		500	525	525	525
fS		29.8	28.74	35.8	22.97
IHC	A,B	381	363	506	454
IVC	C,D	499	524	524	524
IHO	0,1	192	156	193	161
IVO	2,3	12	23	37	30
IHAW	4,5	670	690	684	684
ILS	6,7	210	210	215	212
I_HS	8,9	793	793	895	798
VSC	E,F	9	9	8	9
OHO	20,21	151	153	151	151
OVO	22,23	39	39	37	39
HSC	24,25	0	0	0	0
VSCmax		10	10	11	11
OVOmax		47	47	43	43
OVOmin		31	31	16	18
HSCmax		8	8	6	60
HSCmin		0	0	0	0
VSCzoom		9	9	6	6

Note: If IHC < 128, 512 is added to value.

Table 15. PAL Parameter Register Values, 640x480 Resolution

	Pointer	DMT6475	XGA6475	MAC13LC	VGA_m3
fV		75	75	66.7	59.94
fH		31.5	39.375	35	31.469
H		500	525	525	525
fS		35.7	28.74	35.8	22.97
IHC	A,B	472	449	506	562(50)
IVC	C,D	499	524	524	524
IHO	0,1	230	170	228	194
IVO	2,3	11	20	26	30
IHAW	4,5	760	760	760	780
ILS	6,7	233	230	238	240
I_HS	8,9	950	900	1023	900
VSC	E,F	3	5	3	1
OHO	20,21	230	241	250	242
OVO	22,23	56	51	51	51
HSC	24,25	4	0	0	3
VSCmax		4	6	4	4
OVOmax		61	61	62	62
OVOmin		41	41	14	14
HSCmax		11	11	12	8
HSCmin		0	0	0	0
VSCzoom		0	5	3	4

Note: If IHC < 128, 512 is added to value.

Table 16. NTSC Parameter Register Values, 800x600 Resolution

	Pointer	VG900602	VG900601	MAC_16	VS900603
fV (Hz)		60.317	56.25	75	72.188
fH (kHz)		37.879	35.156	49.1	48.077
H		628	625	654	666
fS (MHz)		27.65	25.66	40.5	35
IHC	A,B	377	407	291	297
IVC	C,D	627	624	653	665
IHO	0,1	200	178	189	157
IVO	2,3	20	11	8	12
IHAW	4,5	684	690	689	689
ILS	6,7	212	217	212	212
I_HS	8,9	862	821	823	825
VSC	E,F	19	19	22	20
OHO	20,21	151	151	151	151
OVO	22,23	37	33	35	35
HSC	24,25	0	10	0	0
VSCmax		20	19	22	23
OVOmax		43	44	42	42
OVOmin		16	16	28	28
HSCmax		5	6	8	7
HSCmin		0	0	0	0
VSCzoom		18	18	22	18

Table 17. PAL Parameter Register Values, 800x600 Resolution

	Pointer	VG900602	VG900601	MAC_16	VS900603
fV (Hz)		60.317	56.25	75	72.188
fH (kHz)		37.879	35.156	49.1	48.077
H		628	625	654	666
fS (MHz)		23	21.37	29.95	29.2
IHC	A,B	467	508	361	368
IVC	C,D	627	624	653	665
IHO	0,1	215	202	216	189
IVO	2,3	17	13	15	6
IHAW	4,5	720	721	771	772
ILS	6,7	256	260	234	242
I_HS	8,9	900	893	938	948
VSC	E,F	11	10	17	15
OHO	20,21	218	218	249	242
OVO	22,23	42	42	53	50
HSC	24,25	9	9	0	0
VSCmax		11	9	18	17
OVOmax		50	50	64	60
OVOmin		33	33	42	40
HSCmax		16	14	10	10
HSCmin		0	0	0	0
VSCzoom		18	16	18	15

Table 18. NTSC Parameter Register Values, 1024x768 Resolution

	Pointer	DMT1085	XGA1076	XGA_m5	VG901101
fV		85	60	70	75.782
fH		68.7	48.363	56	61.08
H		808	806	804	806
fS		50.1	29	41	42
IHC	A,B	204	303	253	232
IVC	C,D	807	805	803	805
IHO	0,1	179	194	212	218
IVO	2,3	36	28	32	29
IHAW	4,5	580	690	690	680
ILS	6,7	215	197	216	216
I_HS	8,9	728	790	838	853
VSC	E,F	29	32	29	29
OHO	20,21	151	151	151	153
OVO	22,23	38	46	38	38
HSC	24,25	12	0	0	0
VSCmax		28	31	29	25
OVOmax		45	60	46	45
OVOmin		16	28	30	30
HSCmax		20	10	6	8
HSCmin		0	0	0	0
VSCzoom		32	32	32	28

Table 19. PAL Parameter Register Values, 1024x768 Resolution

	Pointer	DMT1085	XGA1076	XGA_m5	VG901101
fV		85	75.782	70	60
fH		67	61.08	56	48.363
H		808	806	804	806
fS		51.64	42	34	29
IHC	A,B	256	291	314	366
IVC	C,D	807	805	803	805
IHO	0,1	184	221	237	247
IVO	2,3	31	28	28	16
IHAW	4,5	640	775	700	770
ILS	6,7	249	249	249	256
I_HS	8,9	750	775	845	980
VSC	E,F	23	23	23	23
OHO	20,21	224	216	214	226
OVO	22,23	45	45	47	42
HSC	24,25	22	23	13	4
VSCmax		22	22	24	22
OVOmax		52	54	56	48
OVOmin		12	36	38	32
HSCmax		48	28	23	12
HSCmin		0	0	0	0
VSCzoom		32	32	30	23

Table 20. Default BiPGEN Test Pattern Parameters

	Pointer	NTSC	PAL
IHO	0,1	128	128
IVO	2,3	128	104
IHAW	4,5	512	512
ILS	6,7	220	274
I_HS	8,9	766	766
VSC	E,F	0	1
OHO	20,21	192	192
OVO	22,23	32	32
HSC	24,25	0	43
VSCmax		5	6
OVOmax		36	32
OVOmin		18	6
HSCmax		5	56
HSCmin		0	34
VSCzoom		0	0

Notes:

Notes:

Notes:

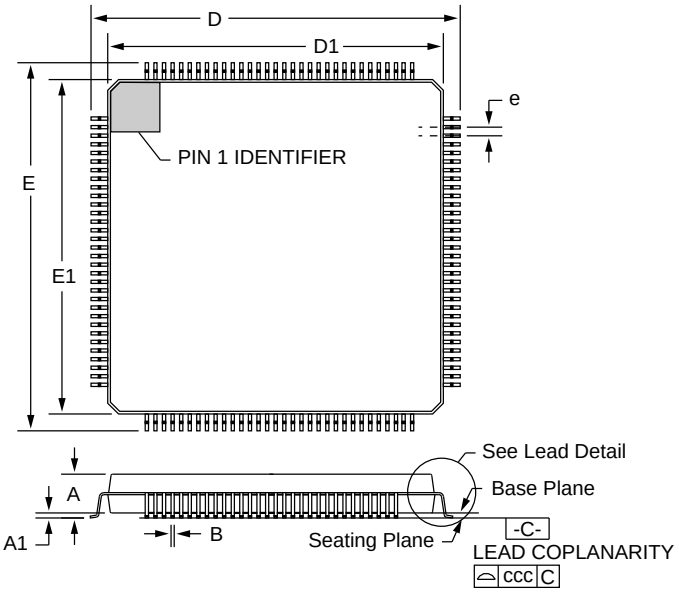
Mechanical Dimensions

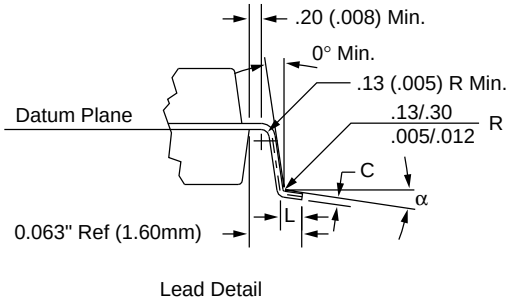
128 Lead MQFP

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.160	—	4.07	
A1	.010	—	.25	—	
B	.012	.018	.30	.45	3, 5
C	.005	.009	.13	.23	5
D/E	1.219	1.238	30.95	31.45	
D1/E1	1.098	1.106	27.90	28.10	
e	.0315 BSC		.80 BSC		
L	.029	.041	.73	1.03	4
N	128		128		
ND	32		32		
α	0°	7°	0°	7°	
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Controlling dimension is millimeters.
3. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be .08mm (.003in.) maximum in excess of the "B" dimension. Dambar cannot be located on the lower radius or the foot.
4. "L" is the length of terminal for soldering to a substrate.
5. "B" & "C" includes lead finish thickness.





Lead Detail

Preliminary Information

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2376KCC	0°C to 70°C	Commercial	128 Lead MQFP	2376KCC

Use Restriction

Technology licensed from a third party has been incorporated into the TMC2376. To comply with the license agreement, the TMC2376 may not be used in peripherals with the sole function of PC-to-TV scan conversion. However the TMC2376 may be incorporated into products such as:

- Laptops
- PC video controllers
- TV PC video in
- Video Kiosks

that have a primary function other than scan conversion. Contact the factory for licensing details.

Preliminary Information